

Normally-off logic based on resistive switches – Part I: Logic gates

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Abstract—To extend the scaling of digital integrated circuits, beyond-CMOS approaches based on advanced materials and novel switching concepts are strongly needed. Among these approaches, the resistive switching memory (RRAM) allows for fast and nonvolatile switching at scalable power consumption. This work presents functionally-complete logic gates based on RRAM technology. Logic computation is obtained through conditional switching in RRAM circuits with serially-connected switches. AND, IMP, NOT and bit transfer operations are demonstrated, each using a single clock pulse, while other functions (*e.g.*, OR and XOR) are achieved in multiple steps. The results support RRAM logic for normally-off digital circuits with extremely high density.

Keywords: Resistive switching memory (RRAM), logic gates, logic circuits, logic computing

I. INTRODUCTION

Moore's law has driven the scaling of CMOS technology for logic and memory applications for almost 40 years. Today, CMOS scaling is becoming increasingly hard mainly due to the increase of the subthreshold leakage current, which raises the static and stand-by power consumptions in digital circuits. To suppress the leakage-induced power, novel device technologies, such as the tunnel field-effect transistor (TFET) [1] and the nanoelectromechanical switch (NEMS) [2] with improved subthreshold slope, have been proposed. A more radical approach consists in adopting materials-based switching, such as spintronic [3]–[7] and resistive switching [8]–[10]. In most cases, the switching states of the material are nonvolatile, which allow for storing the input/output states of a logic gate even without any power supply. This approach allows for normally-off logic circuits having two major benefits: (i) the suppression of the static power and (ii) the storage of the computed states in the logic circuit, which may thus be capable of instant boot.

Among the nonvolatile logic concepts, those based on resistive (or memristive) switching have received strong interest due to the scalable operation current [11], [12], the high switching speed [13], [14], and the simple 2-terminal structure, which makes it possible to integrate a switch in a crossbar circuit with individual device area of $4F^2$, where F is the minimum feature size allowed by the lithography. Resistive switching is nonvolatile, thus providing the basis for the resistive switching memory (RRAM) for

high-density and embedded storage [15]–[17]. RRAM was initially proposed for application as a reconfigurable switch in field-programmable gate array (FPGA), to reduce the area usually occupied by SRAM-based switches [18]–[21]. Material implication (IMP) has been demonstrated in RRAM circuits with two parallel-connected switches [8], [9]. IMP allows for functionally-complete logic through the iteration of multiple computing steps, however achieving other logic functions such as AND or NOT in a single clock pulse would allow for greatly reduced computation time and simplified logic operation.

This work demonstrates functionally-complete logic gates based on RRAM switches. Logic functions are performed through conditional switching in RRAM circuits with serially-connected switches. Unlike previous works where only IMP and its associated operations (*e.g.*, negative IMP, reverse IMP, NOT) were achieved within one clock pulse [8], [9], here we demonstrate AND, IMP, NOT and bit transfer operations, all with one clock pulse and 2 switches. In our approach, cascading of more logic operations is possible as the input and output have the same nature, namely, a resistance state in a RRAM switch [3], [9]. Other functions, *e.g.*, OR and XOR, can be achieved by a combination of the primary operations in a sequence of multiple computing steps. We focus on single logic operations in this work while circuit operations and complex functionalities will be addressed in the companion paper [22].

II. RRAM CHARACTERISTICS

To demonstrate logic operations with resistive switching, we used electrochemical RRAM devices provided by Adesto Technologies [15]. The device stack consisted of a W bottom electrode, a GeS_2 solid electrolyte and a Ag top electrode (TE). Resistive switching in these devices is due to the

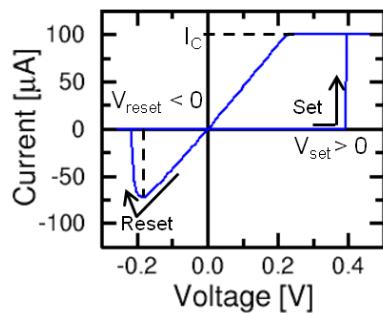


Fig. 1. Measured I-V curve for the RRAM device showing set and reset transitions under positive and negative voltages, respectively.

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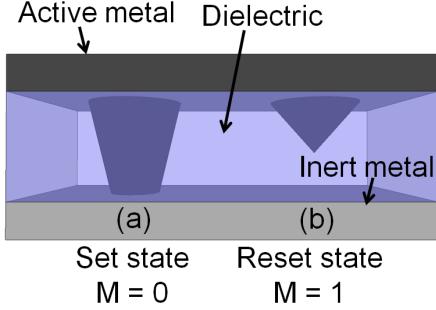


Fig. 2. Schematic illustration of the RRAM switch in the set ($M = 0$, a) and reset ($M = 1$, b) states. Active metal is Ag, while the dielectric is GeS₂.

voltage-induced migration of Ag cations within the solid electrolyte, causing the formation/disruption of a conductive filament (CF), or conductive bridge [23], [24]. Fig. 1 shows the I-V characteristics of the RRAM device used in our work. Application of a positive voltage above the set voltage V_{set} leads to set transition from high to low resistance, as a result of the formation of the CF. The maximum current is fixed by the measurement setup to a compliance current $I_C = 100 \mu\text{A}$, to allow control of the CF size, hence of the resistance R . After set transition, the voltage snaps back to a value V_C of about 0.15 V, which identifies the characteristic voltage to induce migration in the CF on the 1-s timescale of the experiment [25]. Application of a negative voltage above the reset voltage V_{reset} results in the reset transition from low to high resistance, revealing the dissolution of the CF by Ag migration back to the TE.

Fig. 2 schematically shows the two states of the RRAM devices, namely set state (a) and reset state (b). In the set state, the RRAM has a low resistance R due to the CF connecting top and bottom electrodes. After disconnection of the CF in the reset state, the RRAM displays a high resistance. The shape of the CF in the set and reset states may vary depending on the RRAM concept, material and type of operation. Previous results on electrochemical RRAM devices showed that the CF protrudes from the top electrode, *i.e.*, the anode during the set transition, toward the bottom electrode [26]–[28], as shown in Fig. 2. The opposite behavior is instead proposed in some interpretations [29]–[31]. Electrochemical RRAM devices are considered in this work because of their extremely low power operation, which was demonstrated in the few-nA range [32], [33] and few-ns timescale [34]. In addition, electrochemical RRAM displays digital switching thanks to a large resistance window of about 6 decades [33] which can be explained by the variation of CF diameter between the atomic size (about 0.3 nm) and few tens of nm. Additional contributions to the resistance range come from the size-dependent resistivity due to surface roughness scattering and the transition from metallic conductivity to hopping conduction at low defect concentration [35]. Digital switching behavior is also promoted thanks to the abrupt reset transition in Fig. 2, compared to the gradual resistance increase in bipolar oxide-based RRAM devices [36]. The digital switching properties of electrochemical RRAM support Ag-GeS₂ as an ideal device for logic operation.

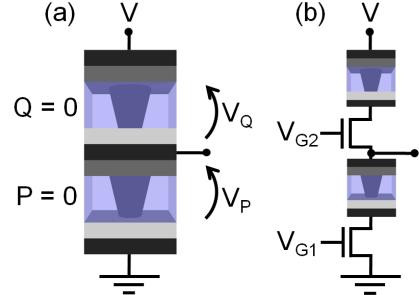


Fig. 3. Schematic layout of the RRAM-based logic gate (a) and of the 2T2R structure used for experimental verification (b). Two switches are connected in series, while the logic operation is dictated by the applied voltage.

III. RRAM LOGIC GATES

We first assign two logic values to the device states in Fig. 2. The set and reset states are defined as states $M = 0$ and 1 , respectively, where M is the state variable reflecting the value of V_{set} in the I-V curve [10]. In a RRAM logic gate, the switching devices (or switches) both store the input/output states, and operate in response to an applied driving pulse. Different logic functions are achieved by different values of the pulse voltage, *e.g.*, high/low voltages [10], or positive/negative voltages. This is different from the conventional CMOS logic gates, where the logic functionality relies on the transistor gain at the basis of the digitalization. RRAM logic, instead, features no gain and relies on *conditional switching*, where one switch in the logic gate can change its state depending on the value of the input (*i.e.*, initial) states. Similar gain-less logic approaches were previously reported for devices based on resistive switching [9], spin-torque magnetic switching [7] and phase change switching [10].

In addition, RRAM logic differs from CMOS logic by the topological organization of the logic gate: in CMOS logic, in fact, each logic function has a specific circuit topology, *e.g.*, a NAND gate differs from a NOR gate by the connection of pull-up and pull-down transistors. RRAM logic instead totally lacks topological organization of the logic gates, thus allowing for standardization of the circuit architecture through the adoption of the crossbar array with extremely high density achieved by the small device size of $4F^2$ [37]. Another key difference from CMOS logic is that the output states are stored in the logic gate even after the supply is turned off, as a result of the nonvolatile behavior of the switch. Since there is no need for a supply voltage to sustain the output state in a RRAM device, the off-power consumption is theoretically zero. This allows normally-off operation of the logic circuit with a consequent suppression of the static and stand-by power.

A. Experimental setup

Fig. 3a schematically shows the structure of a switch-based logic gate. Two RRAM devices P (bottom switch) and Q (top switch) are connected in series. Both switches can be accessed individually, *e.g.*, to write the input state or for reading, by application of a voltage V_P or V_Q as shown in Fig. 3a. To drive the logic operation, however, the switches must be biased together in the serial configuration, by

applying a driving voltage V to the top electrode while leaving the intermediate electrode floating and the bottom electrode grounded. Depending on the states of P and Q and on the polarity of V , conditional switching can take place in either switch, thus resulting in a compute operation. Application of a positive V can result in a set transition of P or Q , while a negative V can induce reset transition in either switch. Finally, the output can be obtained as the final states P' and Q' of the switches, which can then be used as new input states in the same switch or can be transferred to other switches for further operations [10].

To experimentally demonstrate the fundamental logic gates, we used 2 RRAM devices connected to a switching matrix (Agilent 34970A). The switching matrix was needed to prepare separately the 2 switches with the parameter analyzer (Agilent B1500A) and then connect them in series to operate the logic function. The resistance of the RRAM device was measured both before and after the logic operation. For more complex logic gates, namely OR and XOR, we developed a printed circuit board with all the connections. RRAM devices were wire-bonded to the board while the wiring reconfiguration was performed using external transistors. To protect the resistive state during the reconfiguration and to control the resistance after set transition, we used 1T1R devices, where a transistor is connected in series to the switching device. The resulting 2-transistor/2-resistor (2T2R) structure is schematically shown in Fig. 3b. To infer the state of RRAM device before and after logic computation, we read the switching current during the computation pulse. A similar board was developed also to demonstrate the 1-bit full adder presented in the companion paper [22].

B. AND gate and bit transfer

Fig. 4 schematically describes the operation of an AND gate, showing, from left to right, the initial (input) states of the switches, the I-V characteristics with the corresponding RRAM switching, the final (output) states and the experimental demonstration of the logic gate. The input states may be directly written in the two RRAM switches, or be transferred there from other switches, or be the result of a previous operation in the switches. The logic operation is enabled by application of a driving pulse of positive voltage ($2V_C < V < 2V_{set}$) across the two serially-connected switches. The applied voltage is positive, thus the switching can only induce set transition in either switch. If $P = Q = 0$ (a), no switching can take place since the switches are both in the set state, thus the final states are the same as the initial states, namely $P' = Q' = 0$. For $P = 0$ and $Q = 1$ (b), most of the applied voltage drops across Q , causing set transition to $Q' = 0$. Similarly, for $P = 1$ and $Q = 0$ (c), the large voltage drop across P induces set transition to $P' = 0$. Finally, if both P and Q are equal to 1 (d), the voltage divides equally across P and Q , resulting in no switching in either P or Q , since $V < 2V_{set}$. As a result of this conditional switching, both output states P' or Q' provide the AND function of the input states P and Q , as summarized in Tab. I. As a special case of the AND operation for $Q = 1$, the state of P is automatically

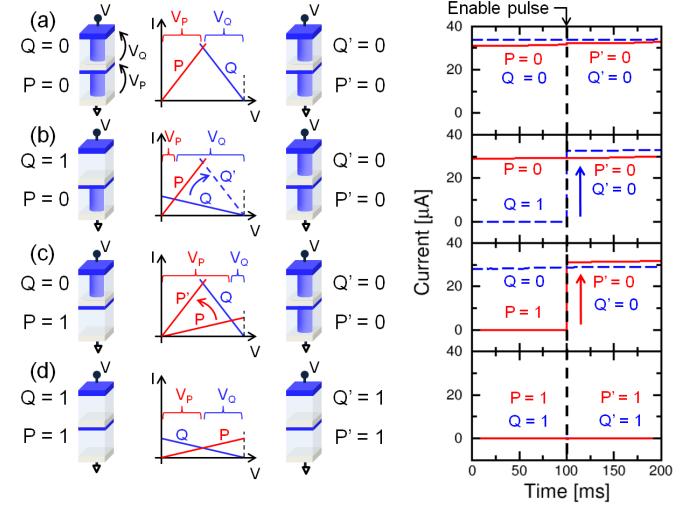


Fig. 4. Schematic of the RRAM-based AND gate showing (from left to right) the initial (input) states P and Q , the I-V curves for RRAM devices, the final (output) states and the experimental demonstration, where the current was measured at $V = 50$ mV before and after the enable pulse. The four initial states of P and Q are considered, namely $P = Q = 0$ (a), $P = 0$ and $Q = 1$ (b), $P = 1$ and $Q = 0$ (c) and $P = Q = 1$ (d). A positive voltage is applied, resulting in AND operation.

transferred to Q' , serving as a scheme for bit transfer between two switches.

The AND function $P \cdot Q$ is experimentally demonstrated for 2 wire-bonded conductive-bridge RRAM switches, as shown by the current measured at $V = 50$ mV shown in Fig. 4. A 100 ms enable pulse with voltage 0.8 V was applied to drive the logic operation, resulting in a set transition from 1 to 0 for $P = 0$ and $Q = 1$ (b) and $P = 1$ and $Q = 0$ (c). No switching takes place for $P = Q$ in (a) and (d). the conductance for state 0 was around 0.6 mS, corresponding to a resistance of about 1.65 k Ω . This state was achieved by limiting the current to $I_C = 100$ μ A during the initial writing and logic operation. The compliance current was maintained by properly-biased transistors in series with the switches in the so-called one-transistor/one-resistor (1T1R) configuration [11], [12]. The random variability of state 1 may represent an issue for the case $P = Q = 1$ in Fig. 4d. For instance, assuming that P has a higher resistance than Q , V_P is higher than V_Q , thus possibly inducing set transition in P . However, P also has a higher set voltage V_{set} than Q , due to the relationship between V_{set} and R [35]. Also, even in the case where the set transition is initiated in P , soon V_P decreases in the voltage divider, thus the set process is inhibited. These effects are expected to prevent variability-induced set transition in the case $P = Q = 1$. Despite such inherent robustness of the AND gate against variability, variation of resistance and V_{set} should be minimized as much as possible to ensure high reliability.

C. IMP, NOT and regeneration

Fig. 5 shows the material implication (IMP) gate, consisting of the same structure as the AND gate but operated under a negative voltage $|V| < 2V_{reset}$. Similar to Fig. 4, Fig. 5 shows, from left to right, the initial (input) states, the I-V curves with RRAM switching, the final (output) states and the measured

TABLE I
TRUTH TABLE FOR AND OPERATION, HIGHLIGHTING THE SPECIAL CASES OF BIT TRANSFER $Q' = P \cdot 1$.

P	Q	$P' = P \cdot Q$	$Q' = P \cdot Q$
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

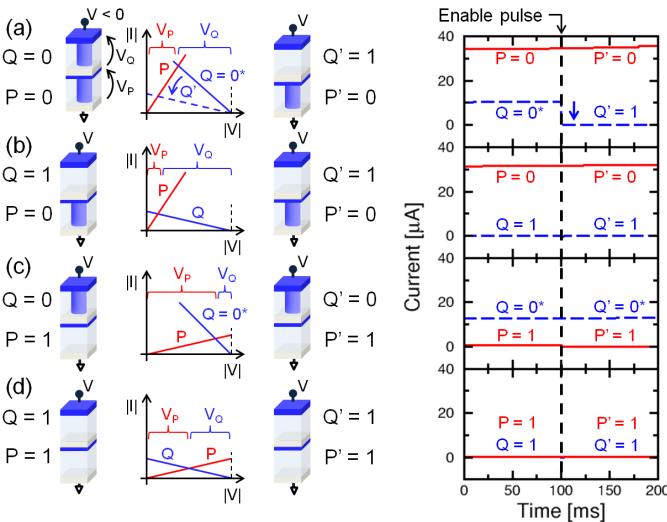


Fig. 5. Schematic of the RRAM-based IMP logic gate showing (from left to right) the initial (input) states P and Q, the I-V curves for RRAM devices, the final (output) states and the experimental demonstration, where the current was measured at $V = 50$ mV before and after the enable pulse. The four initial states of P and Q are considered, namely $P = Q = 0$ (a), $P = 0$ and $Q = 1$ (b), $P = 1$ and $Q = 0$ (c) and $P = Q = 1$ (d). A negative voltage is applied, resulting in IMP operation.

TABLE II

TRUTH TABLE FOR IMP OPERATION, HIGHLIGHTING THE SPECIAL CASES OF BIT INVERTER $Q' = \text{NOT}(P) = P \rightarrow 0^*$.

P	Q	$P' = P$	$Q' = P \rightarrow Q$
0	0^*	0	1
0	1	0	1
1	0^*	1	0^*
1	1	1	1

conductance before/after application of the enable pulse. For $P = Q = 0$, the voltage divides equally across P and Q, thus reset occurs in neither P nor Q since $|V| < 2V_{reset}$. To allow for switching in this case, Q is prepared in the set state with a smaller compliance current I_C^* , e.g., $I_C^* = 30 \mu\text{A}$ in Fig. 6, thus resulting in a smaller CF and in a smaller conductance (about one third of P in Fig. 6). This will be referred to as state $Q = 0^*$ in the following. The imbalance between the two states results in more voltage drop across Q, thus forcing transition to $Q' = 1$ with no disturb to P, as shown by the measured conductance of Q decaying to a small value after the enable pulse in Fig. 5a. For $P = 0$ and $Q = 1$ (b), the voltage drop across P is negligible, thus preventing any reset transition to occur in P. On the other hand, the large voltage across Q cannot lead to any reset transition, since Q is already in the reset state. Similarly, for $P = 1$ and $Q = 0^*$ (c), reset transition is inhibited in Q due to the low voltage drop, while

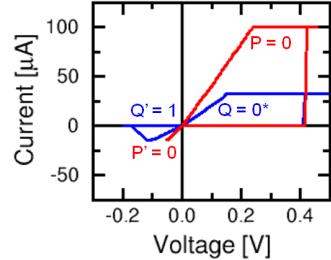


Fig. 6. Measured I-V curves during preliminary write ($V > 0$) and compute ($V < 0$) for IMP with $P = 0$ and $Q = 0^*$. For controlled switching to $Q' = 1$, Q must be set to a higher R (state $Q = 0^*$) with lower I_C .

P is already in the reset state. Finally, for $P = Q = 1$ (d), no reset is possible as both RRAMs are already in the reset state. After conditional switching, the output Q' corresponds to the IMP function $Q' = P \rightarrow Q$, as summarized in Tab. II. For the special case with $Q = 0^*$, the output Q' provides the function $Q' = \text{NOT}(P)$, thus working as a bit inverter. Fig. 5 also shows the current measured at $V = 50$ mV before and after the application of the enable pulse, indicating the reset transition from $Q = 0^*$ to 1 in (a). Transistors in the 1T1R structures were biased to high conductance to minimize the voltage drop across them.

The introduction of the third state 0^* makes regeneration steps necessary, whenever an output state 0 must serve as the second operand in an IMP operation, where 0^* is instead expected. In this case, the state 0 can be transferred to an auxiliary switch initially in state 1 by an AND operation with reduced compliance I_C^* thus resulting in state 0^* . The auxiliary switch can then be used as second input in the IMP operation. Note that, before the operand state is transferred to an auxiliary switch, there is no need for a preliminary read operation, since state 1 will also be transferred without modification. The opposite case is also possible, namely an output state 0^* is needed as first operand in an IMP operation. In this case, the switch can be straightforwardly regenerated by a set operation at a voltage V between V_C and V_{set} in Fig. 1. In fact, state 0^* will switch to 0 by CF growth accelerated by the voltage being higher than V_C , while state 1 is not disturbed since $V < V_{set}$. Fig. 7 shows the measured I-V curves for state 0 (a), 0^* (b) and 1 (c), indicating regeneration of state 0^* in Fig. 7b with no disturb on 0 and 1. Finally, note that 0 and 0^* can both appear as input states in AND operation, since the output is always 0, except for both initial states being $P = Q = 1$.

Another approach to achieve different reset behaviors for P and Q in Fig. 5a is to use different RRAM materials

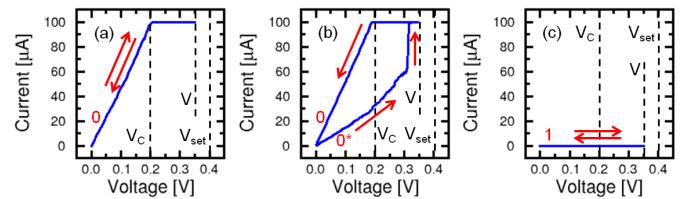


Fig. 7. Measured I-V curves during regenerate operation for the state 0 (a), 0^* (b) and 1 (c). Applying a voltage between V_C and V_{set} state 0^* switches to state 0 (b) while state 1 (c) is not disturbed since $V < V_{set}$.

for P and Q. For instance, the Ag-GeS₂ RRAM used in this work shows a remarkable asymmetry between the set and the reset processes, where the I_{reset} can be significantly smaller than I_C [32], [33], [38]. The ratio I_{reset}/I_C can be as small as 0.1 for Ag-GeS₂ RRAM devices and was shown to depend on I_C , namely an increasingly smaller I_{reset}/I_C is obtained at decreasing I_C [38]. The set/reset asymmetry was attributed to the compressive stress affecting the CF after set transition and contributing to the CF retraction during reset transition. On the other hand, RRAM based on metal oxides, such as HfO_x [11], [25], [39] and TaO_x [40], usually display symmetric set/reset processes with $I_{reset} \approx I_C$. No significant stress effects are expected in this case, due to the presence of both cations, *e.g.*, ionized Hf in HfO₂, and anions, *i.e.*, O²⁻. The opposite migration of cations and anions might minimize accumulation of impurities and stress buildup. A logic gate where P has symmetric switching ($I_{reset} \approx I_C$) and Q has asymmetric set/reset switching ($I_{reset} < I_C$) can intrinsically allow for the IMP behavior in Fig. 5. By appropriate choice of electrode/switching materials, the 2 layers can be engineered to minimize the mismatch between the values of V_{set} . In fact, CBRAM devices with V_{set} higher than 1 V (therefore similar to oxide-RRAMs) have been reported [30], [41], [42].

D. OR gate

Other logic functions can be achieved by combining IMP, NOT and AND functions discussed above. OR can be simply obtained through the DeMorgan theorem, namely

TABLE III

IMPLEMENTATION OF OR GATE IN 3-PULSES SEQUENCE WITH 5 SWITCHES. IMP OPERATIONS ARE HIGHLIGHTED IN GRAY WHILE THE OUTPUT RESULT IS HIGHLIGHTED IN GREEN.

Clock =	1	2	3
P1=A			
P2=B			
P3=0*	P1→P3	P3·P4	
P4=0*	P2→P4	P3·P4	
P5=0*			P4→P5

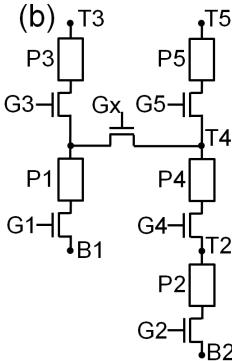
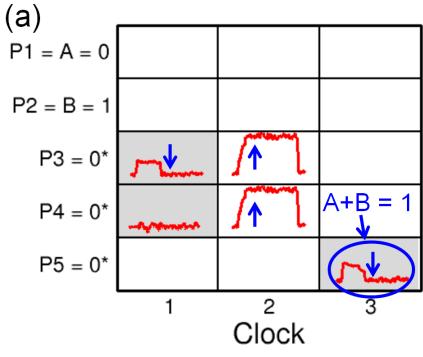


Fig. 8. Measured switching current for an OR gate with input A = 0 and B = 1 (a) and circuit used for the experimental demonstration (b). Operations in each cycle are carried out according to Tab. III. Switches are indicated as P1 through P5, with P1 and P2 serving as input, P3 and P4 serving as auxiliary switches, and P5 serving as output. Three clock pulses are used for the OR operation. Arrows indicate set and reset transitions, IMP operations are highlighted in grey.

$A+B = \text{NOT}(\text{NOT}(A) \cdot \text{NOT}(B))$. This translates into three pipelined operations, namely (i) inversion of both inputs A and B, which can be operated in parallel, (ii) AND operation and (iii) inversion of the previous output. This sequence is summarized in Tab. III, showing the 5 switches used for the operation, namely the 2 input switches P1 = A, P2 = B, the output switch P5 = A OR B, and 2 auxiliary switches P3 and P4. Switches P3 and P4 are initially prepared in state 0*, since they must operate in IMP operations aimed at inversion (see Tab. II). In the first clock pulse, P3 receives the inverted value of P1, while P4 receives the inverted value of P2. Then, AND of P3 and P4 is performed at the second clock pulse. Note that any state 0* would be regenerated to 0 in the second stage, since AND is operated at a compliance current $I_C > I_C^*$. In the third stage, P4 is inverted and transferred into the output switch P5. The output state can be either 0* or 1, thus can be readily used as second operand in a subsequent IMP operation. In case of read or other types of operation (*e.g.*, AND, or first operand in IMP), the output must be regenerated from 0* to 0, as shown in Fig. 7.

Fig. 8a demonstrates the OR operation by showing the measured current during the three stages of OR operation in Tab. III, namely NOT, AND and final NOT. The demonstration was carried out by the experimental setup in Fig. 8b, where all indicated nodes were electrically accessible to select and/or bias individual RRAM switches. Input states A = 0 and B = 1 were chosen to exemplify the logic operation. For the experimental demonstration, RRAM devices with 1T1R structures were wire-bonded for serial connection in the logic-gate architecture of Fig. 3. P3 first shows reset transition at the beginning of clock pulse #1, then undergoes set transition during the AND operation in the second clock pulse. Finally, a reset transition appears in P5 due to P4 = 0*. The final state P5 = 1 provides the output of the OR operation. The functionality of the logic gate can be similarly demonstrated for other states of the inputs A and B.

E. XOR gate

The XOR operation $A \oplus B$ can be achieved in 3 steps by cascading NOT, IMP and AND, namely:

$$A \oplus B = (A \rightarrow B') \cdot (B' \rightarrow A), \quad (1)$$

which is schematically shown in Fig. 9. Tab. IV shows the 4-pulse sequence to complete XOR operation in a circuit of 5 RRAM switches. First, A is copied from P1 to P5 with reduced compliance I_C^* to change 0 into 0*, while B is inverted in P3. In the second pulse, the inverted B is regenerated to change 0* into 0, while another inverted B is transferred into P4. These 2 pulses complete the preliminary NOT operations in Fig. 9. IMP operations are carried out in the third pulse,

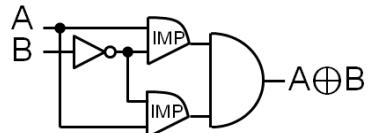


Fig. 9. Schematic layout of XOR gate achieved using NOT, IMP and AND.

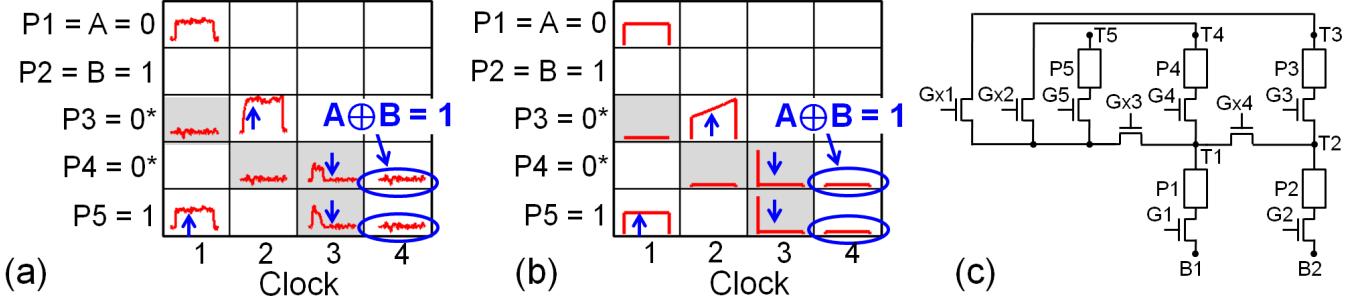


Fig. 10. Measured (a) and calculated (b) switching current for a XOR gate with input $A = 0$ and $B = 1$ and circuit used for the experimental demonstration (c). Arrows indicate set and reset transitions. Operations in each cycle are carried out according to Tab. IV.

TABLE IV

IMPLEMENTATION OF XOR GATE IN 4-PULSES SEQUENCE WITH 5 SWITCHES. IMP OPERATIONS ARE HIGHLIGHTED IN GRAY WHILE THE OUTPUT RESULT IS HIGHLIGHTED IN GREEN.

Clock =	1	2	3	4
P1=A	P1·P5			
P2=B				
P3=0*		P2→P3	P3=P3	
P4=0*			P2→P4	P1→P4
P5=1	P1·P5		P3→P5	P4·P5

with output in $P4 = A \rightarrow B'$ and in $P5 = B' \rightarrow A$. Finally, the AND product $P4 \cdot P5$ is performed in the fourth pulse. Fig. 10 shows the measured (a) and calculated current (b) as a function of time during the operation of the XOR sequence of Tab. IV, while Fig. 10c shows the circuit used for the experimental demonstration. The demonstration was carried out for input $A = 0$ and $B = 1$, resulting in an output $P4 = P5 = A \oplus B = 1$. Calculations were achieved by simulating the 2-RRAM switches with current limitation to describe the effect of the select transistors. Simulations were done by using an analytical model for RRAM set/reset temperature- and field-assisted migration of ionized defects [43]. XOR operation is essential to achieve more complex functions, such as addition which is addressed in the companion paper [22].

F. Logic-gates implementation in a crossbar array

The feasibility of logic gates in the previous subsections was discussed assuming a reconfigurable wiring, where individual switches were connected with suitable wires to compute each operation. Although useful for practical demonstration of RRAM logic, reconfigurable wiring is too expensive for

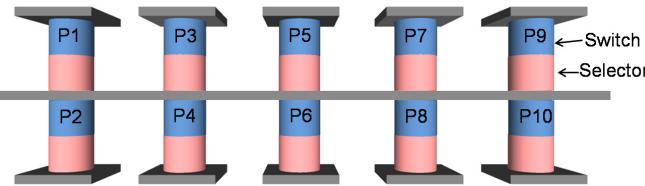


Fig. 11. Cross-section of a portion of a crossbar array for implementation of any generic function. Each logic cell includes a switch element and a selector. This crossbar implementation can be used, e.g., for OR (Sec. IIID), XOR function (Sec. IIIE) or any generic logic function.

TABLE V

IMPLEMENTATION OF OR GATE IN A CROSSBAR ARRAY WITH 5 PULSES AND 6 SWITCHES. FOR EACH CLOCK PULSE THE TABLE SHOWS THE CONNECTED SWITCHES AND THE COMPUTED OPERATION.

Clock=0	1	2	3	4	5
P1 = 0*	P2 → P1			P1 · P6	
P2 = A					
P3 = 0*		P4 → P3	P3 · P6		
P4 = B					
P5 = 0*					P6 → P5
P6 = 1			P3 · P6	P1 · P6	

integration, since CMOS circuits would require a very large area to drive all switches. To reduce the circuit complexity, the circuit can be implemented in a crossbar architecture as shown in Fig. 11. Here, the cross-section of a portion of a 2-layer crossbar array is shown, including both switching elements and selectors. For the fundamental gates, namely AND and IMP, 2 switches from the top and bottom layers (e.g., P1 and P2, or P1 and P4) can be selected to carry out computation by applying a driving pulse. For more complex functions, such as OR and XOR, a suitable sequence of logic operations can be performed in multiple switches and multiple clock pulses. For instance, Tab. V reports the sequence of operations for an OR function, using 6 switches (e.g., P1 to P6 in Fig. 11) and 5 clock pulses. Here, NOT operations are performed at clock #1 and #, while NOT(B) is transferred from the top to the bottom layer at clock #3. AND and NOT operations are finally carried out at clock steps #4 and #5, respectively. Note that a crossbar implementation generally requires a higher number of switches and/or clock pulses, however the area for the periphery circuit to address the lines is minimized through this approach. Similar to OR, also the XOR function can be implemented in a crossbar array using 8 switches and 8 clock pulses. Circuit architectures and select/unselect schemes in the crossbar array are further addressed in the companion paper [22].

IV. CONCLUSIONS

We have demonstrated nonvolatile logic operation in RRAM through conditional switching in serially-connected devices. The RRAM state variable can be 0 (low-resistance set state) or 1 (high-resistance reset state). The state variable is used both as input or output of the logic operations. AND, IMP,

NOT and transfer can be achieved in a single clock pulse, while OR, XOR and all other operations (*e.g.*, NAND and NOR) are achieved in multiple computation steps. The new nonvolatile logic approach allows to suppress the static leakage power dissipation, while reducing the area consumption thanks to the scalable 2-terminal structure of the RRAM switch.

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