Time-to-Digital Converter card for multichannel time-resolved Single-Photon Counting applications

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ABSTRACT

We present a high performance Time-to-Digital Converter (TDC) card that provides 10 ps timing resolution and 20 ps (rms) timing precision with a programmable full-scale-range from 160 ns to 10 µs. Differential Non-Linearity (DNL) is better than 1.3% LSB (rms) and Integral Non-Linearity (INL) is 5 ps rms. Thanks to the low power consumption (400 mW) and the compact size (78 mm x 28 mm x 10 mm), this card is the building block for developing compact multichannel time-resolved instrumentation for Time-Correlated Single-Photon Counting (TCSPC). The TDC-card outputs the time measurement results together with the rates of START and STOP signals and the number of valid TDC conversions. These additional information are needed by many TCSPC-based applications, such as: Fluorescence Lifetime Imaging (FLIM), Time-of-Flight (TOF) ranging measurements, time-resolved Positron Emission Tomography (PET), single-molecule spectroscopy, Fluorescence Correlation Spectroscopy (FCS), Diffuse Optical Tomography (DOT), Optical Time-Domain Reflectometry (OTDR), quantum optics, etc.

Keywords: time-to-digital conversion (TDC), single-photon counting, photon timing, time-correlated single-photon counting (TCSPC).

1. INTRODUCTION

High precision time-interval measurements are required in many fields, therefore instruments able to accurately measure timings down to the picoseconds scale at an affordable cost find a broad market, both in scientific and industrial communities. In particular, the Time-Correlated Single Photon Counting (TCSPC) technique [1] is able to reconstruct fast, low-intensity, repetitive optical waveforms, through the detections of single photons of the optical signal and on the precise measurement of their arrival times; after many acquisitions of individual events, it is possible to reconstruct the waveform of the optical signal, down to few picoseconds with no need to employ electronics with hundreds of GHz bandwidth. Concerning single-photon detectors, Single-Photon Avalanche Diodes (SPAD) or photomultiplier tubes (PMT) are usually employed. Specific applications like Fluorescence Lifetime Imaging (FLIM) [2],[3], Förster Resonance Energy Transfer (FRET) [4] and Diffuse Optical Tomography (DOT) [5] make use of Time-Correlated Single Photon Counting (TCSPC) where multichannel systems are more and more required. In fact the increasing number of acquisition channels allows to reach high performance in applications such as Diffuse Optical Spectroscopy (DOS) [6] or time-resolved optical spectrometer [7].

In order to fulfill the demanding requirements, several array of single-photon avalanche diodes (SPADs) [8] with integrated time measurement circuitry have been developed. The best chip so far reported in literature can reach good detection performance but with poor timing performance [9],[9], or they can reach good timing performance, but with poor detection efficiency and high noise [11],[12]. The best performance can be achieved by using state-of-the-art TCSPC equipment, provided by Becker&Hickl GmbH boards [13] and by PicoQuant GmbH modules[14]. However such solutions are not compact and have high power consumption, so these issues severely limit the number of channels and the achievable count rate for each channel [15].

In this paper we present a high-performance, low-power, time-to-digital converter (TDC) card, able to measure up to 10 µs time intervals, with 21 ps rms precision, and less than 1.3% LSB rms differential non-linearity. These features make the TDC Card suitable for the development of multichannel time measurement systems.

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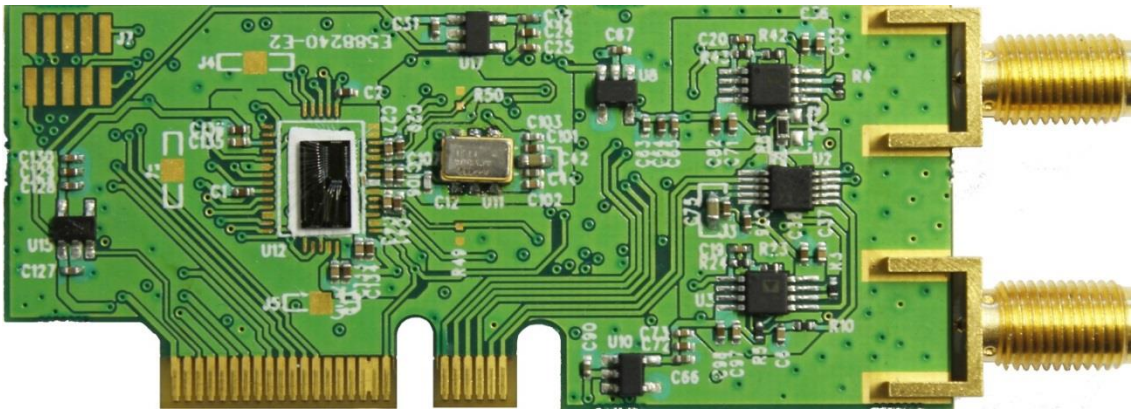

Figure 1. Photo of the Card, hosting the TDC chip, with the proper 100 MHz reference clock, the two input SMA connectors, the front-end circuitry, and the I/O edge card connector. Overall dimensions are 78 mm x 28 mm x 10 mm.

This paper is organized as follows. The architecture of the TDC Card is described in Section 2 an the experimental characterization is presented in Section 3. Finally, Section 4 draws the conclusions.

2. CARD ARCHITECTURE

The TDC Card, shown in Figure 1, measure the time interval defined by the START and STOP input signals, which can be provided by two SMA connectors or through two dedicated edge card connector pins. This edge card connector provides also the data result interface, the module configuration, and the power supply. The card form factor allow easily development of multichannel time measurement systems.

The core of the TDC Card is an application-specific integrated TDC circuit fabricated in a 0.35 µm CMOS technology [16], able to reach 10 ps resolution by means of two independent START/STOP channels for measuring the START/STOP arrival times in respect to an extremely stable and low jitter 100 MHz external reference clock. In order to reach the best performance in terms of single shot precision, measurement linearity, while keeping a low power consumption, the Card hosts an input signal front-end circuitry that performs signal conditioning while a Complex Programmable Logic Device (CPLD) manages the TDC chip, data acquisition, and calibration.

2.1 TDC Chip

The chip is composed of a counter and a two interpolators for the START and STOP signals: after the START event arrival the counter accumulates the number of the 100 MHz reference clock rising edge until the STOP event define the end of the time interval, with a 160 ns full scale range. In order to reach 10 ps resolution the two identical interpolators resolve the occurrences within the reference clock period and the START and STOP arrival time. Since the reference clock is uncorrelated to the START and STOP signal this topology implements the sliding-scale technique, assuring high performance in terms of measurement linearity. The occurrence within an input signal and the reference clock is resolved by means of a two stage interpolator circuit in order to reach the 10 ps resolution and good linearity, limiting the conversion time and keeping a low power consumption.

The TDC operation principle is shown in Figure 2: the counter provides the number $T_{counter}$ of clock rising edges between START and STOP events. Then the two interpolator improve the time resolution resolving the occurrences T_{START} and T_{STOP} between the reference clock period and the START and STOP signals respectively.

The measured time interval T is thus given by:

$$T = T_{counter} + T_{START} - T_{STOP} \quad (1).$$

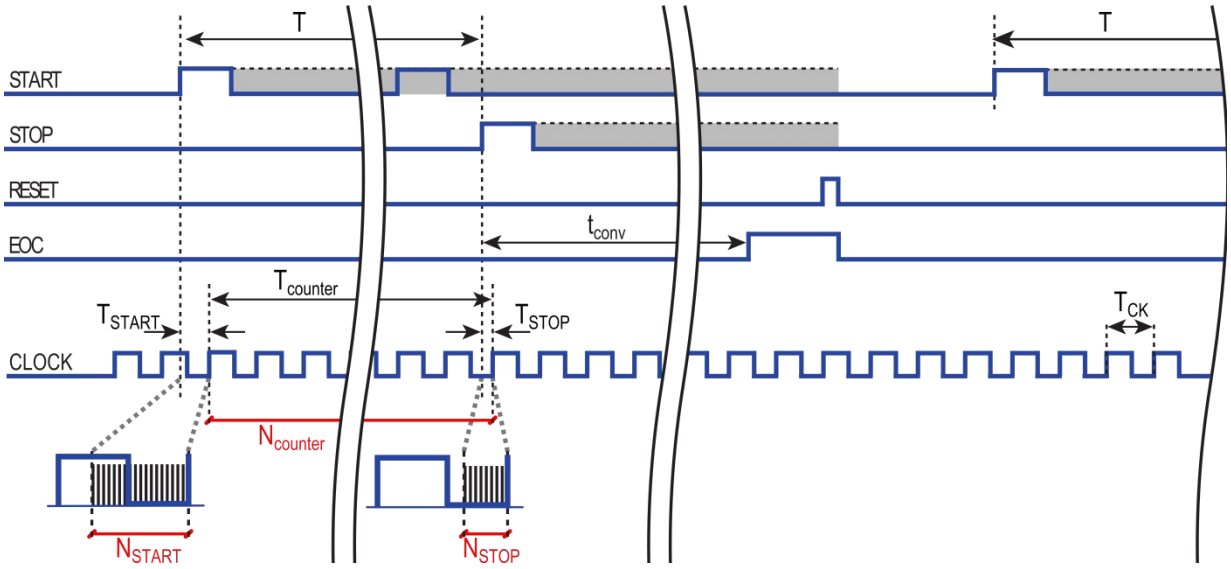

Figure 2. Operating principle of the TDC chip: a counter counts the number of reference clock's rising edges between START and STOP while the two-stages interpolators resolve the event occurrence within the clock period reaching 10 ps resolution.

2.2 Signal-Conditioning Electronics

The front-end signal-conditioning electronics is needed in order to guarantee compatibility with any kind of signal levels, like CMOS, TTL, ECL, NIM, and even non-standard signals, either positive or negative edge-triggered. As shown in Figure 3, the front-end is based on fast comparators (LT1711 by Linear Technology), powered at ±3.3 V, where the positive input is fed by the SMA while the negative one is connected to a Digital-to-Amplitude Converter (DAC) circuit able to generate the input threshold from -2.5 V to 2.5 V in 2.44 mV steps. Then a non-volatile 40 logic elements CLPD (Altera MAX V family) is drive by the comparators output and also by two I/O edge-card connector pins. In this way the TDC chip START and STOP signals can be fed by the SMA connectors or by the edge-card connector.

The CPLD is programmed in order to select the proper input source and the proper synchronization edge that define the time interval to measure. Then contain also two flip-flop in order to guarantee to the TDC chip the arrival of a STOP event only alter the arrival of the START event, with the proper pulse width.

2.3 Control and Data Processing Electronics

The TDC chip results are the raw data of the counter and the two interpolator; thus a non-volatile 570 logic elements CPLD (Altera MAX V family) is used to perform chip management, data acquisition and calibration, and rates measurement.

The CPLD handles the TDC chip readout by means of a state machine able to read the counter and interpolators results after an End-Of-Conversion (EOC) signal and then reset the TDC in order to enable the chip for a new conversion. Then the CPLD implements the data conversion using a 5 stage pipeline structure performing Eq. 1 and applying the necessary interpolator calibration coefficients. A range extension circuitry allows to measure time interval up to 10 µs without performance degradation. When the conversion result is ready, the time measurement data are provided on the I/O edge-card connector using, in according to the CPLD firmware, a parallel or a serial interface.

The CPLD implements also four counters in order to measure the rate of START, STOP, Valid START and Valid Conversion, since these information are very useful in most applications, in particular the ones based on TCSPC technique.

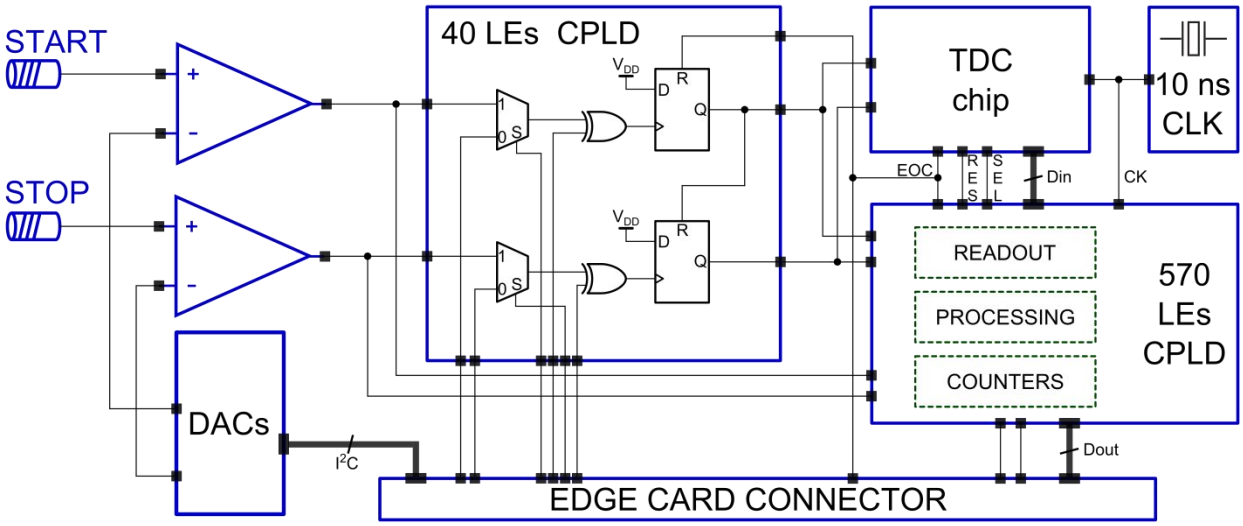

Figure 3. Block diagram of the TDC Card, based on the TDC chip. The 100 MHz reference clock is provided by a crystal oscillator and a phase-locked loop (PLL) circuit. The START and STOP input pulses are signal-conditioned before being fed to the chip by means of an input comparator with adjustable threshold an a small CPLD. The second CPLD performs the data readout and the data processing.

2.4 Power Supply

All necessary power supplies are feed by the edge-card connector, and they are: ±3.6 V for the first signal-conditioning stage with the input comparators and for the threshold generation; +3.5 V for the TDC chip and the CMOS interface; +2 V for the data processing. These voltages feed LDO (Low DropOut) regulators, which provide standard ±3.3 V and 1.8V voltages and keeping them separate to the different parts of the module, guaranteeing minimum mutual interference and low jitter performance degradation.

The Card consumes less than 0.4 W, and the on-board LDO regulators allows to design multichannel systems based on switching regulators guaranteeing an high power conversion efficiency without deteriorate the time measurement performance.

3. EXPERIMENTAL CHARACTERIZATION

The main figures of merit for a time measurement system are timing precision (also called single-shot precision in TCSPC instrumentation), timing accuracy, non-linearity, maximum conversion rate and power consumption.

The Card is able to perform time measurement with a conversion rate up to 3 Mconversion/s, limited by the TDC chip conversion time, while the overall consumption ranges from 350 mW and 400 mW respectively when there are no conversions and when the Card run at the maximum conversion rate.

The timing precision represents the uncertainty in the conversion of a given time interval. This parameter is evaluated measured a constant START-STOP delay a large amount of times and the distribution of the conversion results reflect the measurement uncertainty: the timing precision is the distribution standard deviation. The TDC Card timing precision is measured sweeping the START-STOP delay along the overall full scale range of 10 μs (with 1.5 ns step) reaching about 21 ps rms, as showed in Figure 4.

The timing accuracy represents the ability to measure the exact time interval between START and STOP signals. Actually the absolute time interval is not require, so the accuracy is defined as the ability to exactly measure the time difference between START-STOP couples. Starting from a reference 10 ns pulse generator, START-STOP couple with a

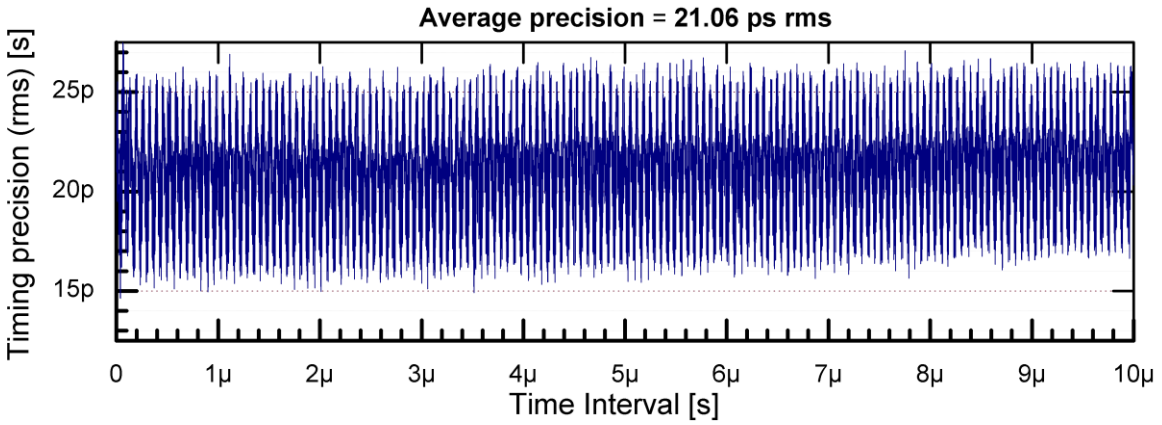

Figure 4. . Timing precision of the TDC Card, expressed as rms value of the distribution of measurement results around the mean value of a constant time-interval, swept across a 10 µs full scale range with 1.5 ns steps.

time interval duration of a random multiple of the reference 10 ns were provided to the TDC Card a 100 ppm accuracy was found. Also changing the input repetition rate the timing precision remains the same and the measurement peak position vary less than a LSB.

The non-linearity shows the bin value variation in respect to the nominal bin value and there are Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). We measured the TDC Card linearity by means of a code density test: a periodic STOP signal and an uniformly distributed random START signal (e.g., a single photon detector dark count) define randomly variable time intervals to be measured. The resulting histogram reflects the Card non-linearity, with a DNL of 1.25 % LSB rms (9.5 % LSB peak) and with a INL of 5 ps in a 320 ns full scale range. In particular the DNL is higher in the first 50 ns measurement range due to crosstalk in the signal conditioning front end while then reach the DNL performance of the TDC chip alone: 0.9 % LSB rms.

4. CONCLUSIONS

We presented a TDC Card able to measure time interval up to 10 µs with 10 ps resolution, 21 ps rms precision, 100 ppm accuracy, 1.25% LSB rms DNL with less than 0.4 W power consumption and up to 3 Mconversion/s conversion rate.

The Card, thanks to the high performance, low-cost, low-power consumption and very compact implementation, open the way to an easily development of multichannel timing instrumentation for TCSPC-based measurements where very many-channels working in parallel are needed.

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