High linearity SPAD and TDC array for TCSPC and 3D ranging applications

Federica Villa[a], Rudi Lussana[a], Danilo Bronzi[a], Alberto Dalla Mora[b], Davide Contini[b], Simone Tisa[c], Alberto Tosi[a], Franco Zappa[a]

[a]Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria Piazza Leonardo da Vinci 32, I-20133 Milano, Italy;
[b]Politecnico di Milano, Dipartimento di Fisica, Piazza Leonardo da Vinci 32, I-20133 Milano, Italy;
[c]Micro Photon Device S.r.l., Via Stradivari 4, 39100, Bolzano, Italy

ABSTRACT

An array of 32x32 Single-Photon Avalanche-Diodes (SPADs) and Time-to-Digital Converters (TDCs) has been fabricated in a 0.35 µm automotive-certified CMOS technology. The overall dimension of the chip is 9x9 mm^2. Each pixel is able to detect photons in the 300 nm – 900 nm wavelength range with a fill-factor of 3.14% and either to count them or to time stamp their arrival time. In photon-counting mode an in-pixel 6-bit counter provides photon-number-resolved intensity movies at 100 kfps, whereas in photon-timing mode the 10-bit in-pixel TDC provides time-resolved maps (Time-Correlated Single-Photon Counting measurements) or 3D depth-resolved (through direct time-of-flight technique) images and movies, with 312 ps resolution. The photodetector is a 30 µm diameter SPAD with low Dark Count Rate (120 cps at room temperature, 3% hot-pixels) and 55% peak Photon Detection Efficiency (PDE) at 450 nm. The TDC has a 6-bit counter and a 4-bit fine interpolator, based on a Delay Locked Loop (DLL) line, which makes the TDC insensitive to process, voltage, and temperature drifts. The implemented sliding-scale technique improves linearity, giving 2% LSB DNL and 10% LSB INL. The single-shot precision is 260 ps rms, comprising SPAD, TDC and driving board jitter. Both optical and electrical crosstalk among SPADs and TDCs are negligible. 2D fast movies and 3D reconstructions with centimeter resolution are reported.

Keywords: Single-photon avalanche diode (SPAD), photon counting, 2D Imaging, 3D Ranging, Time-of-Flight, Time-to-Digital Converter.

1. INTRODUCTION

Single-photon time-resolved measurements of very faint and fast optical signals are nowadays particularly important in safety and security, medical and biological applications, spectroscopy, and 3D ranging. There is an increasing demand for compact, multi-channel, time-resolved instruments. Sub-nanosecond timing resolutions are required in Time-of-Flight (TOF) based Positron Emission Tomography (PET) scanners [1], in 3D depth ranging and LIDAR (Light Detection And Ranging) [2], and in Time-Correlated Single-Photon Counting (TCSPC) [3], to accurately reconstruct the waveforms of fast and faint optical signals through repetitive excitation of the sample under investigation. Furthermore, demanding TCSPC applications require extremely good precision and Differential Non-Linearity (DNL) much better than ½ LSB (Least-Significant Bit) of the timing resolution. All these applications could benefit from single-photon sensitivity and and precise timing circuit that both can be provided by SPAD-based photodetector arrays.

This paper reports a single-chip imager, fabricated in a 0.35 µm automotive certified CMOS technology, consistong of 32 x 32 pixels, each containing a SPAD (Single-Photon Avalanche Diode) detector and a Time-to-Digital Converter (TDC) [4]. It can be used in counting-mode (for counting the number of detected photons) providing photon-number resolved 2D movies, or in timing-mode (for measuring the arrival time of the first photon in each pixel with 312 ps resolution) for acquiring sub-nanosecond optical waveforms and time-resolved maps.

A camera based on this chip, able to provide 2D and 3D images and movies has been developed. It is made of 3 boards: the first one provides the power supplies to the other boards and to the chip, the second one is a commercial board with

Quantum Sensing and Nanophotonic Devices XII, edited by Manijeh Razeghi, Eric Tournié, Gail J. Brown,
Proc. of SPIE Vol. 9370, 93701U · © 2015 SPIE · CCC code: 0277-786X/15/$18 · doi: 10.1117/12.2077847

FPGA (Xilinx Spartan-6) and DDR2 memory (128 MB), the third one includes the chip and all the connections with the FPGA and the external signals.

2. CMOS SPAD

SPAD is essentially a p-n junction biased above the breakdown voltage (V_{BD}), which requires avalanche quenching and recharge mechanisms [5]. When a photon triggers an avalanche multiplication process within the SPAD junction, the quenching circuitry stops the avalanche, preventing too high a current flow and power dissipation, and keeps the SPAD quenched for a fixed hold-off time ($T_{hold\text{-}off}$) in order to release trapped charges, thus avoiding the triggering of spurious (the so-called afterpulsing) avalanches. Finally, the recharge circuitry brings the SPAD back to operation for the next detection cycle, by raising the bias voltage again above breakdown [6]. SPAD models have been developed to simulate the electrical behavior of electronics [7].

The exploitation of a custom technology gives the opportunity to tailor dopants concentration and diffusions widths to optimize SPAD performance. On the other hand very scaled CMOS technologies make it possible to develop very dense arrays of SPADs with in-pixel pre-processing electronics [9]-[11].

The SPAD array here described was designed in a 0.35 μm high-voltage technology with high level of cleanness and controlled substrate to reduce the number of defects that could deteriorate SPAD performance. Such not-scaled technology node is a good compromise to achieve not only large arrays of smart pixels but also high performing SPADs.

The cross-section of a SPAD is represented in Figure 1: the p+ diffusion and the n-enrichment define the active absorption and avalanche region, the p-guard ring avoids premature edge breakdown. Many SPADs with different size have been preliminary produced and their characterization in terms of Dark Count Rate (DCR), Photon Detection Efficiency (PDE) and timing jitter is reported in [12]. The SPAD with 30 μm active area diameter has been selected to be integrated in the present array, since it is a good compromise of overall performance (50 cps DCR at room temperature, 50% PDE, 76 ps FWHM timing jitter, low afterpulsing, at 5 V excess bias) and size. The DCR *vs.* PDE plot at different excess bias and wavelength is shown in Figure 2 left. The DCR has been measured when all the 1024 SPADs were working in parallel without cooling the array (and so the temperature of the chip was higher than room temperature). Figure 2 right represents the inversecumulative distribution function of the array DCR. Less than 5% of the pixels can be defined "hot-pixels" (i.e. pixels with DCR considerably higher than the median of the other pixels).

An integrated quenching and active reset circuit is connected to the SPAD's anode, because the latter shows lower parasitic capacitance compared to cathode, thus resulting in faster avalanche quenching and lower timing jitter [13].

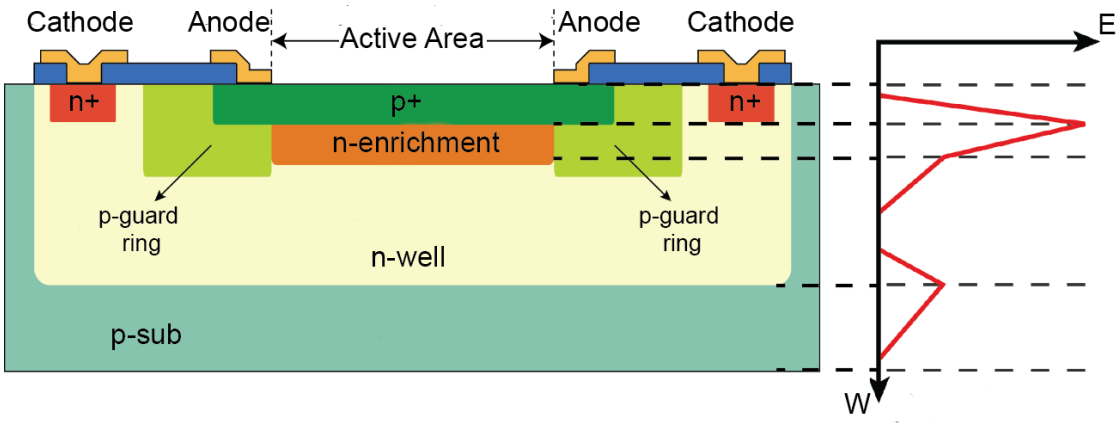

Figure 1 Cross-section of the SPAD developed in 0.35 μm high-voltage CMOS technology and simplified electric field along the center of the device. The p+ and n-enrichment diffusions define the absorption and avalanche region.

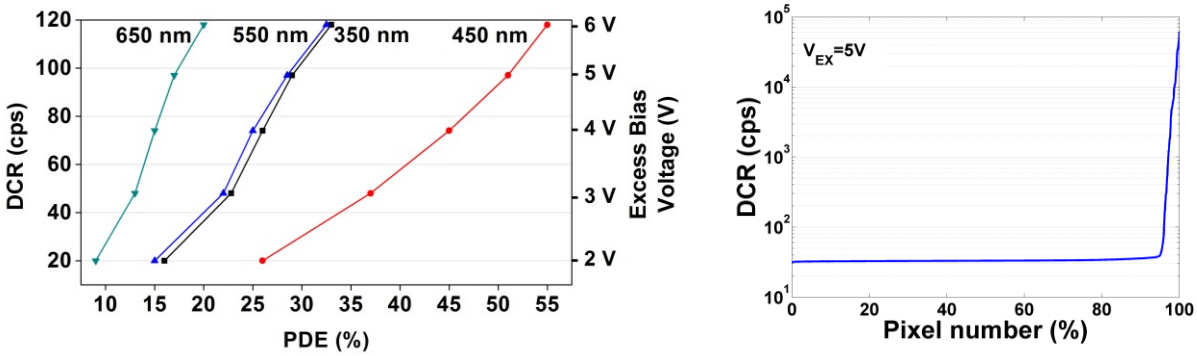

Figure 2 Left: Dark Count Rate *vs*. Photon Detection Efficiency of the CMOS SPADs of the reported imager, at four different wavelengths and five excess biases (2 V, 3 V, 4 V, 5 V, and 6 V). Right: Cumulative distribution function of DCR among array pixels.

3. STRUCTURE OF THE ARRAY AND TIMING ELECTRONICS

The imager is constituted by 32 × 32 pixels (each comprising the SPAD, the timing and counting electronics, internal memory and output buffers), global timing electronics (Delay Locked Loop DLL, STOP interpolator and synchronizer) and readout circuitry (row selector and output multiplexer). The minimum frame duration required for reading out the whole 32 × 32 array is 10 µs, corresponding to 100,000 fps maximum frame rate.

The 0.35 µm CMOS technology prevents to shrink the in-pixel electronics (pixel size is 150 µm × 150 µm), thus limiting the attainable fill-factor to 3.14% (with no micro lens array), but at the same time it allows to exploit large 30 µm SPADs with DCR of just 120 cps (counts/s) without cooling the array. Such large SPADs mitigate the fill-factor reduction, which eventually is even better than what reported in other more scaled technology, e.g. 1% [10], or 2.3% [14] in 130 nm technology.

In each pixel, when a photon triggers the SPAD, the avalanche sensing electronics provides a START signal to the in-pixel TDC. The global STOP is provided to all TDCs by an external synchronization signal (e.g. the excitation laser sync-out signal). The structure of the pixel is very similar to the one described in [15], in which just a single pixel is reported. The TDC is made of two stages: a 6-bit counter that counts the number of reference clock periods between the START and STOP signal, and a 4-bit interpolator that latches the phase of the START in respect to 16 shifted replicas of the reference clock generated by the global DLL. Another global 4-bit interpolator is used to latch the phase of the STOP, which is asynchronous in respect to the reference clock in order to implement the sliding scale technique for improving linearity [16]. By changing the period of the reference clock, it is possible to modify the resolution (i.e. Least Significant Bit, LSB) of the TDC and thus the full-scale range (FSR). The maximum clock frequency is 200 MHz, which corresponds to 312 ps resolution and 320 ns FSR, the minimum is 50 MHz, i.e. 1.25 ns resolution and 1.28 µs FSR.

A detailed description and characterization of the timing electronics is reported in [4]. At the maximum reference clock frequency (200 MHz) the single shot precision is 254 ps rms (with a variance of 27.8 ps among different pixels), the linearity is the best ever reported for an array of SPADs and TDCs, with 2% LSB Differential-Non-Linearity (DNL) and 10% LSB Integral-Non-Linearity (INL). The optical and electrical crosstalk between pixels is negligible, and the accuracy is better than one LSB across the entire array.

In counting mode, the same 6-bit counter of the TDC is used to count the number of absorbed photons in each frame, whose minimum duration is 10 µs.

The total power consumption in photon-counting mode is less than 70 mW, whereas in photon timing it depends on the timing resolution and on the number of gate-on windows per frame. Table I shows the power consumption for each array block in photon-timing mode, at two different timing resolutions depending on the external reference clock.

Table I: Power consumption of the imager main blocks in photon timing mode for DLL clock frequencies of 160 MHz (i.e. LSB = 390 ps) and 200 MHz (i.e. LSB = 312 ps).

Circuit block	Notes	Power consumption		Units
		LSB = 390 ps	LSB = 312 ps	
DLL		260	315	mW
In-pixel electronics	1 conversion per frame	40		mW
Clock distribution	1 gate per frame	33	50	mW
Digital I/O	at 100,000 fps	20		mW
Analog I/O		< 5		mW
TOTAL		358	430	mW

4. 2D FAST MOVIES

The SPAD array can operate in photon counting mode, when 2D intensity map of the scene must be acquired. The camera reaches high frame rates (up to 100 kfps) in burst acquisition, when the data are stored inside the local memory integrated in the same board of the FPGA, or 15 kfps in continuous acquisition, limited by the data transfer from the FPGA to the computer through an USB 2.0 link. This bottleneck will be overcome in the future using an USB 3.0 connection. Thanks to the high frame rate, it is possible to acquire very fast phenomena that cannot be recorded with traditional CCD cameras. As an example, Figure 3 shows eight frames from a 2D movie acquired at 50,000 fps of an optical chopper rotating at 39,000 revolutions per second. Note that is also visible the flickering at 100 Hz of the neon lamp that illuminated the scene.

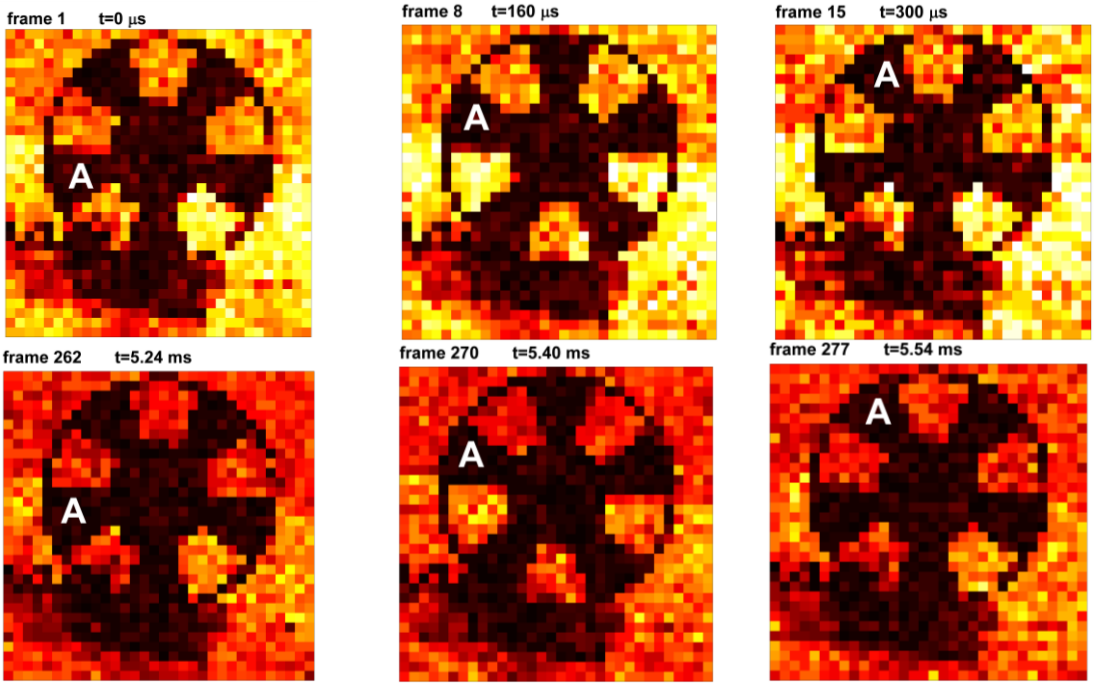

Figure 3 Six frames from a 2D movie acquired at 50,000 fps of an optical chopper rotating at 39,000 revolutions per seconds, illuminated by a neon lamp flickering at 100 Hz.

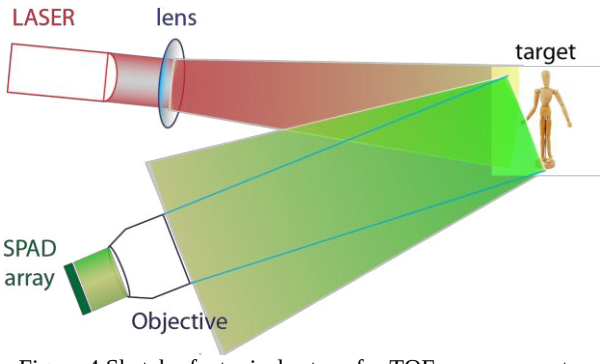

Figure 4 Sketch of a typical set-up for TOF measurements.

Such high frame rate in counting mode can be also exploited in molecular application, for instance in Fluorescence Correlation Spectroscopy (FCS) [17] or in Diffuse Correlation Spectroscopy (DCS) [18] in order to reduce the minimum correlation interval that can be measured.

5. 3D RANGING MEASUREMENTS

In TOF applications the round trip of a laser pulse is measured, thus active illumination is necessary. The START signal is given by the SPAD output, whereas the STOP is given by the laser synchronization signal. A typical non-confocal set-up for 3D measurements is sketched in Figure 4. In the actual set-up the laser and the objective were very close each other so the emitted and the back-scattered light are almost parallel. The used illuminator is a 750 nm pulsed laser (90 mW average emitted optical power) and an objective with adjustable (50 mm - 250 mm) focal length and f/4.8 aperture was placed in front of the camera. Figure 5 represents a 3D reconstruction of human targets at 8 m distance from the camera (left) and 5 m (right), acquired in 5 ms. Each pixel acquired on average about 3,000 photons, so depth-information is measured with a precision given by:

$$\sigma_N = \frac{\sigma_1}{\sqrt{N}} \tag{1}$$

where the overall precision σ_N of 0.7 mm (i.e. 4.6 ps rms), is achieved after N=3,000 valid events, with the previously reported single-shot precision σ_1 of 254 ps rms.

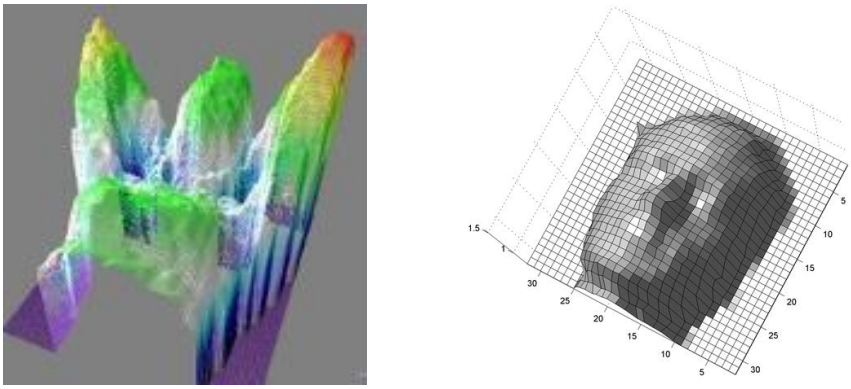
Figure 5 3D reconstruction of a human target at 8 m (left) and 5 m (right) distance from the camera, acquired in 5 ms.

6. CONCLUSIONS

Arrays of SPADs and TDCs have been already reported in literature [10],[14],[19]-[21]. They integrate SPADs with diameters smaller than 10 μm and high DCR. High fill-factors (> 10%) have been achieved with multiplexed architectures, in which many SPADs share one TDC. Typical resolutions of the reported TDCs are in the order of tens of picoseconds, but the DNL and INL are higher than 30% LSB and 120% LSB, respectively.

Here we reported on an array that integrates a high-performance large-area SPAD with a high-linearity (DNL = 2% LSB, INL = 10% LSB) TDC in each pixel. This array can acquire 2D fast movies at high frame rate up to 100,000 fps, and 3D images with centimeter resolution. Furthermore, it can be exploited in molecular imaging for experiments based on correlation spectroscopy exploiting the counting capability within short frames, or in TCSPC applications thanks to the sub-nanosecond resolution and high linearity of the TDCs.

REFERENCES

[1] Daube-Witherspoon, M. E., Matej, S., Werner, M.E., Surti, S., Karp, J.S., "Comparison of list-mode and DIRECT approaches for time-of-flight PET reconstruction," IEEE Nucl. Science Symp. Conf. Record, 2252-2258 (2010).

[2] McCarthy, A., Ren, X., Della Frera, A., Gemmell, N. R., Krichel, N. J., Scarcella, C., Ruggeri, A., Tosi, A., Buller, G. S., "Kilometer-range depth imaging at 1550 nm wavelength using an InGaAs/InP single-photon avalanche diode detector," Opt. Express 21(19), 22098-22113 (2013).

[3] Becker, W., "Advanced Time-Correlated Single Photon Counting Techniques," Springer, Berlin (2005).

[4] Villa, F., Lussana, R., Bronzi, D., Tisa, S., Tosi, A., Zappa, F., Dalla Mora, A., Contini, D., Durini, D., Weyers, S., Brockherde, W., "CMOS Imager With 1024 SPADs and TDCs for Single-Photon Timing and 3-D Time-of-Flight," Selected Topics in Quantum Electronics IEEE Journal of, 20 (6), 1-10, (2014).

[5] Zappa, F., Tisa, S., Tosi, A., Cova, S., "Principles and features of single-photon avalanche diode arrays," Sensors Actuators A Phys. 140(1), 103–112 (2007).

[6] Tisa, S., Zappa, F., Tosi, A., Cova, S., "Electronics for single photon avalanche diode arrays," Sensors and Actuators A: Physical, vol. 140 (1), 113-122 (2007).

[7] Zappa, F., Tosi, A., Dalla Mora, A., Tisa, S., "SPICE modeling of single photon avalanche diodes," Sensors and Actuators A: Physical, 153 (1), 197-204 (2009).

[8] Gulinatti, A., Rech, I., Panzeri, F., Cammi, C., Maccagnani, P., Ghioni, M., Cova, S., "New silicon SPAD technology for enhanced red-sensitivity, high-resolution timing and system integration," Journal of Modern Optics, 59 (17), 1489-1499 (2012).

[9] Guerrieri, F., Tisa, S., Tosi, A., Zappa, F., "Single-Photon Camera for high-sensitivity high-speed applications," Photonic Journal IEEE, 2 (5), 759-774 (2010).

[10] Veerappan, C., Richardson, J., Walker, R., Li, D., Fishburn, M.W., et al. "A 160×128 Single-Photon Image Sensor with On-Pixel 55ps 10b Time-to-Digital Converter," IEEE Int. Solid-State Circuits Conf. (2011).

[11] Bronzi, D., Villa, F, Tisa, S., Tosi, A., Zappa, F., Durini, D., Weyers, S., Brockherde, W., "100 000 Frames/s 64 × 32 Single-Photon Detector Array for 2-D Imaging and 3-D Ranging," Selected Topics in Quantum Electronics IEEE Journal of , 20 (6), 1-10 (2014).

[12] Villa, F., Bronzi, D., Zou, Y., Scarcella, C., Boso, G., Tisa, S., Tosi, A., Zappa, F., Durini, D., et al., "CMOS SPADs with up to 500 μm diameter and 55% detection efficiency at 420 nm," J. Mod. Opt. 61(2), 102–115 (2014).

[13] Bronzi, D., Tisa, S., Villa, F., Bellisai, S., Tosi, A.., Zappa, F., "Fast Sensing and Quenching of CMOS SPADs for Minimal Afterpulsing Effects," IEEE Photonics Technol. Lett. 25(8), 776–779 (2013).

[14] M. Gersbach, Y. Maruyama, E. Labonne, J. Richardson, R. Walker, et al., "A parallel 32×32 time-to-digital converter array fabricated in a 130 nm imaging CMOS technology," ESSCIRC 2009 - Proceedings of the 35th European Solid-State Circuits Conference, 196-199 (2009).

[15] Villa, F. A., Markovic, B., Bellisai, S., Bronzi, D., Tosi, A., Zappa, F., Tisa, S., Durini, D., Weyers, S., et al., "SPAD Smart Pixel for Time-of-Flight and Time-Correlated Single-Photon Counting Measurements," IEEE Photonics J. 4(3), 795–804 (2012).

[16] Markovic, B., Tisa, S., Villa, F.A., Tosi, A. and Zappa, F., "A high-linearity, 17 ps precision time-to-digital converter based on a single-stage delay Vernier loop fine interpolation" IEEE TCAS- I, 60 (3), 557-569 (2013).

[17] Michalet, X., Colyer, R. A., Scalia, G., Ingargiola, A., Lin, R., et al., "Development of new photon-counting detectors for single-molecule fluorescence microscopy," Philosophical Transaction B, 368 (1611), 1-22, (2012).
[18] Durduran, T., Choe, R., Baker, W. B., & Yodh, A. G., "Diffuse optics for tissue monitoring and tomography," Reports on Progress in Physics, 73(7), 076701 (2010).
[19] Niclass, C., Favi, C., Kluter, T., Gersbach, M., Charbon, E., "A 128x128 Single-Photon Imager with on-Chip Column-Level 97ps 10bit Time-to- Digital-Converter Array," IEEE International Solid-State Circuits Conference (ISSCC), (2008).
[20] Niclass, C., Soga, M., Matsubara, H., Kato, S., Kagami, M., "A 100-m Range 10-Frame/s 340 x 96-Pixel Time-of-Flight Depth Sensor in 0.18 µm CMOS," IEEE Journal of Solid-State Circuits, 48 (2), 559-572 (2013).
[21] Richardson, J., Walker, R., Grant, L., Stoppa, D., Borghetti, F., Charbon, E., et a., "A 32×32 50ps resolution 10 bit time to digital converter array in 130nm CMOS for time correlated imaging," Custom Integrated Circuits Conference, 2009. CICC '09. IEEE, 77-80 (2009).