An Open-hardware Platform for MPSoC Thermal Modeling

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Abstract. Current integrated circuits exhibit an impressive and increasing component density, hence an alarming *power* density. Future devices will require breakthroughs in hardware power dissipation strategies and software active thermal management to operate reliably and maximise performance. In this *scenario*, thermal modelling plays a key role in the design of next generation cooling and thermal management solutions. However, extending existing thermal models, or designing new ones to account for new cooling solutions, requires parameter identification as well as a validation phase to ensure correctness of the results. In this paper, we propose a flexible solution to the validation issue, in the form of a hardware platform based on a Thermal Test Chip (TTC). The proposed platform allows to test a heat dissipation solution under realistic conditions, including fast spatial and temporal power gradients as well as hot spots, while collecting a temperature map of the active silicon layer. The combined power/temperature map is the key input to validate a thermal model, in both the steady state and transient case. This paper presents the current development of the platform, and provides a first validation dataset for the case of a commercial heat sink.

Keywords: MPSoC · Thermal Modeling · Dark silicon.

1 Introduction

In the history of thermal management for multi/many-core CPUs/GPUs and MPSoCs, two "revolutions" can be observed. The first one dates back to the release of the Pentium, and consisted in the need for a heat sink and a fan. The second one, corresponding to the introduction of computational sprinting techniques like the Intel Turbo Boost, consisted in thermal management becoming vital for the operation itself of a chip.

Before the first revolution, in fact, CPUs just resembled more ordinary integrated circuits. After, their packaging and installation had to be specifically designed to take thermal dissipation into account. Before the second revolution, with reasonable dissipation conditions, CPUs could operate at their maximum performance state indefinitely. After, they had become so power-dense to not allow such an operation anymore, at least with market-affordable dissipation

systems, and thus to require a mechanism that permits maximum power only within a certain thermal budget.

As such, modern chips require dynamic thermal management, as not reacting promptly enough to highly variable and hardly predictable power bursts would cause unacceptable reliability issues, or even thermal runaway. And looking at the future, high-performance CPUs and MPSoCs – for consumer, datacenter, supercomputing and exascale applications – strongly need improvements in cooling solutions and thermal management, as such improvements could immediately entail increases in performance and profitability.

The importance of thermal modeling in the development of next generation solutions to the thermal wall issue cannot be overstated. Fast, accurate, steady state and transient thermal models are needed to cost-effectively explore the design space of thermal management and cooling solutions. Doing so however requires thermal models with a significant degree of flexibility, such as the ability to quickly and accurately introduce models for evaporative cooling, peltier cooling, liquid cooling, as well as a library of off-the-shelf heatisinks. All those models would also need to accurately support transient simulations for them to be useful in the development of dynamic thermal management policies.

Existing thermal models would thus need significant extensions and redesign to reach the level of flexibility required for future integrated circuits thermal design space exploration. Improvement of existing thermal models as well as the design of new ones is however hindered by one major issue: the difficulty of validating them.

Thermal models are either obtained from first priciple equations describing the thermal phenomenon or through empirical correlations when detailed modeling would be too compute intensive. Thermal conduction in solids is an example where first principle modeling is employed, while natural and forced convection in fluids is an example where empirical correlations are commonplace. In both cases, a thermal model critically depends upon a number of parameters, such as material properties, geometric dimensions and empirical coefficients. A precise identification and validation of such parameters requires experiments. Since the main purpose of an MPSoC thermal model is the faithful reproduction of an integrated circuit temperature map under operating conditions, the main experiment requirement is to subject an integrated circuit not just to a known power, but also a known power spatial distribution across the silicon die, and to be able to measure a temperature map of the active silicon layer. Such requirements are incompatible with ordinary MPSoCs, due to the uncertainty in the power distributions as well as the general lack of temperature sensors, and instead call for custom hardware dedicated to thermal model validation.

In this paper we present a validation platform for MPSoC thermal models conceived to fulfill the needs just evidenced. This platform is based on a Thermal Test Chip (TTC), an integrated circuit containing an array of power dissipating elements and an array of temperature sensors. Our thermal validation platform is capable of applying a generic power dissipation pattern to the thermal test chip, both constant for steady state experiments, or time varying for transient

experiments, and measuring the corresponding temperature map, at a rate up to 1kHz. This capability allows to measure the temperature map of an integrated circuit subject to reference power dissipation maps, and identify parameters in thermal models.

A first dataset is provided with this paper, consisting in the result of thermal experiments performed on a commercial heat sink. Plans are to offer the community a variety of data sets, so as to allow validating models under heterogeneous operating conditions, possibly also off-design. Although the presented platform is complete, we are currently developing support tools to interface to the platform from a PC and integrate it in MPSoC simulation tools to support hardware-in-the-loop simulations, as well as finalizing the documentation. When this is done, we plan to release the design files of the platform as open hardware together with the microcontrollers firmware and support tools, to allow researchers to build their own apparatus.

2 Related work

Numerous thermal simulators specifically designed for CPUs/MPSoCs were proposed in the literature. Among the most successful ones are HotSpot [4] and 3D-ICE [10], on which we mainly concentrate here. HotSpot supports the simulation of both 2D and 3D integrated circuits, can simulate thermal dissipation through a simple model for an heat sink, air flow and fan, as well as a secondary heat transfer path through the printed-circuit board. 3D-ICE supports 2D and 3D integrated circuits as well, but in addition it can simulate heat dissipation through liquid flow in microchannels etched in the silicon and passively cooled embedded MPSoCs [6]. Although both simulators have been validated, extending them to support other cooling solutions in order to explore different heat dissipation solutions, or just to keep up with the diversity of modern technologies, e.g. the ubiquitous heat pipes used in laptop computers, would require additional validation. Other simulators exist, such as Therminator [18] – targeted to smartphone thermal simulation but limited to steady state only – and a Modelica thermal simulator integrated in a MPSoC simulation workflow [14].

As can be seen, the range of heat dissipation solutions that can be represented by state-of-the-art thermal simulators is somewhat limited, and those simulators are inflexible in nature, tightly coupled with a few cooling solutions, and not easy to extend. We argue that one of the main reasons that prevented more generic thermal simulators lies in the corresponding validation and parameter identification difficulty.

Validation and parameter identification of a thermal model can be performed in a number of ways. A first possibility would be to take an off-the-shelf processor, connect it to the desired thermal dissipation solution, run benchmarks that cause well-defined power dissipation patterns, and measure the chip temperature with its internal temperature sensors. This solution has unfortunately a large number of drawbacks and stopgaps that make it impractical. First of all, although the total power being fed to a chip can be measured, there is no easy

way to measure the power *spatial distribution* across the silicon die. Then, relevant information such as the chip floorplan and the placement of temperature sensors, is known only by the manufacturer, and this makes parameter identification extremely difficult. Finally, although high accuracy on-chip temperature sensors can be made [3], those commonly found in off-the-shelf processors are often low-resolution, affected by significant noise, and few in number.

Another validation solution could be to decap an off-the-shelf MPSoC and collect a thermal map using a thermal camera [9, 1]. This solution allows to achieve high resolution thermal maps, but prevents the chip under test from being connected to an arbitrary heat dissipation solution, and the thermal maps obtained in this way can thus be significantly different than the ones in real-world operating conditions [5]. Moreover, this validating solution does not solve the issue of the lack of knowledge on the spatial distribution of power dissipation, as the obtained map is of temperature and not power.

Thermal test chips are integrated circuits containing a number of resistive heaters, to dissipate power in a controlled way, and a number of temperature sensors, to probe the active silicon temperature when connected to an arbitrary cooling solution. Such chips thus represent the perfect solution to thermal model parameter identification and validation. Thermal test chips are a however niche product, manufactured by a small number of companies [11, 16], and although available for a number of years, to date they have not seen widespread use in academia for thermal model validation. One of the reason for this fact is that thermal test chips are either sold as bare die requiring bonding, individual components, or with very basic breakout boards [17]. The time and effort required to design an entire thermal validation platform is thus a major stopgap.

This paper means to provide an answer to this important necessity; in detail, we present a general-purpose, flexible thermal validation platform as a "turnkey" solution to perform accurate and repeatable experiments on heat dissipation. We believe this to be a real step forward because to the best of our knowledge, no other such solution is to date available, not even as a commercial product.

3 The platform

The proposed thermal validation platform is built around a TTV-1202 [15] thermal test chip. The chip has a silicon die area of 10.23 x 10.23mm, mounted in a flip-chip configuration to a BGA substrate. The chip is organised as a 4 x 4 array of individual cells, each capable of temperature sensing and power generation through a resistive element. The heating element in each cell is capable of dissipating up to 12W, for a total chip power dissipation of 192W. However, the actual maximum power dissipation depends upon the cooling solution provided, as the chip temperature has an absolute maximum rating of 150°C.

An analysis of the requirements of thermal experiments has been performed, resulting for the validation platform in the following design requirements.

– It should be possible to produce arbitrary patterns of power dissipation across the TTC, thus requiring an array of voltage sources to drive the

resistive elements inside the TTC. This solution allows to test realistic spatial power dissipation patterns of CPUs and MPSoCs, as well as hot spots.
– The aforementioned array of voltage sources need to be software controllable, and adequate support software is needed to perform a "playback" of a given power waveform to each heating element, thus allowing to test realistic temporal power dissipation patterns that are produced as a result of code execution in CPUs and MPSoCs.
– A readback of the power value being applied to the chip is beneficial to compensate for physically generated inaccuracies, including e.g. power loss in the wires connecting the driving subsystem to the TTC.
– A temperature sensing periods as low as 1ms should be possible, to capture the fast thermal transients that occur in the active silicon layer [13].
– A temperature resolution of 0.1°C is beneficial to see the detail of thermal transients, and to capture accurate steady state thermal maps.

The proposed thermal test platform fulfils all those requirements; its hardware design and firmware is detailed in the following.

3.1 Hardware infrastructure

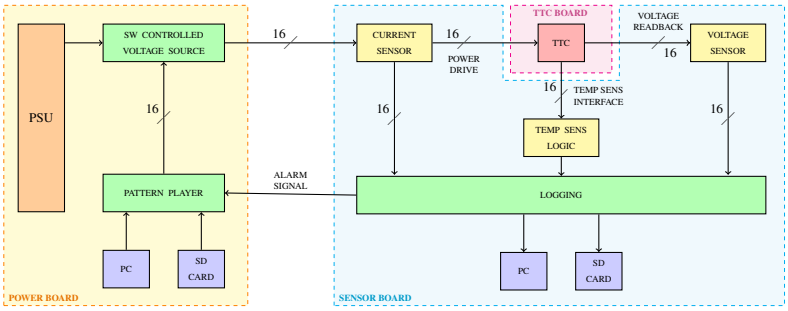

Fig. 1. Block diagram of the platform hardware.

Figure 1 shows a block diagram of the the hardware infrastructure. The hardware architecture is composed of three distinct boards: a carrier for the TTC, a sensing board for measurements and a driving board for the generation of power profiles.

The TTC carrier board is shown in figure 2. It holds the thermal test chip and provides support holes for the heat dissipation solutions to be tested. Two connectors on the bottom of the board allow electrical interconnection to the sensing board, which is designed to sit under the TTC carrier one. In fact, the main purpose of the TTC carrier board is to provide mechanical support. It was designed to not have any electrical component beside the TTC, to provide maximum flexibility in thermally connecting the TTC to different kind of heat

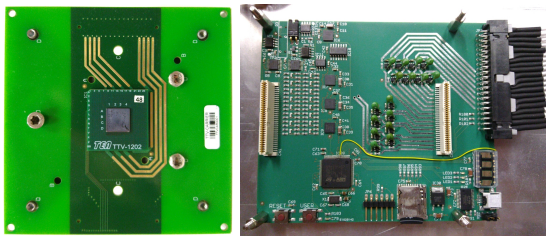

Fig. 2. The board hosting the thermal test chip (left) and sensor board (right).

dissipation solutions. A metal backing plate – of the type employed in PC motherboards underneath the CPU socket – is fixed at the bottom of the board to provide the required mechanical rigidity in case heavy heat sinks are used. Moreover, this backing plate provides binding posts for standard LGA 1150 PC heat sinking solutions.

The sensor board is shown in figure 2. This board holds the components required for sensing the thermal map of the TTC and for the power map readback.

The TTV1202 temperature sensing capability is based on silicon diodes, whose forward voltage when driven by a constant current source linearly depends on the junction temperature. Diodes in various cells are connected in a multiplexed 4 x 4 matrix arrangement matching the cell layout. Each row and column signal is duplicated allowing a four wire measurement arrangement. This arrangement eliminates measurement errors due to resistive losses and increases measurement linearity. Four 4-way analog multiplexers are used to switch the current source and ADC inputs to any of the 16 diodes, and a software driver cycles through all sensors approximately every 300us. The temperature reading resolution is 0.1°C.

In order to be able to know exactly the power being fed to each element, a voltage and current sensor are added to each of the 16 lines coming from the power board. Current sensors are implemented using 20mOhm current sense resistors, and high-side amplifiers. Voltage sensing is also performed using a 4 wire measurement approach, as in the TTV1202 the pins of the heating elements are duplicated as well. Voltage resolution is 6mV, current resolution 0.5mA. Voltage and current are measured at up to 1kHz.

An STM32 ARM Cortex M4 microcontroller completes this board, performing measurements, performing soft calibration, providing an overtemperature alarm to the power board and logging the measured data. For what concerns the latter, logging can either be performed to a PC through an USB port, or through an SD card resulting in standalone operation.

The sensor board voltage and current sensors have been calibrated against a 0.8% accuracy multimeter. Temperature measurements have been calibrated using a class A RTD temperature sensor. A soft calibration feature of the firmware allows easy calibration by editing calibration parameters in a configuration file.

The last board is the power board, shown in figure 3. This is composed of a backplane where eight power supply blades are connected. Each blade is a

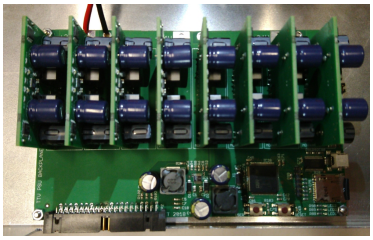

Fig. 3. The power board.

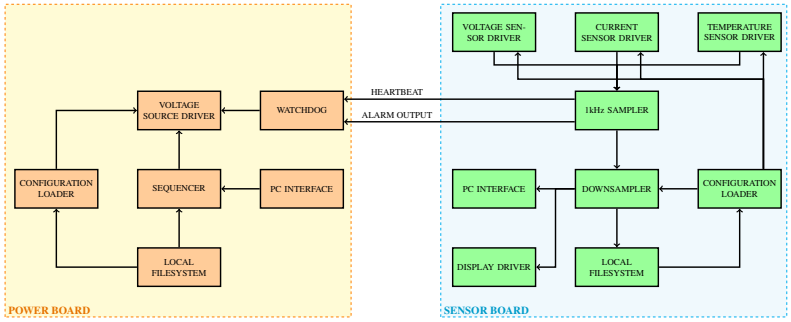

Fig. 4. Block diagram of the platform software.

software controllable dual output power supply providing power to two TTC heating elements. The backplane contains a similar microcontroller than the one in the sensor board.

3.2 Firmware architecture

The firmware for the sensor and power board is structured as in figure 4. Both firmwares are written in C++ and use the Miosix [12] operating system.

The sensor board has drivers for the temperature, voltage and current sensors, which are operated by a sampling thread operating ar 1kHz. The sampling thread collects the raw measurements, computes the values using the calibration parameters made available by the configuration loader, and checks that the temperatures are still within the safe limit, signaling an alarm to the power board if required. A heartbeat signal is also provided to protect the system. The power board cuts off power to the TTC should the alarm be raised, or in the case of irregualrites in the heartbeat signal. The power board has a driver for the software controllable power supply and a sequencer thread that produces the desired power waveform either from the local filesystem or PC.

4 Experimental evaluation

We performed a series of experiments with a commercial copper heat sink available at Digikey, of type HS483-ND, attached to the TTC, both under natural

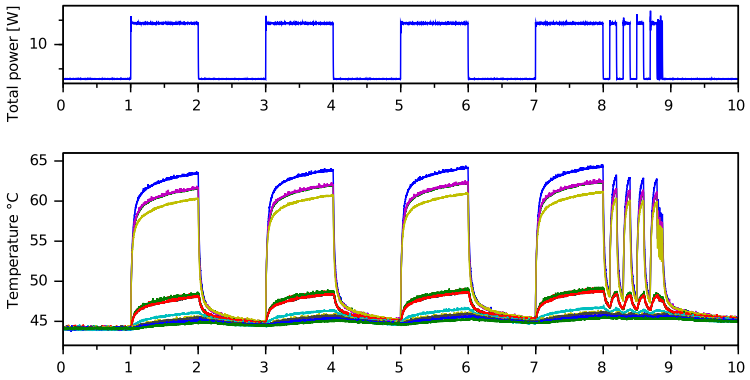

Fig. 5. Temperature profile produced by a step respone of four heating elements with period 2s, 200ms 20ms.

convection and forced convection using a P14752-ND fan. The collected dataset can be used to integrate a model of that heat sink in any thermal simulator. This dataset, consisting of 39 experiments, for a total of 78 individual figures showing power and temperature, is too large to fit in the paper, so only selected figures are reported. The full dataset will be released in the form of raw `csv` files that can be directly used to compare the experiment results with the output of a thermal simulator for validation and parameter identification.

Additionally, to show how the proposed thermal experimentation platform can be integrated with an architectural simulator, we performed an experiment with a power trace coming from the simulation of an MPSoC executing a subset of the MiBench benchmarks.

4.1 A first Dataset

To accurately model a heat sink both in transient and steady state, we designed a campaign composed of three groups of experiments using 13 different power maps each, for a total of 39 experiments. The 13 power maps are constructed using different patterns of activation of the heating elements, providing a 3W power to active heating elements, and 0.2W to inactive ones. The last four patterns are dedicated to hotspots, where only one heating element is given 7W, leaving all the other at 0.2W.

Of the three group of experiments, the first uses the 13 patterns to identify the fast thermal dynamics occurring near the silicon active layer. To this end, a sequence of step responses is used alternating between the given pattern and a blank pattern where all heating elements provide 0.2W. The step responses is repeated with a 2s, 200ms and 20ms period. Figure 5 shows one of the 13 patterns which consists in turning on the four heating elements in the northwest side of the chip. The top part shows the readback of the total power provided to the heating elements, while the bottom part shows the corresponding temperature of each of the 16 heating elements (each shown in a different color), sampled

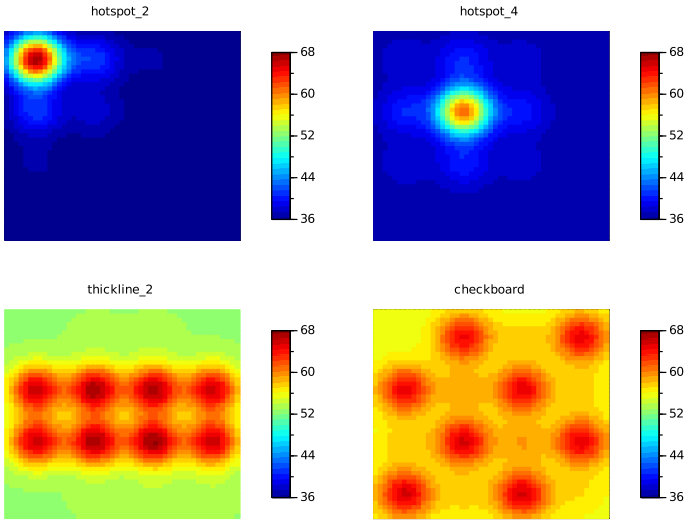

Fig. 6. Steady state temperature map interpolated from the TTC sensors, for four different conditions taken from the dataset.

at 1kHz. The heating element reaching the highest temperature is the one in the corner of the chip, as it can dissipate heat laterally only to two of its sides. The two elements with only one side at the corner of the chip reach the second highest temperature (both reach the same temperature and thus the traces overlap), followed by the fourth activated element. The other heating elements, even though they are kept at a constant power, exhibit a temperature increase due to thermal coupling. As can be seen, the proposed thermal validation platform allows to capture high resolution temperature transients of the TTC attached to the desired thermal dissipation solution, providing validation and identification information for transient thermal simulations.

The second and third group of experiments is instead dedicated to the identification of the slow thermal dynamics, caused by the heat sink heating up. One set of experiments was performed under natural convection the other with the fan active at full power. Each experiment group consists in applying each of the 13 patterns as a single 30 minutes long step response. Although the experiment dataset includes full thermal transients used for heat sink transient modelling, we will here present them in the form of a steady state temperature map with the temperature at the end of the 30 minutes step response. Figure 6 shows four of the 13 experiments with the fan active. The top two experiments are hot spot experiments, where a single heating element is dissipating 7W, while all the other 0.2W. In the left case, where the hotspot is in the corner, a temperature of 68.3°C is reached, and the maximum thermal gradient is 32.5°C. In the right case, the hotspot can better conduct heat laterally, thus its temperature is lowered to 61.9°C, and the maximum thermal gradient has been

reduced too, to 24.9°C. The bottom experiments instead explore the case where 8 heating elements are active at 3W, and the other at 0.2W. The left case shows a maximum temperature of 68.2°C, while the right one shows that spreading heating elements reduces the maximum temperature to 66.6°C and the gradient to 10.5°C.

4.2 Simulation flow integration example

The proposed thermal validation platform is not limited to producing step responses or steady-state studies, but is also very useful for showing the behaviour of a dissipation setup in the face of a theraml load coming from real software execution. To show this, the validation platform, with the same heat sink as in the previous experiments, was connected to the simulation flow [14], which uses GEM5 [2], McPAT [8] and Orion [7] to simulate an MPSoC power consumption. The example configuration of the simulation flow was used, which simulates a 12 core architecture with four tiles of 3 cores interconnected by NoC routers. Each core is an Alpha out-of-order processor executing Mibench benchmarks. Table 1 reports the main architectural parameters. The simulation flow includes a floorplan to grid mapper that can produce power values for a uniform grid. We configured the grid as 4x4, thus matching the heating elements of the thermal test chip.

The top part of Figure 7 shows the power applied to each of the 16 heating elements (each shown using a different color), while the bottom part shows the temperature trace of each of the TTC heating elements (again each shown with a different color). The experiment was performed with the heat sink under natural convection while executing a sequence of Mibench benchmarks, namely basicmath, bitcount, crc, fft, sha1, stringsearch.

As can be seen, the proposed thermal validation can be integrated in an MPSoC simulation workflow instead of a simulated thermal model. Although the number of heating elements is fixed to 16, interpolation can be used to map an arbitrarily complex floorplan into the available elements.

5 Conclusions and future work

This paper has presented a generic solution to the problem of validating thermal models, in the form of a thermal validation platform making use of a thermal

Table 1. Microarchitectural parameters.

Processor core	2GHz, out-of-order Alpha core
Functinal Units	4 Int-ALU, 2 Int-Mult/Div, 2 FP-Mult/Div
L1 cache	64kB 2-way set assoc. split I/D, 2 cycles latency
L2 cache	512KB per bank, 8-way associative
Coherence Prot.	MESI
Router	3-stage wormhole switched with 64b link width, 4vcs per vnet
Topology	2D-mesh 4 tiles 2x2 (3 CPU per tile)
Technology	32nm at 1.1V

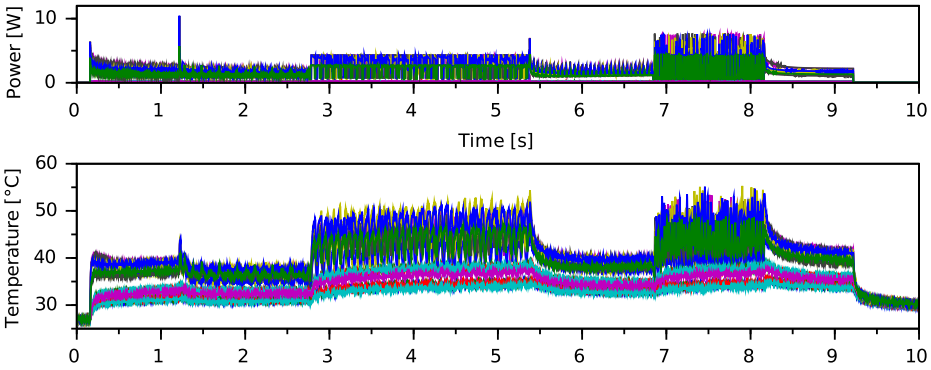

Fig. 7. Temperature profile produced by the TTC sensors when subject to the power computed by simulating the execution of seven mibench benchmarks.

test chip. This solution allows to apply a known power spatial distribution to a TTC connected to the cooling solution under test, and measure the corresponding transient and steady state temperature across said chip. This platform allows to collect the critical measurements required for thermal model parameter identification and validation, and is expected to help in improving the flexibility of thermal simulator by lowering the barrier required to accurately model innovative cooling solution. A first validation dataset has been provided for a commercial heat sink, and work is already underway to add its model to the 3D-ICE thermal simulator, as well as to characterise other heat dissipation solutions. When the PC-side software support tools are complete, we plan to publish its design as Open Hardware, to allow researchers to build their own apparatus and use it for heatsink modeling and hardware-in-the-loop MPSoC simulations.

Acknowledgements

The work has been partially supported by the H2020 projects MANGO (GA 671668) and RECIPE (GA 801137).

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