

# A novel sufficient condition to avoid subharmonic oscillations for buck converters with constant on-time control

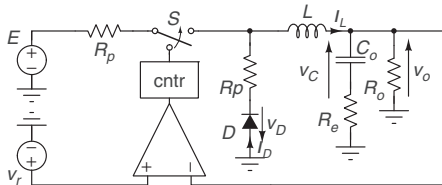
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Fast transient response, simple control scheme and low cost are features that distinguish constant-on-time buck converters from others. Simplicity of the control scheme is reflected in a single requirement for power electronics engineers: a design that ensures enough low amplitude resistive ripple component at the feedback to precisely starts the on-time pulse. There are design rules that guide the selection of the components. A well known one reported in the literature predicts if the converter suffers of the sub-harmonic oscillations undesirable phenomenon. The authors present a better simple design expression to avoid the onset of this unwanted drawback.

**Introduction:** Constant ON-Time (COT) DC-DC converters are popular for point-of-load (POL) regulation [1, 2]. Their excellent dynamic response, simple control scheme and mainly low cost makes COT POL regulators an attractive choice for powering demanding, high-speed digital loads such as FPGAs, ASICs, and CPUs. For the same reasons, COT converters are also largely used in low cost consumer electronics. From a design perspective, a very important practical problem is to ensure that the COT converter will operate without a pulse-bursting [3], viz. avoiding sub-harmonic oscillations.

Avoiding pulse-bursting in steady-state operating conditions is necessary to prevent excessive ripple amplitudes in the inductor current and output voltage waveforms, whose undesirable consequences may include degraded efficiency, reduction of the output current capability because of premature engagement of current limit protections, and, most important, violation of the steady-state output voltage ripple specifications (output voltage noise). Unpredictable Electro-Magnetic emissions might also be a concern.

In this Letter, we provide a straightforward novel sufficient condition, overcoming in term of reliability the popular one presented in [4], to prevent the appearance of such dynamical behaviour. This condition is valid not only when the COT converter works in steady state but also during transient evolutions. We focus on the COT converter architecture reported in Fig. 1, which considers also the  $R_p$  resistors modelling both the ON-state resistance of the  $S$  high-side switch and the  $D$  low-side switch.



**Fig. 1** Schematic of the COT converter

Circuit parameter reference values:  $C_o = 35.3 \mu\text{F}$ ,  $R_e = 12.3 \text{ m}\Omega$ ,  $R_p = 30 \text{ m}\Omega$ ,  $L = 470 \text{ nH}$ ,  $E = 5 \text{ V}$ ,  $v_r = 1 \text{ V}$ ,  $\Delta t_{\text{OFF}}^{\text{min}} = 177 \text{ ns}$  and  $\Delta t_{\text{ON}} = 118 \text{ ns}$

**COT converter architecture:** A key aspect of the COT converter is its control algorithm implemented in the cntr block (see Fig. 1). It can be summarised as follows:

Step 1: The  $S$  switch is closed for the  $\Delta t_{\text{ON}}$  fixed time interval (ON-phase) as soon as the controller catches the positive edge of the output of the comparator. This occurs any time the  $v_r - v_o$  signal becomes positive.

Step 2: At the end of the ON-phase,  $S$  is opened and is kept open for the  $\Delta t_{\text{OFF}}^{\text{min}}$  fixed time interval (minimum OFF-phase).

Step 3: At the end of the  $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\text{min}}$  time interval, the controller checks the output of the comparator. If  $v_r - v_o < 0$ , the  $S$  switch remains open (OFF-phase) until the condition at Step 1 becomes true. Otherwise, if  $v_r - v_o > 0$ , i.e. the output of the comparator is still positive, the  $S$  switch is closed again and a new ON-phase starts immediately. The overall duration of the OFF-phase is  $\Delta t_{\text{OFF}} \geq \Delta t_{\text{OFF}}^{\text{min}}$ .

The role of the  $D$  diode in Fig. 1 is to avoid a negative  $i_L$  current. Actually, in modern architectures such as synchronous buck converters, to enhance converter efficiency the diode is replaced by a low-side

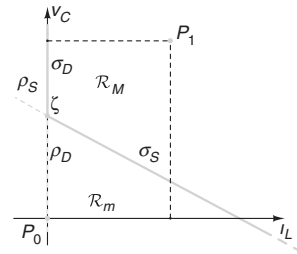
MOSFET which is operated as a synchronous rectifier. Consequently, ‘diode’  $D$  – that actually works as a controlled switch in perfect ‘diode emulation’ – is modelled as a piecewise-linear ideal component with  $i_D = 0$  for  $v_D \leq 0$  and  $v_D = 0$  for  $i_D \geq 0$ .

In the  $(i_L, v_C)$  state plane (shown in Fig. 2) the  $v_r - v_o = 0$  switching condition induced by the cntr block leads to the straight line

$$\rho_S(i_L, v_C) : v_r - \frac{R_o(i_L R_e + v_C)}{R_e + R_o} = 0 \quad (1)$$

whereas the effect of the  $D$  low-side switch defines

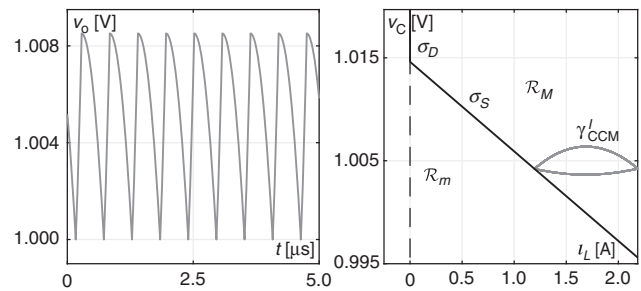
$$\rho_D(i_L, v_C) : i_L = 0 \quad (2)$$



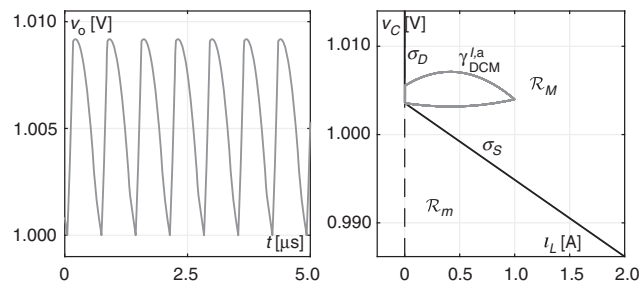
**Fig. 2** Basic geometrical elements on the  $(i_L, v_C)$  state plane

The  $\mathcal{R}_m$  (resp.  $\mathcal{R}_M$ ) sub-region of the state space is made up of those points lying both at the right of the  $\rho_D$  line and below (resp. above) the  $\rho_S$  line.  $\mathcal{R}_m$  and  $\mathcal{R}_M$  are separated by the half-line  $\sigma_S \subset \rho_S$  that originates in  $\zeta$

**Geometry of the steady-state solutions:** Typical regular steady-state trajectories of a well-behaving COT converter, in both continuous current mode (CCM) and discontinuous current mode (DCM) are shown in Figs. 3 and (4), respectively. They were obtained for the reference circuit parameter values reported in the caption of Fig. 1, by setting  $R_o = 0.59 \Omega$  and  $R_o = 2.43 \Omega$ , respectively (for all numerical results presented in the following, only the circuit parameter values that differ from the reference ones are reported).



**Fig. 3** Regular CCM steady-state solution of the COT converter.  $R_o = 0.59 \Omega$



**Fig. 4** Regular DCM steady-state solution of the COT converter.  $R_o = 2.43 \Omega$

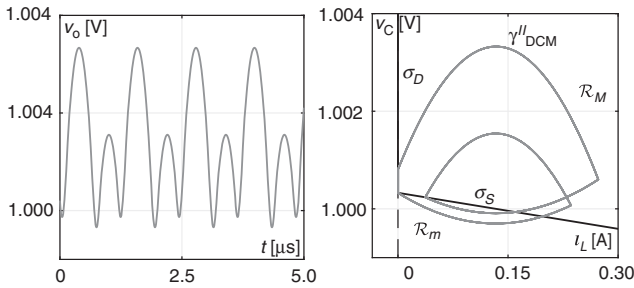
The ON-phase of the  $\gamma_{\text{CCM}}^a$  and  $\gamma_{\text{DCM}}^a$  limit cycles starts on  $\sigma_S$  (Step 1 of the control algorithm) for  $i_L > 0$  and  $i_L = 0$ , respectively.  $\sigma_S$  is the half-line belonging to  $\rho_S$  originating in  $\zeta$  (see Fig. 2). In the DCM regime, the trajectory hits  $\sigma_D$  during the OFF-phase and it slides on it till  $\zeta = \rho_D \cap \rho_S = (0, (v_r(R_e + R_o)/R_o))$ , where the OFF-phase ends since  $\sigma_S$  is reached.  $\sigma_D$  is the half-line belonging to  $\rho_D$  originating in  $\zeta$  (see Fig. 2). From the left panel of both Figs. 3 and (4), we can see that the  $v_o$  voltage (Fig. 1) keeps greater or equal to  $v_r$ . This traduces in trajectories in the  $(i_L, v_C)$  state plane evolving in the  $\mathcal{R}_M$  region only (see Fig. 2).

In both cases, it is assumed that the COT converter controller is not saturated at steady state, viz. the OFF-phase lasts more than  $\Delta t_{\text{OFF}}^{\text{min}}$ .

The  $\gamma_{\text{CCM}}$  and  $\gamma_{\text{DCM}}^a$  limit cycles make *regular* the COT converter steady-state behaviours in the sense that they do not exhibit sub-harmonic oscillations, viz. such limit cycles is composed of a *single turn*.

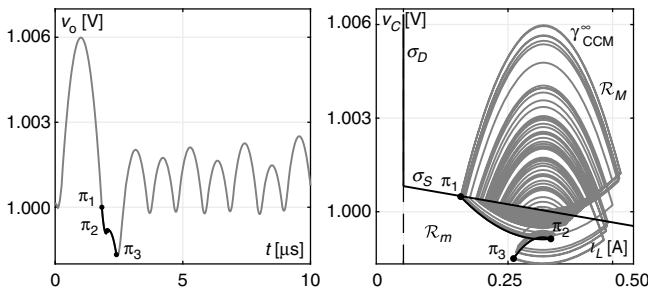
It is well-known that a bad selection of the COT converter parameters leads to steady-state solutions much more complex than  $\gamma_{\text{CCM}}$  and  $\gamma_{\text{DCM}}^a$ . This is due to the fact that even if the COT converter dynamics is governed by a piecewise linear vector field, the decisional process implemented by its controller is articulated even if simple its design is simple.

In Fig. 5, for instance the  $\gamma_{\text{DCM}}^b$  limit cycle is shown, which is characterised by the presence of *two turns*. It is worth noticing that it is made up of two ON-phases and two OFF-phases. The segments of trajectory corresponding to the ON-phases starts on  $\sigma_S$  and evolve both in  $\mathcal{R}_m$  and  $\mathcal{R}_M$ . Thus in the left panel of Fig. 5 we observe the  $v_o$  voltage becoming lower than  $v_r$ . Both such segments end in  $\mathcal{R}_M$  and consequently the OFF-phase are expected to last more than  $\Delta t_{\text{OFF}}^{\text{min}}$  (see Step 3 of the control algorithm).



**Fig. 5** Sub-harmonic DCM steady-state solution of the COT converter with  $\tau_{\text{OLD}} = 59$  ns and  $\tau_{\text{NEW}} = 66.80$  ns and  $\tau = 17.37$  ns  
 $C_o = 7.06$   $\mu\text{F}$ ,  $R_e = 2.46$  m $\Omega$ ,  $L = 2.0$   $\mu\text{H}$  and  $R_o = 7.5$   $\Omega$

In Fig. 6, the  $\gamma_{\text{CCM}}^{\infty}$  CCM steady-state chaotic trajectory is shown. It evolves both in  $\mathcal{R}_m$  and  $\mathcal{R}_M$ . We see segments of the trajectory corresponding to ON-phases that do not end above  $\sigma_S$  (see, for instance the black coloured segment from  $\pi_1$  to  $\pi_2$  in Fig. 6). For this reason, according to Step 3 of the control algorithm, each one of these segments is followed by a minimum OFF-phase (from  $\pi_2$  to  $\pi_3$  in Fig. 6).



**Fig. 6** Sub-harmonic (chaotic) CCM steady-state solution of the COT converter with  $\tau_{\text{OLD}} = 54$  ns,  $\tau_{\text{NEW}} = 166.67$  ns and  $\tau = 17.37$  ns  
The orbit in the right panel refer 30  $\mu\text{s}$  of time evolution.  $C_o = 7.06$   $\mu\text{F}$ ,  $R_e = 2.46$  m $\Omega$ ,  $L = 2.0$   $\mu\text{H}$ ,  $R_o = 3.0$   $\Omega$  and  $\Delta t_{\text{ON}} = 108$  ns

Both the  $\gamma_{\text{DCM}}^b$  and  $\gamma_{\text{CCM}}^{\infty}$  steady-state behaviours exhibit undesired sub-harmonic oscillations.

*Avoiding sub-harmonic regime:* The well-known condition to predict the appearance of sub-harmonic regimes for COT buck converters

$$C_o R_e \equiv \tau > \frac{\Delta t_{\text{ON}}}{2} \equiv \tau_{\text{OLD}} \quad (3)$$

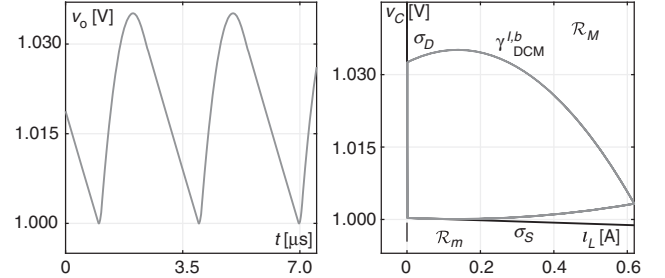
was provided in [4] and it can be used if the COT converter works in CCM. Here we propose the novel constraint

$$C_o R_e \equiv \tau > \frac{L_o v_r}{R_o (E - v_r)} \equiv \tau_{\text{NEW}} \quad (4)$$

that represents a *true sufficient condition to avoid sub-harmonic regimes*. It turns out to be more accurate than (4) and it works in DCM too.

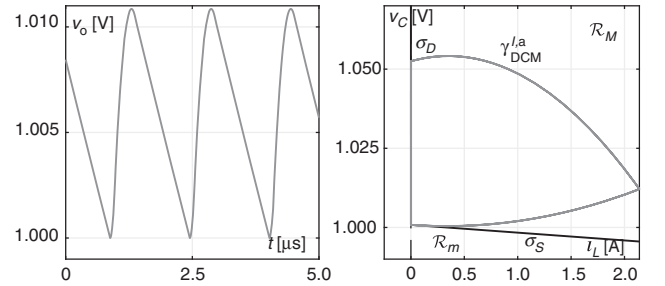
Let us consider the  $\gamma_{\text{DCM}}^b$  and  $\gamma_{\text{CCM}}^{\infty}$  steady-state behaviours presented above. According to the values of  $\tau$ ,  $\tau_{\text{OLD}}$  and  $\tau_{\text{NEW}}$  reported in the caption of Figs. (5) and (6), we note that (3) and (4) are not satisfied in both cases (we recall that actually (3) should be used only for  $\gamma_{\text{CCM}}^{\infty}$  since in [4] a condition for DCM operation is not provided).

As far as  $\gamma_{\text{DCM}}^b$  is concerned, to verify the effectiveness of (4) we increased the  $E_o$  value in order to reduce  $\tau_{\text{NEW}}$  keeping  $\tau_{\text{OLD}}$  unchanged. The result is shown in Fig. 7. The  $\gamma_{\text{DCM}}^b$  limit cycle does not exhibit sub-harmonic oscillations even if (3) is significantly violated.



**Fig. 7** DCM steady-state solution of the COT converter with  $\tau_{\text{OLD}} = 59$  ns and  $\tau_{\text{NEW}} = 15.23$  ns and  $\tau = 17.37$  ns  
 $C_o = 7.06$   $\mu\text{F}$ ,  $R_e = 2.46$  m $\Omega$ ,  $L = 2.0$   $\mu\text{H}$ ,  $R_o = 7.5$   $\Omega$  and  $E_o = 12.5$  V

Something similar can be done to regulate  $\gamma_{\text{CCM}}^{\infty}$ , for instance reducing the  $L_o$  inductance. In Fig. 8, it can be seen the  $\gamma_{\text{DCM}}^a$  limit cycle, which is regular even if (3) is not satisfied.



**Fig. 8** DCM steady-state solution of the COT converter with  $\tau_{\text{OLD}} = 54$  ns,  $\tau_{\text{NEW}} = 16.67$  ns and  $\tau = 17.37$  ns  
 $C_o = 7.06$   $\mu\text{F}$ ,  $R_e = 2.46$  m $\Omega$ ,  $L = 0.2$   $\mu\text{H}$ ,  $R_o = 3.0$   $\Omega$  and  $\Delta t_{\text{ON}} = 108$  ns

The numerical results that we illustrated clearly prove that the condition presented in [4] as a tool for the prediction of sub-harmonic oscillations may fail. Furthermore (4) is more articulated and depends on more design parameters of the COT converter than (3). The next section is devoted to the analytical derivation of (4) and to its peculiarity of being a *sufficient condition* to avoid sub-harmonic oscillations. Furthermore, it is shown how (4) can be approximately reduced to (3) in CCM.

*Theoretical aspects:* The dynamics of the COT converter (for  $i_L > 0$ ) is ruled by the state equations

$$\begin{aligned} \dot{v}_C &= \frac{R_o i_L - v_C}{(R_e + R_o) C_o}, \\ \dot{i}_L &= -\frac{(R_e (R_o + R_p) + R_o R_p) i_L + R_o v_C}{(R_e + R_o) L_o} + \xi \frac{E}{L_o}, \end{aligned} \quad (5)$$

where  $\xi = 1$  in the ON-phase and  $\xi = 0$  in the OFF one. The piecewise linear dynamical system described by (5) admits the two

$$P_{\xi} = \left( \frac{E R_o \xi}{R_o + R_p}, \frac{E \xi}{R_o + R_p} \right)$$

different equilibria for  $\xi \in \{0, 1\}$  (see Fig. 2). The generic orbit of (5) is attracted by either  $P_1$  or  $P_0$  (see Fig. 2), during the ON-phase or the OFF-phase, respectively.

Since the vector-field in the r.h.s. of equation (5) is autonomous, i.e. it does not explicitly depend on time, previous theoretical results state that

trajectories in the  $(i_L, v_C)$  state plane are not allowed to intersect once a given value of  $\xi$  is selected. This consideration is crucial since it is the pillar condition equation (4) grounds on. Owing to the relative position of  $\sigma_S$  and  $P_1$  it turns out that sub-harmonic oscillations may appear only if ON-phase segments of trajectory are allowed to visit  $\mathcal{R}_m$ . In fact, this makes possible the *folding* mechanism clearly visible in Fig. 5. Furthermore, as it can be realised from Fig. 6, owing to the very nature of the control algorithm of the COT converter, if the ON-phase ends below  $\sigma_S$  it is possible to observe sequence of segments as the  $\pi_1 - \pi_2 - \pi_3$  one that generates a steady-state behaviour characterised by *multiple* turns. If the converter parameters are chosen in such a way that trajectories originated on  $\sigma_S$  at the beginning of the ON-phase are enclosed within  $\mathcal{R}_M$ , sub-harmonic oscillations can be avoided.

With this caveat in mind, let us introduce the unit-vector normal to  $\rho_S$

$$\eta = \left( \frac{1}{\sqrt{1+R_e^2}}, \frac{R_e}{\sqrt{1+R_e^2}} \right)^T \quad (6)$$

and formulate the constraint

$$\eta^T \cdot (\dot{v}_C, i_L|_{\xi=1})_{(v_C, i_L) \in \sigma_S} > 0 \quad (7)$$

that forces the vector-field in (5) (with  $\xi = 1$ ), computed for any point on  $\sigma_S$  at the beginning of the ON-phase, to ‘push’ the state of the system in  $\mathcal{R}_M$ . Equation (7), which practically states that on  $\sigma_S$  the tangent vector to the system trajectories always exhibit a non-null component (the r.h.s. of (7)) that is oriented toward  $\mathcal{R}_M$ , recasts as

$$\frac{C_o R_e R_o (E_o - v_r) + \bar{i}_L R_o (L_o - C_o R_e R_p) - L_o v_r}{R_o C_o L_o \sqrt{R_e^2 + 1}} > 0, \quad (8)$$

where  $\bar{i}_L = i_L|_{(v_C, i_L) \in \sigma_S}$ . Under the realistic assumption  $L_o - C_o R_e R_p > 0$ , a more restrictive condition can be obtained by fixing  $\bar{i}_L = 0$ , i.e. setting it to its lower value. So doing (4) is achieved. We recall that at steady state in CCM operation assuming  $\bar{i}_L = 0$  is a restraint since actually the ON-phase starts on  $\sigma_S$  for  $i_L > 0$  (see  $\gamma_{CCM}^I$  in Fig. 3). On the contrary, (4) becomes exact in DCM since the ON-phase originates on  $\sigma_S$  for  $i_L = 0$  (see  $\gamma_{DCM}^I$  in Fig. 4).

Note that, once (7) is satisfied, sub-harmonic oscillations do not appear both in transient evolution, for example when there is a step change in load power demand, and at steady state.

By computing an approximation of the  $\Delta i_L$  current during the  $\Delta t_{ON}$  time interval through the assumption that the  $v_o$  voltage remains constant at  $v_r$ , it is possible to write  $L_o(\Delta i_L/\Delta t_{ON}) = E - v_r$ , from which

we have  $(L_o/(E - v_r)) = (\Delta t_{ON}/\Delta i_L)$ . In the CCM condition the  $i_o = (v_r/R_o)$  output current can be assumed equal to the average value of  $i_L$ , which is a positive constant, plus  $(\Delta i_L/2)$ . We can now write  $(v_r/R_o) \geq (\Delta i_L/2)$ . At the end we obtain

$$\underbrace{C_o R_e}_{\tau} \geq \underbrace{\frac{L_o}{E - v_r} \frac{v_r}{R_o}}_{\tau_{NEW}} \geq \frac{\Delta t_{ON}}{\Delta i_L} \frac{\Delta i_L}{2} = \underbrace{\frac{\Delta t_{ON}}{2}}_{\tau_{OLD}}$$

These crude approximations have collapsed (4) in (3). Note that in DCM condition (3) is incorrect since  $(v_o/R_o) < (\Delta i_L/2)$  while condition (4) is exact.

*Conclusion:* A novel modelling methodology of COT buck converters based on state-space variables has been introduced. This method leads to graphical representation and interpretation of the switching behaviour of a buck topology under COT control. A new sufficient condition to avoid pulse-bursting has been derived. Under simplifying assumptions, it has been shown that the new condition includes and largely improves the one already known in the literature.

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## References

- 1 Hariharan, K., Kapat, S., and Mukhopadhyay, S.: ‘Constant on/off-time hybrid modulation in digital current-mode control using event-based sampling’, *IEEE Trans. Power Electron.*, 2019, **34**, (4), pp. 3789–3803
- 2 Fu, W., Tan, S.T., Radhakrishnan, M., *et al.*: ‘A DCM-only buck regulator with hysteretic-assisted adaptive minimum-on-time control for low-power microcontrollers’, *IEEE Trans. Power Electron.*, 2016, **31**, (1), pp. 418–429
- 3 Wang, J., Xu, J., and Bao, B.: ‘Analysis of pulse bursting phenomenon in constant-on-time-controlled buck converter’, *IEEE Trans. Ind. Electron.*, 2011, **58**, (12), pp. 5406–5410
- 4 Li, J., and Lee, F.C.: ‘Modeling of  $v^2$  current-mode control’, *IEEE Trans. Circuits Syst. I, Regul. Pap.*, 2010, **57**, (9), pp. 2552–2563