Partitioning-Based Unified Power Flow Algorithm for Mixed MTDC/AC Power Systems

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***Abstract*—This paper presents a unified power flow algorithm for large and complex mixed AC/DC power systems based on the partitioning of power grids, a version of the two-level Newton method, and the modified nodal analysis formulation. Partitioning significantly increases numerical efficiency without altering the accuracy of the power flow solution. This approach can be applied to any combination of multiple DC and possibly non-synchronized AC systems. It considers the steady-state interaction of AC and DC systems for a wide range of converter representations and control functions. Simplification of elements within the converter stations is not required. Both DC and AC-side converter losses are adequately accounted for by using a generalized converter loss model. The steady-state converter equations are derived in their most general form, with the AC and/or DC-side power exchange or voltages defined as controlled quantities.**

***Index Terms*—AC/DC, HVDC transmission, MTDC, power flow analysis, circuit partitioning.**

I. Introduction

POWER flow algorithms are widely used by engineers and play an essential role in power system analyses. These algorithms were originally developed to find the steady-state solution of large and complex AC systems in a fast and efficient way. Modern numerical tools can determine the power flow solution (PFS) of AC power systems described by the single-phase equivalent model and composed of hundreds of thousands of buses and tens of thousands of synchronous generators within reasonable CPU times.

Several power system analyses, such as the small-signal stability analysis, require as input the PFS. Once the PFS is determined, the AC system dynamic model can be initialized, then linearised around the PFS and finally used to perform a small-signal stability analysis [1].

This simulation paradigm has been recently changing due to the increased penetration of high voltage direct current (HVDC) and multi-terminal direct current (MTDC) systems connecting portions of the same AC grid or separated, possibly asynchronous, large AC grids. This has triggered the need to improve and extend conventional power flow (PF) tools to deal with mixed AC/DC systems.

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The literature reports several papers on algorithms to compute the PFS of mixed AC/DC power systems and groups them into two main classes: *sequential* methods [2]–[6] and *unified* methods [7]–[10].

Sequential methods derive their name from the fact that the AC and the DC sub-systems are sequentially and repeatedly solved. This approach comprises four steps and considers AC/DC converters as interfacing elements between AC and DC networks. It provides a first AC-side PFS solution by guessing the power exchange of the DC slack converters (i.e., those in charge of controlling the DC-side voltage). Then, the algorithm defines, based on the AC-side steady-state quantities just found, the power losses and the corresponding power flows at the DC-side point of connection (POC) of all converters but the DC slack ones. Then, the method calculates the DC-side PFS and updates the AC-side power exchange of every converter, including DC slack ones. The power injection of DC slack converters constitutes a new guess for the next iteration of the sequential mixed AC/DC PF computation process. The algorithm iterates and sequentially applies the steps above to solve the AC and DC sub-systems until electrical quantities at the interfaces (i.e., the AC/DC converters) converge.

Sequential solvers solve the same AC and DC sub-systems several times, which makes them less efficient than unified solvers, from a numerical standpoint. Indeed, as stated in [5], a sequential algorithm solves AC sub-systems on average 2.4 times. This iteration process is prone to convergence issues since it depends on the algebraic characteristics of the electrical models of the AC and DC systems under analysis. This is a typical aspect of all sequential methods, which require all the eigenvalues of the iteration matrix to be inside the unit circle in the complex plane [11], [12]. The convergence behavior of the sequential approach is analyzed in detail in [13], when mixed AC/DC power systems are overloaded. A similar analysis on an overloaded version of the IEEE14 test system with an HVDC link [2], [14] was described in [15]. These works show that the number of iterations of the sequential solver largely increases with overloading (see [16] for a detailed comparison between sequential and unified solvers).

On the contrary, the unified approach considers AC and DC grids concurrently, thereby deriving a single PFS for the whole AC/DC power system at once [8]. This method, which includes AC/DC converters in the computation process through a set of nonlinear equations, shows superior convergence robustness to the sequential one.

The robustness of PF methods is crucial for facilitating engineering studies of complex network configurations [17]–[19].

However, the multitude of buses, converters, and synchronous generators in AC/DC systems may compromise the robustness and numerical efficiency of such methods. For example, let us assume to employ the well-known Newton method to solve the nonlinear algebraic equations of a large power system and, thus, its PF. If a small portion of the entire power system suffers convergence problems, the Newton method will perform several iterations, trying to get convergence. At each iteration, the method must re-evaluate the electrical characteristics of all power elements and re-factorize a very large, typically sparse Jacobian matrix. These are the two main CPU time-consuming tasks in PF algorithms. According to [20], [21], the CPU time needed to factorize the Jacobian is almost quadratically-dependent on the number of equations.

In this paper, we show that adequately partitioning the whole mixed AC/DC power system in smaller sub-systems can lead to significant advantages from the point of view of numerical efficiency. Additionally, partitioning allows the use of multiple threads to solve several sub-systems in parallel, while at the same time isolating sub-systems that cause convergence problems. More robust "fall-back" numerical methods, even though CPU time consuming, can be employed only on these smaller problematic portions of the full system [22], [23]. The reduced size of the Jacobian matrix and the reduced number of power elements of these troublesome sub-systems drastically limit the potential impact of low numerical efficiency.

The major contribution of this paper is the development of a general and fast approach for the determination of the PFS of large and mixed AC/DC power systems based on a unified method and system partitioning. The proposed algorithm exploits the presence of AC/DC converters and transformers to suitably partition DC and AC systems. Partitioning allows finding the PFS of an entire AC/DC power system by solving the PF of a given set of its sub-systems (both AC and DC) in a specific order. Contrary to sequential solvers, these sub-systems are solved only once because a unified approach is adopted. By solving the PF of smaller sub-systems, the method considers fewer equations and can compute the PFS of some sub-systems in parallel. As shown, both these aspects grant the proposed method a boost in numerical efficiency. The approach relies on the modified nodal analysis (MNA) due to its superiority in handling basic modeling elements [24], [25][1]. It can be applied to combined AC/DC grids, where power flows in possibly asynchronous AC grids connected via an HVDC/MTDC link [7], [8]. We consider lossy HVDC lines and different types of AC/DC converters, with their main controller configurations (e.g., page 44 of [28]) and losses of AC/DC converters as functions of the AC and DC-side currents. The proposed approach was coded in our circuit/power-system simulator [29], [30], and comparisons are performed with state-of-the-art toolboxes for PF computation in hybrid AC/DC systems [31]–[33].

[1]The modified nodal analysis (MNA) adds currents of "bad-branches" (i.e., elements with electrical characteristics that are not defined on a voltage-basis) among the unknowns. MNA facilitates managing non-linear elements with implicit characteristics that depend on port voltages and currents, and writing of differential-algebraic equations. Textbook descriptions of MNA can be found in [26], [27].

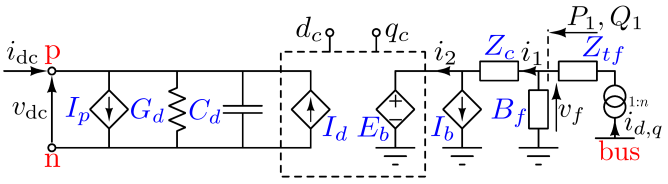

Fig. 1. The equivalent averaged model of the AC/DC converters used in the MTDC grid.

II. The Models of the AC/DC Converters

We use an equivalent averaged model [4], [5] in the DQ axis frame for each AC/DC converter [34] and assume that the AC grids are modeled by the single-phase equivalent model. The schematic in Fig. 1 depicts the equivalent circuit of an AC/DC converter. The bus terminal is the POC of the AC/DC converter to the AC grid. We assume, as in practice happens, that the different controlling functions implemented in the various types of AC/DC converters act to maintain the desired electrical quantities at their AC-side and DC-side POC. For example, in an AC/DC converter that implements a PQ power control the d, q voltage components of the E_b controlled generator are regulated so that the AC/DC converter exchanges the desired active and reactive power at the POC.

The I_d controlled current generator drives the HVDC lines connected to the p and n nodes of the DC-side of the converter. The sum of the power absorbed by I_d and the P_{E_b} active power absorbed by E_b (both in the dashed box in Fig. 1) is always *null*. Therefore the two controlled sources constitute an ideal-active-power coupler.

The impedance of the transformer is given by $Z_{tf} = R_{tf} + jX_{tf}$, where $j = \sqrt{-1}$, and B_f and $Z_c = R_c + jX_c$ model respectively the susceptance of the AC filter and the arm impedance. The I_b controlled current source models averaged additional power losses of semiconductors [3]. This power dissipation is expressed through the following polynomial of the AC-side current component i_1

$$P_b = A_{\rm ac} + B_{\rm ac}\,|i_1| + C_{\rm ac}\,|i_1|^2 \ , \tag{1}$$

where $A_{\rm ac}, B_{\rm ac}, C_{\rm ac} \in \mathrm{R}$ are fitting parameters, derived from accurate electro-magnetic transient simulations of the converter. Equation (1) derives from [5], [13] (that in turn are based on [35]) and is justified by the fact that most of the losses of the AC/DC converters are those of semiconductors that in turn depend on the AC-side current flowing in the legs of the AC/DC converter and on the switching frequency. The G_d conductance on the DC-side of the AC/DC converter models losses depending on the $v_{\rm dc}$ voltage. The I_p controlled current source models averaged additional power losses of semiconductors due to the DC-side current component I_d. This power dissipation is given by

$$P_p = A_{\rm dc} + B_{\rm dc}\,|I_d| + C_{\rm dc} I_d^2, \tag{2}$$

where $A_{\rm dc}, B_{\rm dc}, C_{\rm dc} \in \mathrm{R}$ are fitting parameters that can be derived as those in (1).

The C_d capacitor accounts for the equivalent capacitance of

the legs of the AC/DC converter and filters if any. It has no meaning in the determination of the PFS but plays a role in small-signal stability analysis.

As stated in the Introduction, we use the MNA formulation. In implementing the model of each AC/DC converter, we link in implicit/explicit equations the dependent $i_{d,q}$ and $i_{\rm dc}$ currents to the $v_{d,q}$ voltages at bus and the $v_{\rm dc}$ one shown in Fig. 1. These equations are

$$\begin{cases} i_d = \dfrac{v_d P_{\rm bus} + v_q Q_{\rm bus}}{v_d^2 + v_q^2} \\ i_q = \dfrac{v_q P_{\rm bus} - v_d Q_{\rm bus}}{v_d^2 + v_q^2} \end{cases} \tag{3}$$

$$\begin{cases} P_1 = P_{\rm bus} - R_{tf} \dfrac{i_d^2 + i_q^2}{n^2} \\ Q_1 = Q_{\rm bus} - X_{tf} \dfrac{i_d^2 + i_q^2}{n^2} \end{cases} \tag{4}$$

$$|v_f|^2 = n^2 \frac{P_1^2 + Q_1^2}{i_d^2 + i_q^2} \tag{5}$$

$$|i_1|^2 = \frac{P_1^2 + \left(Q_1 - B_{\rm f} |v_f|^2\right)^2}{|v_f|^2} \tag{6}$$

$$P_{E_b} = P_1 - R_{\rm c} |i_1|^2 - P_b \tag{7}$$

$$v_{\rm dc} i_{\rm dc} + P_{E_b} - P_p - G_d v_{dc}^2 = 0, \tag{8}$$

where $P_{\rm bus}$ and $Q_{\rm bus}$ are the active and reactive power absorbed at bus, and P_{E_b} is the active power absorbed by E_b. These equations are an extension of those in [4], [5], [13].

The d_c and q_c terminals act on the d, q voltage components of the E_b voltage-controlled source and can be used to implement the following control functions, which are typically adopted in AC/DC converters.

- AC-PQ – The $P_{\rm bus}$ and $Q_{\rm bus}$ active and reactive power absorbed from bus are known parameters. The v_d and v_q voltages are the unknowns on the AC-side. The target of the algorithm that computes the PFS is to determine them (AC $\rightarrow$ DC).
- AC-PV – $P_{\rm bus}$ and $|v_{\rm bus}| = \sqrt{v_d^2 + v_q^2}$ are known parameters. The $Q_{\rm bus}$ reactive power and the phase of the $v_{\rm bus}$ voltage are the unknowns (AC $\rightarrow$ DC).
- AC-SLACK – The v_d and v_q voltages are known. The $P_{\rm bus}$ and $Q_{\rm bus}$ powers are the unknowns (AC $\rightarrow$ DC).
- DC-SLACK/AC-Q – The $v_{\rm dc}$ voltage and $Q_{\rm bus}$ are known parameters, whereas the $i_{\rm dc}$ current on the DC-side and the v_d and v_q voltages are the unknowns. (DC $\rightarrow$ AC).
- DC-SLACK/AC-V – The $v_{\rm dc}$ voltage and $|v_{\rm bus}| = \sqrt{v_d^2 + v_q^2}$ are known parameters, whereas the $i_{\rm dc}$ current and $Q_{\rm bus}$ are unknown (DC $\rightarrow$ AC).

In the list, we adopted the (AC $\rightarrow$ DC) or (DC $\rightarrow$ AC) symbols, which recur in the sequel when considering the AC/DC power systems in Fig. 2 and Fig. 4. The grid on the left of each arrow is the one whose PFS can be potentially derived first when solving the PF of the entire AC/DC system. To better clarify this statement, consider for example an AC-PQ converter connected to a power system where MTDC networks are only used to link separate AC grids (i.e., MTDC networks do not connect portions of the same AC grid)[2]. Based on the $P_{\rm bus}$ and $Q_{\rm bus}$ known parameters, a PF algorithm applied exclusively to the AC side of the converter allows deriving the v_d and v_q components of bus. Then, Eqs. (3)–(6) are used to determine the P_{E_b} power in (7). Knowing P_{E_b}, the implicit link (8) between $v_{\rm dc}$ and $i_{\rm dc}$ can be used to determine the PFS of the converter DC-side. Note that the converter unknowns (i.e., v_d and v_q) have been derived without considering any electrical quantity at its DC-side, because P_{E_b} does not depend from a formal standpoint on $v_{\rm dc}$ and $i_{\rm dc}$. This example suggests that the PFS of any AC/DC system could be found by solving the PF of its sub-grids in a given order, which depends on the control functions of the converters and their interconnections. The next section focuses on this key aspect.

III. Power System Partitioner

Partitioning exploits the *reducible* properties of matrices [36], [37]: some matrices, when permuted, become upper (or lower) block-organized. To have a clear picture of the impact of this property on the simulation of mixed AC/DC grids, we assume to compute the PFS of a mixed AC/DC power system using the Newton method. To compute the update, the generic iteration of the Newton method solves the linear problem

$$\overbrace{\begin{bmatrix} \mathbf{J}_{11} & \mathbf{J}_{12} \\ \mathbf{J}_{21} & \mathbf{J}_{22} \end{bmatrix}}^{\mathbf{J}} \overbrace{\begin{bmatrix} \mathbf{\Delta x}_1 \\ \mathbf{\Delta x}_2 \end{bmatrix}}^{\mathbf{\Delta x}} = \overbrace{\begin{bmatrix} \mathbf{r}_1 \\ \mathbf{r}_2 \end{bmatrix}}^{\mathbf{r}} \tag{9}$$

where the $\mathbf{J} \in \mathbb{R}^{N \times N}$ Jacobian matrix is split as a 2×2 block matrix[3], $\mathbf{\Delta x} \in \mathbb{R}^N$ is the vector of the solution updates, and $\mathbf{r} \in \mathbb{R}^N$ is the vector of the residue. Assume that $\mathbf{J}$ is reducible, viz. there exists a permutation matrix $\mathbf{P} \in \mathbb{N}^{N \times N}$ such that $\mathbf{J} = \mathbf{P}\mathbf{A}\mathbf{P}^{-1}$, where $\mathbf{A}$ is a block organized matrix[4]. In particular, (9) can be rewritten as

$$\begin{bmatrix} \mathbf{A}_{11} & \mathbf{A}_{12} \\ \mathbf{0} & \mathbf{A}_{22} \end{bmatrix} \begin{bmatrix} \mathbf{w}_1 \\ \mathbf{w}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \end{bmatrix},$$

where

$$\begin{bmatrix} \mathbf{w}_1 \\ \mathbf{w}_2 \end{bmatrix} = \mathbf{P}^{-1} \begin{bmatrix} \mathbf{\Delta x}_1 \\ \mathbf{\Delta x}_2 \end{bmatrix}, \quad \begin{bmatrix} \mathbf{u}_1 \\ \mathbf{u}_2 \end{bmatrix} = \mathbf{P}^{-1} \begin{bmatrix} \mathbf{r}_1 \\ \mathbf{r}_2 \end{bmatrix}.$$

The LU-factorization of matrix $\mathbf{A}$ and the computation of the solution can be performed in two steps. We first compute $\mathbf{w}_2 = \mathbf{A}_{22}^{-1}\mathbf{u}_2$ and then $\mathbf{w}_1 = \mathbf{A}_{11}^{-1}(\mathbf{u}_1 - \mathbf{A}_{12}\mathbf{w}_2)$. The advantage of partitioning resides in the fact that only $\mathbf{A}_{11}$ and $\mathbf{A}_{22}$ need to be inverted instead of the full matrix $\mathbf{J}$. This results in a boost in numerical efficiency because the size of $\mathbf{A}_{11}$ and $\mathbf{A}_{22}$ is smaller than that of $\mathbf{J}$. Besides, the computational effort of the LU factorization has an (almost) quadratic dependence on the size of the (sparse) matrix. Moreover, regardless of the value of $\mathbf{A}_{12}$[5], the LU factorization of

[2] In the sequel, we discard this hypothesis and introduce the *loop* concept.

[3] This matrix may describe for example two interacting power systems.

[4] Unfortunately, the problem of finding the best permutation matrix (i.e., that makes $\mathbf{J}$ upper (or lower) block organized with block matrices on the main diagonal with minimum and "almost" equal order) has NP-complete complexity. However, there are several algorithms that find a good version of a reducible matrix [22], [36], [37].

[5] When $\mathbf{A}_{12} = \mathbf{0}$ (null matrix), the two power systems are uncoupled.

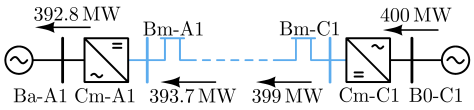

Fig. 2. The block schematic of the Cigrè DCS1 HVDC test systems. This figure is a replica of Fig. 6-25 in [28].

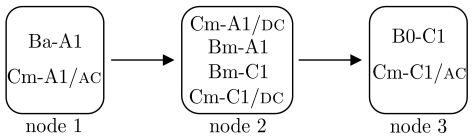

Fig. 3. The dependency graph of the simple DCS1 HVDC mixed power system shown in Fig. 2. Labels inside nodes identify which grids and sections of the AC/DC converters are grouped when computing the PFS. The computation of the PFS of the entire AC/DC grid proceeds from the leaf node to the root.

$\mathbf{A}_{11}$ and $\mathbf{A}_{22}$ (i.e., the block matrices on the main diagonal) can always be performed in parallel, thereby leading to an additional efficiency boost.

The reducible property of the Jacobian matrix can be determined by applying equation ordering methods [36], [37], or by considering the structure of the equations modeling each power system devices and adopting an *ad hoc* topology checker. This tool, which has become a conventional element of modern circuit/power system simulators [22], automatically carries out a topology inspection.

In our specific case, we first focus on the AC/DC converter models listed in Section II. Each of those has characteristics that split the set of modeling equations into two parts. One set comprises Eqs. (3)–(7) and the other includes (8), related to the AC and DC-sides, respectively. For each converter control model in the list, the grid to the left of the arrows of the $(\text{AC} \rightarrow \text{DC})$ and $(\text{DC} \rightarrow \text{AC})$ symbols indicate which set might be potentially solved first. This order depends on the type of converter and its interconnections with the AC/DC grid.

Consider now the simple HVDC link connecting the two separated AC grids in Fig. 2 [28]. We use it to describe the operation of the proposed topology partitioner and to reorganize the equations to be solved to compute the PFS. The Cm-C1 AC/DC converter is an AC-PQ type absorbing $400\,\text{MW}$ and $0\,\text{VAR}$ of reactive power from the B0-C1 AC grid. The Cm-A1 AC/DC converter is a DC-SLACK/AC-Q type that keeps the pole-to-pole voltage of the HVDC link at $400\,\text{kV}$ and absorbs $0\,\text{VAR}$ of reactive power from the Ba-A1 AC grid. Its active power injection in the Ba-A1 AC grid depends on the power losses of the Cm-C1 AC/DC converter, the HVDC line, and the Cm-A1 converter. It is thus easy to realize that

1) the PFS of the B0-C1 AC grid together with the AC section of the Cm-C1 converter can be determined first, independently from the PFS of the remaining sections of the power system.
2) Then, the PFS of the DC section of the Cm-C1 converter, of the HVDC link and the DC section of the Cm-A1 converter can be derived.
3) Lastly, we can compute the PFS of the Ba-A1 AC grid and of the AC section of the Cm-A1 converter.

The topology inspection reveals that the simple AC/DC mixed power system shown in Fig. 2 leads to a reducible Jacobian matrix composed of 3 blocks on the main diagonal.

We underline that the full PFS is exact (from a numerical accuracy standpoint) since the LU-factorized version of the Jacobian matrix used in computing the full PFS is identical to that obtained through partitioning. Besides numerical efficiency improvement due to matrix reduction, another advantage of partitioning is that in the case of numerical convergence issues with the Newton method, additional iterations can be performed but only limited to the partitioned portion of the full system that manifests convergence problems [23], [38]–[40].

The topology partitions can be represented by a directed graph, that we refer to as dependency graph [41]. Each AC/DC converter is a splitting element of the full power system. By referring for instance to the AC-PQ type converter and the (3)-(7) equations, we have shown that these could be solved before (8) if the converter is connected to an AC grid that does not comprise internal portions connected by MTDC networks. Note that, as shown by the arrows in the symbols of the list in Section II, other types of converters (e.g., DC-SLACK/AC-V) indicate that the DC section could be solved before the AC one. We thus define the AC/DC converter model as *unidirectional* splitting; in the dependency graph, each converter constitutes a directed arc that ends in the section to solve first and originates in the other. Nodes thus represent the sub-grids obtained by splitting the full power systems with AC/DC converters.

If the obtained dependency graph does not have loops, the Jacobian matrix is maximally reducible. Otherwise, it is only partially reducible. In this case, sub-grids inside loops must be grouped in a single larger node (grid) in a new dependency graph. This grouping leads to larger blocks in the reduced Jacobian matrix.

The dependency graph of the mixed DCS1 HVDC power system in Fig. 2 is shown in Fig. 3. Since there are no loops, the graph reduces to a tree. The solution sequence goes from the far right leaf node to the left root node. Labels inside nodes list the sections of the power system split by partitioning that are solved together. We underline that the B0-C1 and Ba-A1 AC grids, which may comprise a large number of elements, are separately solved by adopting the Newton iterative method.

A more complex mixed AC/DC system from the same Cigrè report [28], [42] is shown in Fig. 4. At first glance, it is not immediate to understand how this network can be partitioned and, thus, which is the solution sequence. To understand how the topology checker scans the mixed power grid and partitions it, we report in the caption of Fig. 4 the types of AC/DC converters listed in [42]. Through partitioning, we obtain the dependency graph shown in Fig. 5[6] The PFS of the whole AC/DC system is obtained by computing the PFS of each node of the dependency graph, starting from the leaves to the root (i.e., A). In the case of Fig. 5, it is now easy to see that the PFS of the C, D, E, F AC grids can be computed first and independently from each other. Computations can be

[6]We assumed an ideal Cm-E1 DC/DC converter that exchanges constant power. The same holds for Cd-B1 DC/DC converter.

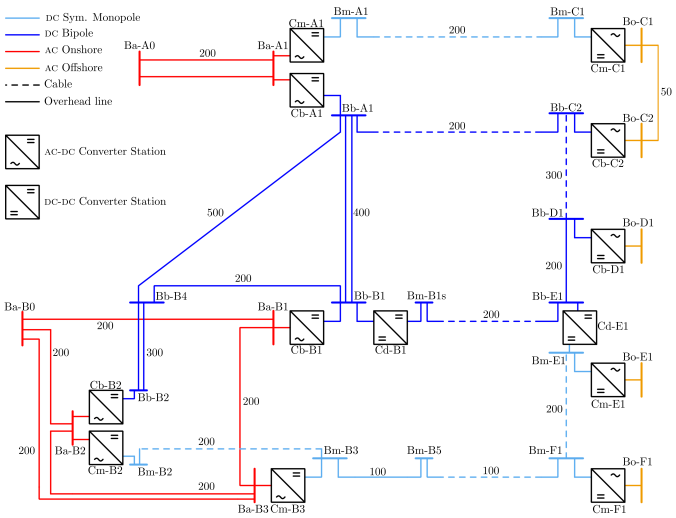

Fig. 4. The block schematic of the Cigrè HVDC test system shown in Fig. 2 of [42]. It comprises respectively 3 and 6 DC and AC grids.
AC/DC converter types – AC-SLACK: Cm-C1, Cb-D1, Cm-E1, Cm-F1 – DC-SLACK/AC-Q: Cm-A1, Cm-B2 – DC-SLACK/AC-V: Cb-A1 – AC-PV: Cb-B2, Cb-B1, Cb-C2, Cm-B3.

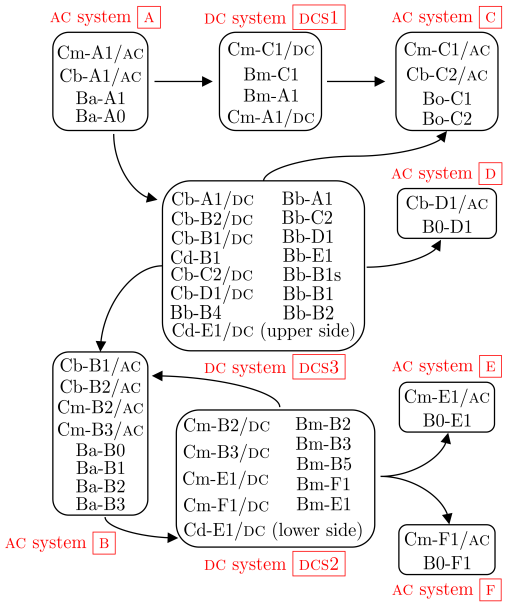

Fig. 5. The dependency graph of the Cigrè HVDC test system shown in Fig. 4. For a description of the meaning of the labels inside the nodes, see the caption of Fig. 3.

carried out concurrently with a parallel solver, regardless of the complexity and extension of each grid. Then, the PFS of the DCS1 DC grid can be derived. By observing the dependency graph, the PFS of the DCS3 DC system cannot be computed until that of the B AC system is determined. However, the PFS of the B and DCS2 grids depend on each other. As a consequence, the dependency graph shows a loop, which means that B and DCS2 must be grouped together, thereby leading to the computation of a unique PFS[7]. Once the loop has been dealt with, the PFS of DCS3 and A grids (and, thus, of the whole power system) can be found.

IV. Cutting Loops

In this section, we describe how loops in the dependency graph can be dealt with to efficiently compute the PFS of complex AC/DC grids. To do so, we also consider AC grids that are meshed by construction and result in irreducible Jacobian matrices. We do this since some AC grids of mixed AC/DC systems may be very large, thereby leading to a burdensome PF computation. To address this issue, several highly specialized algorithms split large graphs into two almost balanced subgraphs by eliminating the almost minimum possible number of edges (sub-optimal solution). KAHIP [43], [44] and METIS [45] are among those. However, if some edges of a graph representing in some way the complex AC grid were cut, the electrical structure of the grid would be modified. We show that by introducing *virtual* elements we can cut loops in the dependency graph and separate meshed large AC grids (and DC grids as well) in smaller sub-grids, while maintaining the final full PFS intact. In other words, the resulting PFS is identical to that obtained without inserting the virtual elements [12], [46].

To describe the operating principle of virtual elements we consider once again the Cigrè HVDC test system in Fig. 4. For space reasons, we only take into account the B and DCS2 nodes of the related dependency graph in Fig. 5 and the two arcs connecting those (i.e., we consider only the arcs and nodes forming the unique loop). In this reduced and simplified case, at the generic Newton iteration we have

$$\overbrace{\begin{bmatrix} \mathbf{J}_B & \mathbf{J}_{B2} \\ \mathbf{J}_{2B} & \mathbf{J}_2 \end{bmatrix}}^{\mathbf{J}_\ell} \begin{bmatrix} \Delta\mathbf{x}_B \\ \Delta\mathbf{x}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{r}_B \\ \mathbf{r}_2 \end{bmatrix}, \tag{10}$$

where the $\mathbf{J}_\ell$ Jacobian is non-reducible. To cut the loop means to directly and deeply act on the electrical configuration of the original mixed AC/DC grid. This action must be performed in a proper way from an electrical perspective.
The loop in the test system of Fig. 4 is generated by the Cm-B2 and Cm-B3 converters that are connected by the Bm-B2/Bm-B3 HVDC link and by the Ba-B2/Ba-B3 AC line. The Cm-B3 converter is of AC-PV type. Consider its equivalent circuit shown in Fig. 1 and assume to remove the transformer and to substitute each both sides of it with two PV generators, referred to as $\mathcal{C}$, which absorb active powers of opposite signs and work at the same voltage magnitude as set by the parameters of the Cm-B3 AC-PV converter. The reactive power at both sides and voltage phase are represented by the $\mathbf{x}_\alpha$ new unknown subvector. The introduction of this new electrical configuration modifies the $\mathbf{J}_\ell$ Jacobian matrix in (10) as

$$\left[\begin{array}{cc|c} \mathbf{J}_B & \mathbf{J}_{2B} & \mathbf{C}_{B\alpha} \\ & \mathbf{J}_2 & \mathbf{C}_{2\alpha} \\ \hline \mathbf{R}_{\alpha B} & \mathbf{R}_{\alpha 2} & \mathbf{1} \end{array}\right] \begin{bmatrix} \Delta\mathbf{x}_B \\ \Delta\mathbf{x}_2 \\ \Delta\mathbf{x}_\alpha \end{bmatrix} = \begin{bmatrix} \mathbf{r}_B \\ \mathbf{r}_2 \\ \mathbf{r}_\alpha \end{bmatrix}. \tag{11}$$

[7]Another arc links DCS3 and DCS2 if the Cm-E1 DC/DC converter is not assumed ideal.

In this new formulation, the important variables are the $\mathbf{r}_\alpha$ residue and $\mathbf{\Delta x}_\alpha$ update. The former tells how the two reactive powers and the phases at both sides of $\mathcal{C}$ mismatch; the latter is the Newton update that modifies the reactive power and voltage phase of both sides of $\mathcal{C}$ to reduce to zero the $\mathbf{r}_\alpha$ residue. When $\mathbf{r}_\alpha = \mathbf{0}$, the $\mathcal{C}$ generators do not alter the original solution, or better said, the solution of the altered mixed AC/DC system coincides with that of the original one, since the power sum of both sides equals zero and voltages are identical. The conclusion is that we have cut the loop while keeping the PFS intact.

At first glance, rather than improving numerical efficiency, the LU-factorization of the matrix in (11) seems to worsen it. However, (11) can be separated in the two equations

$$\begin{bmatrix} \mathbf{J}_B & \mathbf{J}_{B2} \\ & \mathbf{J}_2 \end{bmatrix} \begin{bmatrix} \mathbf{\Delta x}_B \\ \mathbf{\Delta x}_2 \end{bmatrix} = \begin{bmatrix} \mathbf{r}_B \\ \mathbf{r}_2 \end{bmatrix} - \begin{bmatrix} \mathbf{C}_{B\alpha} \\ \mathbf{C}_{2\alpha} \end{bmatrix} \mathbf{\Delta x}_\alpha \tag{12}$$

and

$$\left(\mathbf{1} - \begin{bmatrix} \mathbf{R}_{\alpha B} & \mathbf{R}_{\alpha 2} \end{bmatrix} \begin{bmatrix} \mathbf{J}_B & \mathbf{J}_{2B} \\ & \mathbf{J}_2 \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{C}_{B\alpha} \\ \mathbf{C}_{2\alpha} \end{bmatrix} \right) \mathbf{\Delta x}_\alpha = \mathbf{r}_\alpha - \begin{bmatrix} \mathbf{R}_{\alpha B} & \mathbf{R}_{\alpha 2} \end{bmatrix} \begin{bmatrix} \mathbf{J}_B & \mathbf{J}_{2B} \\ & \mathbf{J}_2 \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{r}_B \\ \mathbf{r}_2 \end{bmatrix}. \tag{13}$$

The matrix in (12) is upper-block organized and can be efficiently LU-factorized while retaining the dimensions of the original problem. The size of the matrix in (13) depends on the number of cutting elements and thus on the ability and efficiency of KAHIP or METIS to find a minimum cut of the dependency graph. Equations (12) and (13) can be solved in a very efficient way by the two-level Newton algorithm [11], [21], [47], [48].

The numerical advantage of the loop cutting approach lays in the fact that, since the cost of the LU-factorization is $\mathcal{O}(N^\beta)$ (where N is the size of the sparse matrix and $\beta \in (1.8, 2.5)$ is empirically estimated), if the problem is split in M smaller problems of N/M size, we obtain that the LU-factorization cost becomes $\mathcal{O}(M\,(N/M)^\beta)$ with a net gain in numerical efficiency of $M^{(\beta-1)}$.

We applied the loop cutting technique to the simple case of the Cigrè HVDC test system shown in Fig. 4, as well as to large and complex AC grids, isolated or interconnected (either internally or externally to other AC grids) through MTDC grids. AC/DC converters and AC transformers are used as splitting elements in the dependency graph. Contrary to the former, the latter introduce bidirectional arcs. The sub-networks connected by transformers constitute the nodes of the dependency graph. This organization reveals that the high-voltage backbone transmission system is often the node that better partitions the graph. The chosen graph splitting algorithm removes the minimum set of arcs (i.e., transformers) to split a grid, which is then solved with a two-level Newton method. All the examples reported in the next section exploit this partitioning technique.

V. Numerical results

We considered several benchmarks of mixed AC/DC systems from the literature. In the following, we specify how each benchmark was implemented and refer to the works which define their parameters and operating conditions. Where needed, we guessed some parameters missing from the references.
This paper shows the schematics of only two simple test systems. We cite the papers whose figures include the more complex power system schematics not reported here for space reasons.
We computed the PFS of each test system with the sequential solvers MATACDC [31], implemented in MATLAB and based on MATPOWER [49], and POWERMODELSACDC.JL [33], implemented in JULIA [50] and based on POWERMODELS.JL [32], and with our proposed method. Computations by the latter were performed with our simulator PAN[8]. All simulation were performed on a 2.3 GHz Intel i7 processor running Linux Mint 18. Some run statistics and comparisons are reported in Table I. The "AC-IT" and "DC-IT" columns describe the total number of iterations performed respectively by the AC and DC solvers implemented in MATACDC. The "ITJ" column reports the CPU time of JULIA. The "IT" column describes the total number of iterations carried out by our proposed approach[9]. We comment on every single run in the next sub-sections.
Fig. 6 shows how the relative error in computing the PFS of some simulated benchmarks changes with the number of iterations by using the proposed method. It is easy to see that traces cluster in two sets and the relative errors quickly fall to the relative precision of the arithmetic-logic unit at $2.22044605 \times 10^{-16}$ (≈ -15.65 in $\log_{10}$ base) after a few iterations.

TABLE I
RUN STATISTICS

CPU times in ms. AC-IT and DC-IT: number of iterations of the AC and DC solvers of MATACDC. ITJ: CPU time of JULIA. IT: number of iterations of the proposed unified solver.

	MATACDC			JULIA	PAN	
	CPU	AC-IT	DC-IT	ITJ	CPU	IT
case5	36	6	3	13	3	5
case5@100%	38	6	3	24	3	5
case5@600%	68	11	5	96	7	7
nordic-32	104	10	3	30	25	6
ieee14-ovl	5590	5310	1836	8188	74	1405
ieee14-hvac	57	12	3	20	5	4
rts-24	73	13	2	26	15	6
cigrè	42	8	3	14	9	5
gb-grid	1879	9	3	650	139	6
usa-grid	$\gg$ 8750	—	—	—	2830	7

A. The 5 AC buses, 3 DC buses, 3 AC/DC converters system

The first benchmark we consider is presented in [3]–[5]. It was used to test the algorithm in [3], which was implemented

[8]Our simulator PAN is mostly written in C and C++. The user can choose the sparse matrix package among SPARSE, CSPARSE, and SUPERLU. The handling of multi-threading is based on custom software that optimizes overhead in execution context switching, a drawback that may limit the use of multiple-threads in very frequent but brief tasks. PAN automatically generates C source code and compiles it (possibly once and for all) in shared-libraries to minimize execution times of user-defined behavioral devices [29], [30]. A similar software paradigm is also implemented in Julia [50], which was used to explore power flow formulations in [32]. PAN can be downloadded from the url https://brambilla.deib.polimi.it.

[9]The number of Newton iterations varies for each partitioned portion of the grid to be solved. Table I reports the maximum number.

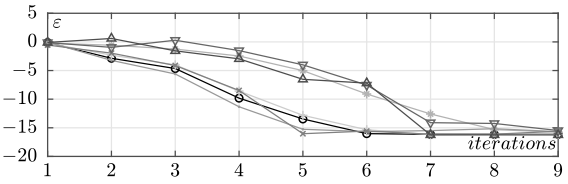

Fig. 6. Relative error ε (in $\log_{10}$ base) in computing solutions of some of the test cases in Table I versus the number of iterations of the proposed approach. `case5`: ○, `case5@100%`: +, `case5@600%`: ∗, `nordic-32`: ▽, `ieee14-ovl`: ●, `rts-24`: ×, `gb-grid`: △.

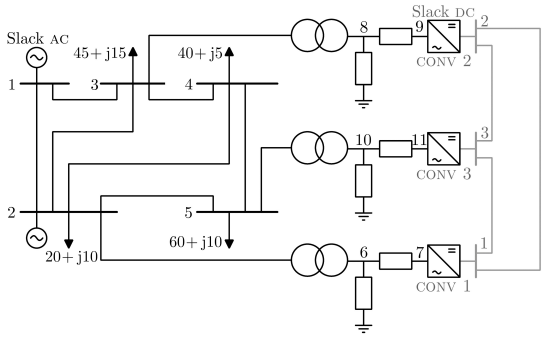

Fig. 7. The schematic of the 5 AC buses, 3 DC buses, 3 AC/DC converters system test system (`case5`). Overloading increases the active power of all loads and that of the CONV1 and CONV2 PQ AC/DC converters.

TABLE II
AC LINE PARAMETERS

Lines are labelled with the "Ln" prefix, integers indicate connected buses,"r", "x" line series resistance and inductance, "b" susceptance to ground. The lines employ a Π model. The '/AC' and '/DC' tags after each parameter denotes an AC or DC line. Values are in [pu], $v_{\text{base}} = 350\,\text{kV}$, $p_{\text{base}} = 100\,\text{MW}$.

	Ln12	Ln13	Ln23	Ln24	Ln25	Ln34	Ln45
r/AC	0.02	0.08	0.06	0.06	0.04	0.01	0.08
x/AC	0.06	0.24	0.18	0.18	0.12	0.03	0.24
b/AC	0.06	0.05	0.04	0.04	0.03	0.02	0.05
r/DC	0.052	0.073	0.052	–	–	–	–

in the MATACDC simulator described in [4], [5]. Its schematic is shown in Fig. 7 and we refer to it as `case5`. Table II shows the parameters of the 5 AC lines and of the 3 DC lines, Table III lists the power of loads and generators, and Table IV defines the parameters of the AC/DC converters in `case5`. The PFS computed with the approach proposed in this paper matches "exactly" (relative precision of 10^{-6} used for each benchmark in this section) that of MATACDC.

TABLE III
POWER LOADS/GENERATIONS

Values are in [pu]. 'g', 'l', 'P', 'Q' and 'V' labels indicate respectively generation, load, constant active power, constant reactive power and constant modulus of the voltage at which the PV or slack generator is connected. $v_{\text{base}} = 350\,\text{kV}$, $P_{\text{base}} = 100\,\text{MW}$.

	Bus1	Bus2	Bus3	Bus4	Bus5
Pg	slack	0.4			
Vg	1.06	1			
Pl		0.2	0.45	0.4	0.6
Ql		0.1	0.15	0.05	0.1

TABLE IV
CONVERTER CHARACTERISTICS

VCS1: AC-PQ type, $P = 60\,\text{MW}$, $Q = 40\,\text{MVA}$. VCS2: DC-SLACK/AC-V, $v_{\text{DC}} = 345\,\text{kV}$, $v_{\text{AC}} = 345\,\text{kV}$. VCS3: AC-PQ type, $P = -35\,\text{MW}$, $Q = -5\,\text{MVA}$. The following parameters are identical for the 3 converters.

R_{tf}	X_{tf}	B_{f}	R_{c}	A_{ac}	B_{ac}	C_{ac}
1.7854	133.43	$74.522\,\mu$	0.1190	$1.103\,\mu$	88.7	2.285

The `case5` test system was also used in [13] to show how the number of iterations of the original sequential method implemented in MATACDC increases (see Fig. 6 in [13]) when the power of the loads and the PQ AC/DC converters gradually increases until $+600\%$. We did the same by progressively overloading the `case5` test system. Results are shown in Table I for nominal load, $+100\%$, and $+600\%$ overloads. In the $+600\%$ overloaded case, the proposed method converges to the PFS of the full system in 7 iterations, while MATACDC requires 11 and 3 iterations of the AC and DC solver respectively. This means that the same AC sub-system is solved 3 times. The difference in CPU time in the two cases is contained but proves that the proposed method is more efficient. This relative gain becomes important when a large number of PFSs must be computed in succession as in optimal power flow (OPF) simulations or where systems parameters such as the overloading index are swept on a fine mesh (as shown in Section V-C).

B. NORDIC-32 *and* RTS-24 *systems with* HVDC *links*

We considered the NORDIC-32 system with an embedded MTDC system shown in Fig. 24 of [51]. A similar benchmark was also used in [7]. Data of the original version of the NORDIC-32 system can be found in [52]. The VCS converters and DC line characteristics are listed in Table A3 of [51]. The functions implemented by each AC/DC converter are defined on page 22 of [51]. The PFS obtained with our method "exactly" matches the original one also in this case.

The schematic of a modified version of the RTS-24 system is shown in Fig. 7 of [5]. Two MTDCs connect two RTS-24 systems. AC/DC converters operate so that power flows from one system to the other. The proposed partitioner splits the modified RTS-24 system into 3 sub-systems. It solves the system injecting power through the MTDCs, then the two MTDCs, and finally the RTS-24 system that absorbs power.

C. Two versions of the IEEE14 *power system*

We considered two modified versions of the IEEE14 power system. In the former, shown in Fig. 8 and labeled as `ieee14-ovl` in Table I, the line between bus 4 and bus 5 is substituted by an HVDC link, as described in [2], [14]. This version was used in [15] to show convergence issues of the sequential method. The authors progressively increased the power setpoint of the PQ AC/DC converter connected at bus 5, starting from $50\,\text{MW}$ in steps of $5\,\text{MW}$ until $475\,\text{MW}$ where there is no solution. We did the same but with a step of $1\,\text{MW}$. CPU times show that the proposed method largely outperforms both MATACDC and JULIA. The CPU time is higher than in

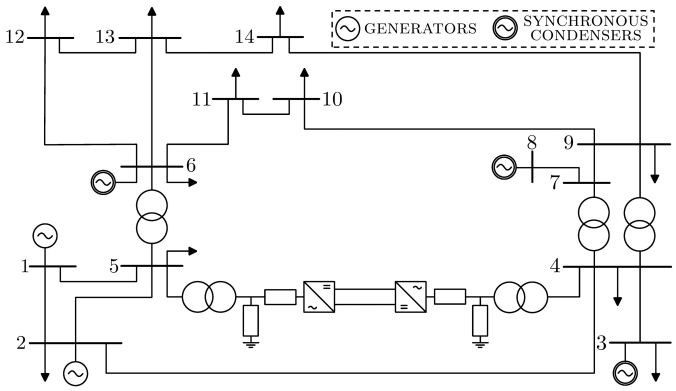

Fig. 8. The modified schematic of the IEEE14 power system, that we label as `ieee-ovl`.

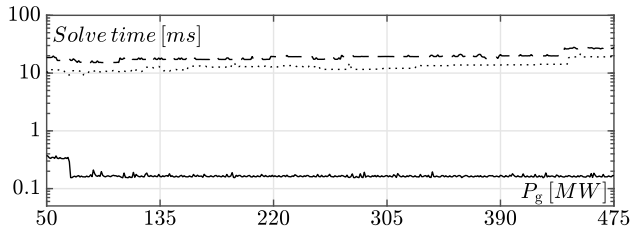

Fig. 9. Times to solution for the `ieee-ovl` system as a function of the power setpoint of the PQ AC/DC converter connected at bus 5. The solid line refers to our simulator PAN, while the dashed and dotted lines refer respectively to JULIA and MATACDC.

previous cases since the PFS of the same power system was repeatedly computed during parameter sweeping. CPU times indicate that previous cases suffer from overheads in PAN, for example due to algorithm initializations.
Figure 9 shows a comparison between the CPU times required by our simulator, MATACDC and JULIA. By carefully watching at the CPU times of MATACDC and JULIA, we see that they increase versus overloading by a 2 factor. This does not happens with JULIA. During overloading sweeping PAN never exceeds 5 iterations and largely outperforms the other two tools.

The second version of the IEEE14 is the high-voltage/low-frequency power system described in [8], labeled as `ieee14-hvac` in Table I. Its schematic is shown in Fig. 6 of [8]. The modification mainly consists of HVDC links and back-to-back AC/DC converters to connect two asynchronous AC grids. The AC/DC converters and the 3 transformers in the network partition the system. Despite our efforts, we could not find the electrical characteristics of the AC and DC cables adopted in the test system. We thus set $r = 0.0843\,\omega/\mathrm{km}$, $l = 0.2526\,\mathrm{mH/km}$, $c = 0.1837\,\mu\mathrm{F/km}$ for the HVAC system at $500\,\mathrm{kV}$ and $r = 0.0114\,\Omega/\mathrm{km}$, $l = 0.9356\,\mathrm{mH/km}$, $c = 0.0123\,\mu\mathrm{F/km}$ for the HVDC systems at $320\,\mathrm{kV}$. Since converter parameters were also missing, we chose $A_{\mathrm{ac}} = 1.103 \times 10^{-6}$, $B_{\mathrm{ac}} = 88.7$ and $C_{\mathrm{ac}} = 2.285$.

D. Larger MTDC systems

The last two benchmarks considered are the Cigrè HVDC test system, already shown in Fig. 4 and the more complex MTDC system described in [53]. The characteristics of the Cigrè HVDC test system are reported in [42] and [28]. To the best of the authors' knowledge, both these papers do not report a precise PFS obtained with specific working conditions. The PFS reported in Fig. 4 of [28] is "approximate" as explicitly stated. However, this test system was also used in [4] (Fig. 11) as a benchmark to test the sequential solver. The converter parameters are not fully given in [28] and are not complete in [4]. We thus omitted these "unknown" parameter values and replicated the simulation in MATACDC to compare simulation results, which proved to be "exact".

The benchmark shown in Fig. 1 of [53] was specifically developed to test mixed PF solvers. Analogously to the previous case, some system parameters are reported in the Tables of the same paper, but full details on the AC/DC converters are missing. We thus used simplified models of the AC/DC converters. We have augmented the system shown in Fig. 1 of [53] by connecting in one case the grid model of the Great Britain to the Ba-A0 AC bus. In another case, we connected the synthesized 70000 bus model (`ACTIVSg70k`) of the North American grid to the Ba-B0 AC bus. These two scenarios are respectively referred in Table I as GB-GRID and USA-GRID. In both cases, loops in the dependency graphs were split as previously detailed by using transformers between transmission systems at different voltage levels as cutting elements. Due to some issues with the MATACDC and POWERMODELSACDC.JL toolboxes, we could determine the CPU time needed to compute the PFS of the USA-GRID case only with our approach. Considering that the MATPOWER tool, which MATACDC is based on, solves the USA-GRID alone in $8.75\,\mathrm{s}$, it is possible to conclude that the adoption of partitioning in computing the PFS leads to a significant boost in simulation efficiency in this case as well.

VI. Conclusions

We presented a unified power flow algorithm for large and complex mixed AC/DC power systems based on the partitioning of power grids, a version of the two-level Newton method, and the MNA formulation. It belongs to the class of *unified* methods, even if partitioning may erroneously induce to categorize it among *sequential* methods. Our approach relies on the MNA due to its superiority in handling basic modeling elements. It is enhanced with several fall-back methods to aid convergence in troublesome systems configurations. It can be applied to combined AC/DC grids, where power flows in possibly asynchronous AC grids connected via HVDC/MTDC links. Several tests were executed comparing the performance of the proposed approach to other available numerical tools.

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