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Stability Boundaries of Wide-Input-Range COT Buck Converters With Ripple Compensation

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ABSTRACT In this paper, we focus on instability issues of a wide-input-range Constant ON-Time buck converter. A transconductance stage in the control path that implements ripple compensation characterizes the architecture of this switching circuit. On the whole, decision rules, that heavily influence stability, govern the dynamical evolution of the converter. We show the onset of sub-harmonic oscillations and pulse-bursting caused by the presence of hysteresis in the regulation comparator. Operational boundaries are provided both in analytical and numerical form. They easily support the designer in choosing the converter parameter values. Theoretical results are verified against SIMetrix/SIMPLIS and MPLAB® Mindi™ simulations for a case study involving a commercial adjustable-frequency, synchronous buck regulator featuring an adaptive ON-time control architecture. A good agreement is obtained, as shown.

INDEX TERMS Circuit stability, DC-DC power converters, nonlinear dynamical systems, switching systems.

I. INTRODUCTION

CONSTANT ON-time control is an attractive choice for the implementation of buck converters. It can operate under a very wide input voltage range, mostly because the variable-frequency characteristic of Constant ON-Time (COT) alleviates minimum controllable ON-time limitations towards the upper value of the input range, faced by fixed-frequency architectures, such as peak-current-mode or voltage-mode ones. However, the simplest version of COT control, where the valley of the output voltage ripple waveform is regulated, inherently suffers from poor output control against input voltage variations. This, known as line regulation, is also influenced by external components values such as inductance, and equivalent series resistance (ESR) of the output capacitor. This issue is well-known in the industry [1]. Basic COT control poor line regulation becomes even more problematic in LED driver applications, where several control "workarounds" might be required to sufficiently stabilize the average value of the inductor current against input voltage variations [2].

Stabilization techniques of the DC output voltage (or current, in the case of LED drivers) have been introduced to the basic form of the COT control. Many of those techniques consist in the addition of an integrating stage which adapts the switching-threshold value of the regulation comparator, while the average output variable value is being regulated at the feedback node. Practical examples of this technique are countless (e.g., [2]–[4] just to cite a few). A conceptual implementation of the DC-improved COT Buck DC-DC converter, that applies the contribution in [3], is shown in Fig. 1.

In many large-volume applications, the input voltage range is wide enough to push the COT Buck converter to operate both at very low or very high duty cycle values. For example, some industrial or automation applications may require an 8-32 V input range, while the 5 V lower value (or even below) and the 40-42 V upper value are not uncommon for automotive 12 V systems.

It was found, both experimentally and from circuit simulations, that the architecture described in Fig. 1 can experience

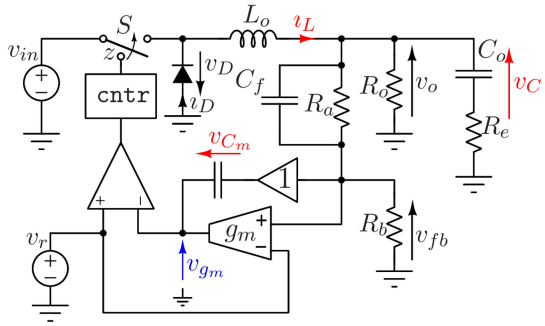

FIGURE 1. The schematic of COT converter. The circuit states variables are the v_C and v_{C_m} voltages and the i_L current. The z signal at the output of the cntr block rules the opening/closing of the S switch.

some stability issues at high duty cycle values, especially when the converter nominal switching frequency is intentionally lowered to maximize the duty cycle range achievable under minimum ON-time limitations. Instability is experienced in terms of pulse-bursting [5]–[8], viz. sub-harmonic oscillations.

Avoiding pulse-bursting in steady-state operating conditions is necessary to prevent excessive ripple amplitudes in the inductor current and output voltage waveforms. Their undesirable consequences may include degraded efficiency, reduction of the output current capability because of premature engagement of current limit protections, and, most important, violation of the steady-state output voltage ripple specifications (output voltage noise). Unpredictable electromagnetic emissions might also be a concern. These are well-known design aspects and researches are still working to propose new analysis techniques and possible technical solutions [9]–[12]. The issue of pulse-bursting was recently analyzed by these authors for the simplest form of COT buck converter control, i.e., without the transconductance stage depicted in Fig. 1, that translates the v_{fb} feedback voltage into v_{g_m}. In the model adopted in that case, two state variables only governed the circuit dynamics. A straightforward novel sufficient condition, overcoming in terms of reliability the popular one presented in [13], to prevent the appearance of the pulse-bursting was presented in [14].

The contribution of this paper aims at providing a quantitative evaluation of the stable operating region of a DC-improved COT control architecture working in continuous current mode (CCM).[1] An approach similar to that adopted in [14] is used here with the addition of handling a "difficult" three-dimensional state-space. Three operational boundaries to check stability are derived accounting also for the presence of hysteresis in the regulation comparator. In particular, the appearance of pulse-bursting is discussed in terms of the

1. In continuous current mode (CCM) current flows continuously in the L_o inductor (see Fig. 1) during the entire switching cycle in steady state operation. On the contrary, discontinuous current mode (DCM) is characterized by the inductor current being zero for a portion of the switching cycle.

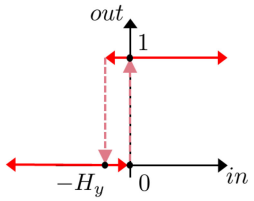

FIGURE 2. Asymmetric hysteretic input/out characteristic of the regulation comparator.

input voltage as a function of significant circuit parameters whose value depends on both the converter architecture (*internal parameters*) and the specific application (*external parameters*) being under user control.

Theoretical results are compared against SIMetrix/SIMPLIS and MPLAB® Mindi™ simulations for a case study involving a commercial adjustable-frequency, synchronous buck regulator featuring an adaptive ON-time control architecture [15]. An excellent agreement is obtained, as shown.

II. THE COT CONVERTER CONTROL STRATEGY

The dynamic evolution of the COT converter state variables (v_C, i_L, v_{C_m}) is governed at first by the following control algorithm, implemented in the cntr block, fed by the regulation comparator whose input-output function is shown in Fig. 2.

Step 1: Any time $v_r - v_{g_m}$ gets positive, the output of the comparator becomes positive, the controller catches the positive edge of this signal, and the S switch is closed for the Δt_{ON} *fixed* time interval (ON-phase). In adaptive COT control (i.e., pseudo constant-frequency in CCM operation and low losses), the duration of this interval is given by

$$\Delta t_{\text{ON}} = \frac{k}{f_{sw}} \frac{v_o}{v_{in}}, \tag{1}$$

where v_o is the output voltage, v_{in} is the input voltage, f_{sw} is the maximum nominal switching frequency, and $k \in [1, k_{\text{MAX}}]$. k takes into account an optional adjustment of the desired switching frequency below its maximum nominal value, and it is under user control (typically implemented by adding or changing external resistors).

Step 2: At the end of the ON-phase, S is opened and is kept open for the $\Delta t_{\text{OFF}}^{\text{min}}$ *fixed* time interval (minimum OFF-phase).

Step 3: At the end of the $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\text{min}}$ time interval, the controller checks the output of the comparator that is typically characterized by hysteresis as shown in Fig. 2. If $v_r - v_{g_m} < -H_y$, the S switch remains open (OFF-phase) until the condition at Step 1 becomes true. The overall duration of the OFF-phase is $\Delta t_{\text{OFF}} \geq \Delta t_{\text{OFF}}^{\text{min}}$. Otherwise, if $v_r - v_{g_m} > -H_y$, i.e., the output of the comparator is still positive, the S switch is closed again and a new ON-phase starts immediately.

There could be several reasons for adding hysteresis to the regulation comparator. For example, one may want to ensure a more "valid" triggering signal for the Δt_{ON} timer,

and more generally to improve the switching noise immunity of the regulation circuit. However, as it will be appreciated in the following, a too large hysteresis window can introduce undesirable side effects, and other methods for noise immunity enhancement should rather be considered.

$\Delta t_{\text{OFF}}^{\min}$ is necessary in practical designs for various reasons, which include reliable implementation of anti-cross conduction control of the power switches, the recharge of the bootstrap capacitor in N-channel high-side topologies and the acquisition of the current signal during the OFF-phase for circuit protection purposes.

The role of the D diode in Fig. 1 is to avoid a negative $\imath_L$ current. Actually, in modern architectures such as synchronous buck converters, to enhance converter efficiency the diode is replaced by a low-side MOSFET which is operated as a synchronous rectifier. Consequently, "diode" D, that actually works as a controlled switch in perfect "diode emulation", is modeled as a piecewise-linear ideal component with $\imath_D = 0$ for $v_D \leq 0$ and $v_D = 0$ for $\imath_D \geq 0$. Furthermore, acting on the limitation of the reverse current of this device, it is possible to have $\imath_L \geq \imath_\zeta$ with $\imath_\zeta \leq 0$. The $\imath_\zeta$ boundary can be set to very negative values if reverse current limit is not implemented by the low-side synchronous rectifier switch.

A. RIPPLE INJECTION

In the schematic in Fig. 1, the C_f capacitor in parallel with R_a is used to implement output *ripple injection* [15]. This technique is used when the ripple of the v_{fb} feedback voltage may be too small to be sensed reliably by the internal control circuit. This is due to output capacitors with low ESR, yet large enough to maintain small phase shift between the $\imath_L$ ripple and the v_o ripple, such that stable operation could still be attained (in absence of comparator hysteresis). More in detail, by referring to the DC component of v_o as $\langle v_o \rangle$, it is possible to write

$$v_{fb} = \frac{R_b}{R_a + R_b} \underbrace{\frac{R_o(\imath_L R_e + v_C)}{R_e + R_o}}_{v_o}, \tag{2}$$

if C_f is not present, or

$$v_{fb} = \frac{R_b}{R_a + R_b}\langle v_o \rangle + \underbrace{v_o - \langle v_o \rangle}_{v_o \text{ ripple}} = v_o - \frac{R_a}{R_a + R_b}\langle v_o \rangle \tag{3}$$

if C_f is inserted, as in this case. Ripple injection can be achieved since the passive network made up of R_a, R_b, and C_f implements a zero-pole transfer function from v_o to v_{fb}. The DC gain of this transfer function is $\frac{R_b}{R_a+R_b}$, whereas the gain is approximately unitary for frequency values in the order of the expected working frequency of the COT converter. In this way, the ripple of the v_o output voltage is not altered by the feedback network.

The voltage across the C_f capacitor can be not inserted among the state variables since its dynamics is typically very slow w.r.t. the characteristic times of the overall circuit. By removing C_f, the effect of ripple injection can be emulated by setting $v_{fb} = v_o$ and replacing v_r with $\hat{v}_r = v_r \frac{R_a+R_b}{R_b}$. With this simplification, a three-state variable equivalent circuit is obtained that is governed by the rules at `Step 1-4` by properly scaling v_r. This will be done in the following.

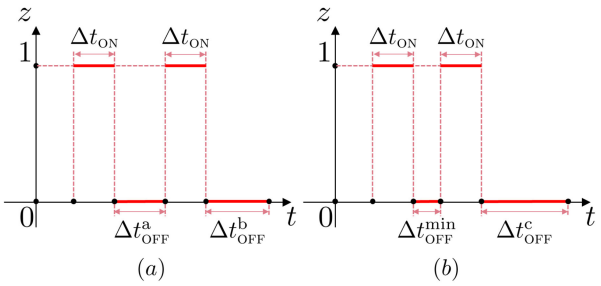

FIGURE 3. Time evolution of the z signal at the output of the `cntr` block. A γ_2 periodic orbit exhibits two different OFF-phases that may last both more than $\Delta t_{\text{OFF}}^{\min}$ (a), or one of them can be *minimum*, i.e., lasting exactly $\Delta t_{\text{OFF}}^{\min}$ (b).

III. STABILITY BOUNDARIES

In dynamical-system theory, when considering the *stability* of *attractors*, one deals with the peculiarity of a set of points in state space that attract all neighboring trajectories from some region named the attraction region.

In switch-mode converters *instability issues* can take different forms, among which are pulse-bursting and subharmonic oscillations. When these occur, the γ_1 limit-cycle characterizing the periodic steady-state of the circuit, typically and desirably made up of a single ON-phase and OFF-phase, changes its structure. In the simplest case, such limit cycle starts exhibiting two ON-phases and two OFF-phases (thus becoming a γ_2 limit-cycle), and this implies the presence of pulse-bursting. This phenomenon is basically governed by the decision process implemented in the `cntr` block.

In Fig. 3, the time evolution of the z signal at the output of the `cntr` block in Fig. 1, which governs the opening and closing of the S switch, is shown for two different pulse-bursting limit cycles. Figure 3(a) refers to a γ_2 limit-cycle exhibiting two OFF-phases of different duration and both lasting more than $\Delta t_{\text{OFF}}^{\min}$. In terms of the control scheme described in Section II, after `Step 1` and `Step 2`, at the beginning of `Step 3`, one gets $\hat{v}_r - v_{g_m} < -H_y$ and the S switch remains open for $\Delta t_{\text{OFF}}^{\text{a}}$ until $\hat{v}_r - v_{g_m}$ gets positive. Then the sequence is repeated once more and `Step 3` lasts $\Delta t_{\text{OFF}}^{\text{b}}$. The γ_2 limit-cycle shown by Figure 3(b) corresponds to the case in which, at the beginning of `Step 3`, one gets $\hat{v}_r - v_{g_m} > -H_y$ and a new ON-phase starts immediately, viz. the first OFF-phase is *minimum* since it lasts $\Delta t_{\text{OFF}}^{\min}$. In this paper, whenever a limit cycle exhibits at least a minimum OFF-phase, it is referred to as a *minimal* limit cycle.

In the following, the appearance of γ_2 limit cycles is analyzed as a function of the v_{in} input voltage, which is the operating parameter that exhibits the widest variation range, as anticipated in the Introduction. As a function of v_{in}, the γ_2 limit cycle appears if one of the constraints introduced hereafter is not fulfilled.

A. PERIOD DOUBLING

The first constraint is related to a period-doubling bifurcation undergone by $\boldsymbol{\gamma}_1$ cycles. For COT buck converters in which the C_m capacitor is not present, viz. the state space is a plane, the occurrence of this bifurcation, leading to a non-minimal $\boldsymbol{\gamma}_2$ cycles, can be avoided by resorting to a proper sufficient condition recently presented in [14]. This condition, which generalizes the well-known classical one [13], is no longer valid when the state-space is three-dimensional since it grounds on the assumption that, in a two-dimensional autonomous dynamical system, such as the mentioned version of the COT converter, the trajectory can not intersect. This is not true in the three-dimensional case. As a consequence, to properly locate this period-doubling bifurcation for the purpose of avoiding it, it is necessary to resort to its standard *test function*, i.e., monitoring the $\{\lambda_i\}$ Floquet multipliers of the $\Phi_{\boldsymbol{\gamma}_1}$ monodromy matrix of $\boldsymbol{\gamma}_1$ limit cycles, and looking for one of those becoming equal to -1 [16], [17]. To this aim it is necessary to (numerically) derive both $\boldsymbol{\gamma}_1$ and $\Phi_{\boldsymbol{\gamma}_1}$. In the specific case of a COT buck converter this is complicated by the switching nature of the circuit, and resorting to the saltation matrix operator is mandatory [18], [19]. Furthermore, since the overall duration of `Step 1` and `Step 2` is fixed, the systems exhibits also a *delayed* switching event that happens at the end of these periods, and thus an extension of the canonical saltation matrix operator must be used [20]. In terms of the v_{in} supply voltage, for a given set of circuit parameter values, one has to set

$$v_{in} > v_{in}^{\mathrm{PD}} | \left\{ \lambda_i \left(v_{in}^{\mathrm{PD}} \right) \right\} \ni -1. \tag{4}$$

It is not possible to derive an analytical expression of v_{in}^{PD} but in Section V it is shown how a reliable approximation of this stability boundary can be numerically achieved. The strong value of the proposed approximation is that it predicts very well the true bifurcation value of v_{in} and it can be derived without computing the $\boldsymbol{\gamma}_1$ limit cycles. It grounds on an accurate estimate of the circuit state variables at the beginning of the ON-phase for a $\boldsymbol{\gamma}_1$ limit cycle.

B. HYSTERESIS CONDITION

The second constraint is related to the switching condition $\hat{v}_r - v_{g_m} > -H_y$ verified at the beginning of `Step 3`. The effect of the comparator hysteresis reveals if in the $\Delta t_{\mathrm{ON}} + \Delta t_{\mathrm{OFF}}^{\min}$ time interval its input does not trespass (decreasing) the $-H_y$ threshold. To derive an approximate condition corresponding to avoid forcing a sudden ON-phase immediately after the minimum OFF-phase, it is sufficient to ensure that a time instant $t_{H_y} \in (t_{\mathrm{ON}}, t_{\mathrm{ON}} + \Delta t_{\mathrm{ON}} + \Delta t_{\mathrm{OFF}}^{\min})$ exists such that

$$\hat{v}_r - v_{g_m}\left(t_{H_y}\right) = -H_y, \tag{5}$$

where $t = t_{\mathrm{ON}}$ represents the beginning of the ON-phase.

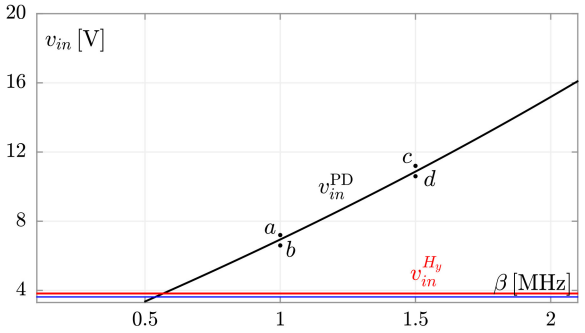

FIGURE 4. According to the parameter values in Table 1, $\beta \equiv \frac{g_m}{C_m} \approx 0.786$ MHz. In *a* and *c* the COT converter is stable whereas pulse-bursting is observed in *b* and *c* since the constraint (4) is no longer fulfilled. The dashed blue line corresponds to $v_{in}^{\mathrm{ST}} = 3.62$ V. The stability boundary (2) (in red) is constant since it does not depend on β. In particular, $v_{in}^{H_y} = 4.08$ V.

TABLE 1. COT converter circuit parameter values.

Name	Value	Name	Value	Name	Value
C_o	470 µF	R_e	45 mΩ	k	[1, 3]
L_o	12 µH	H_y	5 mV	v_r	601 mV
R_a	10 kΩ	R_b	2.21 kΩ	f_{sw}	800 kHz
$\Delta t_{\mathrm{OFF}}^{\min}$	230 ns	g_m	22 µS	C_m	28 pF
R_o	1.1 Ω	C_f	10 nF	R_p	25 mΩ

A reliable approximation of this operational boundary in terms of v_{in} can be written as

$$v_{in} > -\frac{kR_e\hat{v}_r^2\left(R_o + R_p\right)}{f_{sw}L_oH_y(R_e + R_o) - kR_eR_o\hat{v}_r} \equiv v_{in}^{H_y}. \tag{6}$$

In Section V we show in detail how this expression is derived. Violating Equation (6) leads to the creation of minimal γ_2 limit cycles corresponding to Fig. 3(b).

It is worth noticing that, at least for the chosen level of accuracy, $v_{in}^{H_y}$ does not depend on β hence this stability boundary would be identical even in case the C_m capacitor were not present, i.e., without the transconductance stage depicted in Fig. 1.

C. NUMERICAL RESULTS

In Fig. 4 the input-voltage stability boundaries in (4) and (6) are shown as a function of $\beta = g_m/C_m$ (the values of the circuit parameters are reported in Table 1). Such curves are significant only if v_{in} is greater than the Under-Voltage Lock-Out (UVLO)[2] threshold of the particular device, and if the output regulation can still be maintained, viz. maximum duty cycle limitations are not coming into the picture.

The capability of maintaining output regulation corresponds to avoid the control saturation at steady-state. In terms of v_{in}, it translates into identifying a threshold value of the supply voltage such that, exactly at the end of the minimum OFF-phase, the $\hat{v}_r - v_{g_m}$ signal gets positive and

2. The purpose of UVLO is to prevent the device from attempting operation under a voltage level where some internal blocks may not function properly. In case the device is driving power MOSFET (either internal or external), the UVLO also ensures adequate gate drive voltage level to the MOSFETs such that their ON-state resistance is low enough to prevent excessive power dissipation and/or poor conversion efficiency.

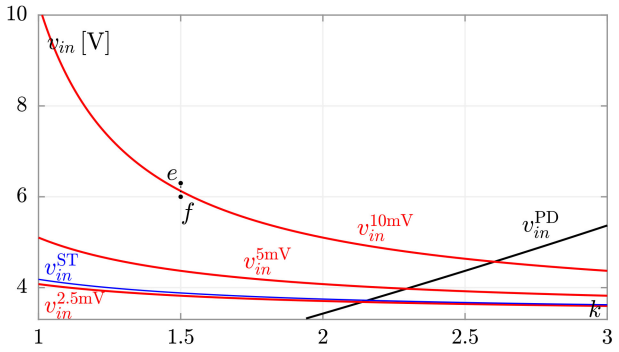

FIGURE 5. The v_{in}^{Hy} stability boundary is shown for $H_y \in \{2.5, 5, 10\}$ mV, respectively by the red curves $v_{in}^{2.5\text{mV}}$, $v_{in}^{5\text{mV}}$, and $v_{in}^{10\text{mV}}$. For instance, if $H_y = 10$ mV, in e the COT converter is stable whereas pulse-bursting is observed in f since the constraint (6) is no longer fulfilled.

provides the constraint (see Section V)

$$v_{in} > \frac{k\hat{v}_r(R_o + R_p)}{kR_o - f_{sw}\Delta t_{\text{OFF}}^{\min}(R_o + R_p)} \equiv v_{in}^{\text{ST}}. \tag{7}$$

It can be noticed that for high enough values of β, the stability of the circuit is significantly influenced by (4) that limits the minimum value of the v_{in} voltage. As an example, imagine to move vertically from point a in Fig. 4 to point b (or from c to d). In a (resp. c) the COT converter is stable and instability appears as soon as the black line is crossed. In this case, pulse-bursting is experienced because the constraint (4) is not fulfilled in b (resp. d).

If one varies the k parameter then the stability boundaries in (4) and (6) turn out to be as in Fig. 5. In this figure, the $v_{in}^{H_y}$ stability boundary is shown for $H_y \in \{2.5, 5, 10\}$ mV. From this figure it becomes clear that, if H_y is low enough, for k lower than approximately 2.3 the v_{in} voltage would be lower bounded by v_{in}^{ST}, i.e., the effects of the comparator hysteresis would be irrelevant. At the same time, if H_y is not properly chosen, it may become a serious limiting factor. Once more as an example, imagine to move vertically from e to f (see Fig. 5) with $H_y = 10$ mV. In e the COT converter is stable and instability appears as soon as the gray solid line is crossed. In this case, pulse-bursting is experienced because the constraint (6) is not fulfilled in f.

Since some of the circuit parameter values such as the R_e ESR are prone to suffer uncertainty, and others, such as the R_o load resistance, may vary during COT operation, the former was thus varied in the range [31.5 mΩ, 58.5 mΩ], i.e., with a variation of ±30% w.r.t. the nominal value in Table 1, and the latter was varied in the {0.66, 1.1, 3.3, 6.6}[Ω] discrete set, which corresponds to a variation from 10% to 100% of the nominal output current ($^{3.3\,\text{V}}/_{0.66\,\Omega} = 5$ A in the example under consideration). The variability of (4), i.e., v_{in}^{PD}, and (6), i.e., v_{in}^{Hy}, w.r.t. to R_e for these values of R_o can be observed in Fig. 6(a) and (b), respectively. It can be noticed that v_{in}^{Hy} and v_{in}^{PD} are almost identically influenced by both R_e and R_o.

IV. CIRCUIT SIMULATIONS

Figure 7 shows the schematic of the COT buck converter that was simulated by employing both the MPLAB® Mindi™

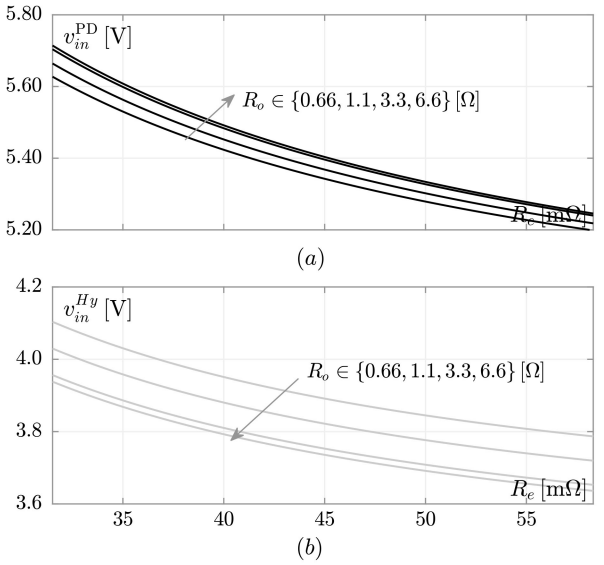

FIGURE 6. v_{in}^{PD} and v_{in}^{Hy} limit conditions w.r.t. to the R_e ESR, in panel (a) and (b) respectively, for different values of the R_o load resistance.

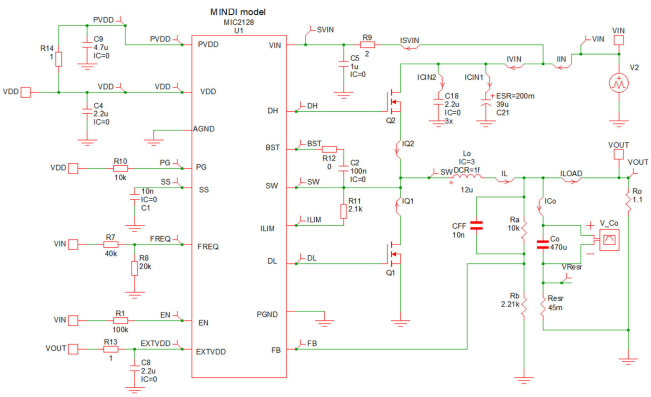

FIGURE 7. The schematic of the COT converter simulated through the MPLAB Mindi Analog Simulator. The core of the circuit is the MIC2128. The parameter k is ruled by R_7 and R_8 as $k = 1 + \frac{R_7}{R_8}$.

Analog Simulator and the SIMetrix/SIMPLIS engine specialised in switching power simulation. The schematic in Fig. 1 is a simplified version of this circuit. The core of the circuit is the MIC2128 by Microchip Technology [15]. The MIC2128 is a constant-frequency synchronous buck controller featuring a unique adaptive ON-time control architecture with external soft start. The MIC2128 operates over an input voltage range from 4.5 V to 75 V. The output voltage is adjustable down to 0.6 V with a guaranteed feedback pin (FB) accuracy of ±1%. The device operates with programmable switching frequency from 270 kHz to 800 kHz. A software library is available and distributed by Microchip Technology which allows the interested reader to reproduce some of the proposed results through the MPLAB® Mindi™ simulator.[3] The values of the circuit parameters reported in Table 1 are those used in Fig. 7.

3. https://www.microchip.com/SWLibraryWeb/producttc.aspx?product=AnalogSimMIC2128

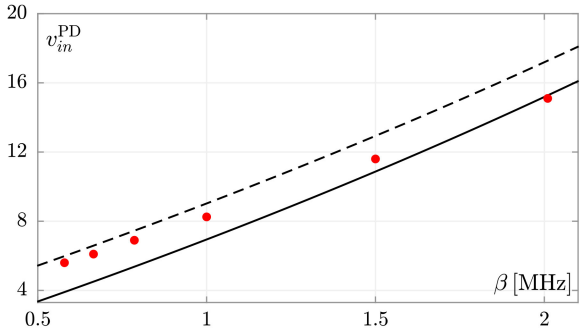

FIGURE 8. The solid and dashed curves represent the v_{in}^{PD} stability boundary obtained by adopting (1) and (8), respectively. The red dots are derived through SIMetrix/SIMPLIS simulations. For such (β, v_{in}) pairs, the circuit exhibits pulse-bursting behavior. These points were achieved by fixing β and sweeping the v_{in} voltage, with a 100 mV step starting from 20 V.

TABLE 2. COT converter circuit parameter values.

β [MHz]	v_{in} [V]	$\Delta t_{\mathrm{ON}}^{\mathrm{sim}}$ [µs]	Δt_{ON} [µs]	$\Delta t_{\mathrm{ON}}^{\mathrm{new}}$ [µs]
0.579	5.60	3.24	2.22	3.21
0.665	6.10	2.84	2.03	2.83
0.786	6.90	2.37	1.80	2.38
1.000	8.25	1.88	1.50	1.89
1.500	11.6	1.23	1.07	1.23
2.010	15.1	0.904	0.822	0.905

The aim of the first set of simulation results is to validate the v_{in}^{PD} stability boundary as a function of the β hyper-parameter. The black solid curve in Fig. 12 represents the v_{in}^{PD} curve obtained by resorting to the numerical procedure described in Section V, for the nominal values in Table 1 and $k = 3$ (for these nominal values $\hat{v}_r = 3.32$ V). Since, the above mentioned MIC2128 MPLAB® Mindi™ model is encrypted to the end-user, it is not possible to alter some of its internal-parameter values. In particular, this holds for g_m, C_m, and H_y. Hence, the red circles reported in Fig. 12 were derived by ad-hoc SIMetrix/SIMPLIS simulations, which were performed by the Microchip Technology staff. For such (β, v_{in}) pairs, the circuit exhibits pulse-bursting behavior. These points were achieved by fixing β and sweeping the v_{in} voltage, with a 100 mV step starting from 20 V. It can be noticed that the boundary derived by starting from the modeling assumptions introduced in Section II (and Section V) is much more optimistic than that obtained simulating the circuit. This discrepancy is observed since (i) the behavioral model of the MIC2128 can only be approximately achieved by the subcircuits that implement its functionalities, and (ii) the working assumptions adopted in Section V are clearly an approximation of the real dynamics of the circuit.

As an example, we report in the third column of Table 2 the Δt_{ON} values corresponding to the red circles shown in Fig. 12 (first and second column of the table). The fourth column reports the values provided by (1). It can be noticed that the ideal model in (1) is not capable of reproducing the same values that are observed in simulation. Hence, we modified the ideal model as

$$\Delta t_{\mathrm{ON}}^{\mathrm{new}} = \frac{k}{f_{sw}} \frac{p}{\frac{v_{in}}{v_o} + q}, \tag{8}$$

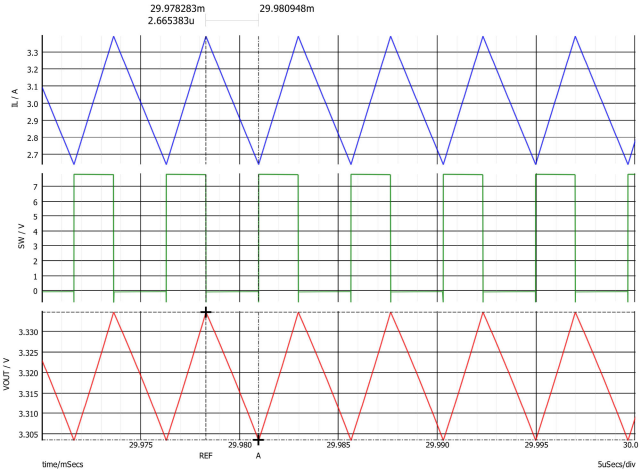

FIGURE 9. The parameter values are reported in Table 1, and $v_{in} = 7.91$ V.

and we derived the p and q fitting values such that $\Delta t_{\mathrm{ON}}^{\mathrm{new}}$ better fits $\Delta t_{\mathrm{ON}}^{\mathrm{sim}}$. After having obtained $p = 0.9639$ and $q = -0.6588$, we derived the values reported in the last column of Table 2, which are in good agreement with $\Delta t_{\mathrm{ON}}^{\mathrm{sim}}$.

Finally, we numerically derived v_{in}^{PD} by resorting to the procedure detailed in Section V but exploiting (8).[4] The result is shown in Fig. 12 (black dashed curve). It can be noticed that the quality of the prediction increases even if now the stability boundary is overestimated.

By adopting MPLAB® Mindi™, we can simulate the circuit for g_m and C_m as in Table 1 ($\beta \approx 0.786$ MHz) . By exploiting (8), we have $v_{in}^{\mathrm{ST}} = 3.50$ V, $v_{in}^{\mathrm{PD}} = 7.40$ V, and $v_{in}^{H_y} = 3.58$ V. Figure 9 shows, for $v_{in} = 7.91$ V the steady-steady evolution of the $\imath_L$ current, of the z signal driving the S switch (see Fig. 1), and of the v_o output voltage (from the top panel to the bottom one). It can be noticed that a single pair of ON-phase and OFF-phase is present and thus the converter is working as predicted ($\boldsymbol{\gamma}_1$ limit cycle), since $v_{in} > v_{in}^{\mathrm{PD}} > v_{in}^{H_y} > v_{in}^{\mathrm{ST}}$. The supply voltage is then reduced below v_{in}^{PD}, and in Fig. 10 a sub-harmonic oscillation can be observed ($v_{in} = 6.89$ V). The $\boldsymbol{\gamma}_1$ limit cycle undergoes a period-doubling bifurcation becoming unstable. A $\boldsymbol{\gamma}_2$ limit cycle is created and the z signal (central panel) exhibits two different and subsequent non-minimal OFF-phases as in Fig. 3(a).

Then we set $R_e = 20\,\mathrm{m}\Omega$ and $k = 1$ obtaining $v_{in}^{\mathrm{ST}} = 4.06$ V and $v_{in}^{H_y} = 12.23$ V. In this case the v_{in}^{PD} stability boundary is not significant since it is lower than v_{in}^{ST} as in Fig. 5 for $k = 1$. The results reported in Fig. 11 were

4. By adopting (8) it is possible to achieve the following generalized version of $v_{in}^{H_y}$ and v_{in}^{ST} too (see (6) and (7), respectively).

$$v_{in}^{H_y} = -\frac{k\left(pR_e\hat{v}_r^2(R_o + R_p) + qf_{sw}L_oH_y(R_e + R_o)\right)}{f_{sw}L_oH_y(R_e + R_o) - pkR_eR_o\hat{v}_r}. \tag{9}$$

$$v_{in}^{\mathrm{ST}} = \frac{k(R_o + R_p)\left(qf_{sw}\Delta t_{\mathrm{OFF}}^{\min} + p\hat{v}_r\right)}{kR_o - f_{sw}\Delta t_{\mathrm{OFF}}^{\min}(R_o + R_p)}, \tag{10}$$

These expressions are used in the following to discuss the simulation results.

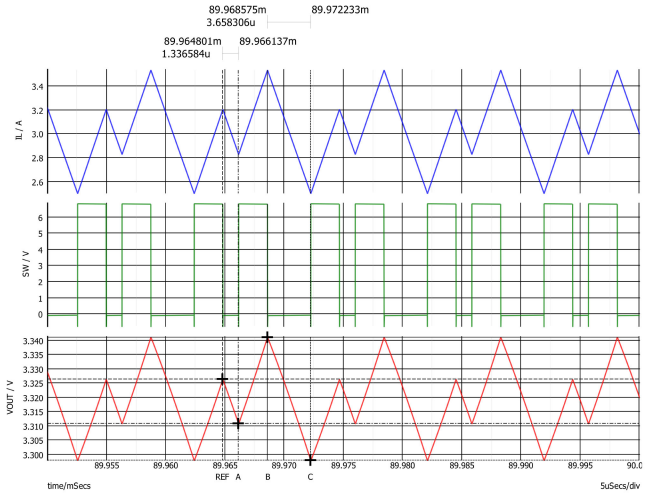

FIGURE 10. The parameter values are reported in Table 1, and $v_{in} = 6.89\,\text{V}$.

obtained by sweeping v_{in} from 24 V (which is significantly larger than $v_{in}^{H_y}$), to $13.00\,\text{V} > v_{in}^{H_y}$. The traces in Fig. 11(a) correspond to this last value of the supply voltage and represent a $\boldsymbol{\gamma}_1$ limit cycle. By further decreasing v_{in} below $v_{in}^{H_y}$, this limit cycle no longer exists since the output of the comparator is still equal to one at the end of the minimum OFF-phase and thus a minimal $\boldsymbol{\gamma}_2$ limit cycle is observed (see the solid traces in Fig. 13 for $v_{in} = 12.00\,\text{V}$). The z signal (central panel) exhibits two different and subsequent OFF-phases, as in Fig. 3(b), being the first one minimal. It is worth mentioning that, if the COT buck converter is started directly at $v_{in} = 13.00\,\text{V}$, a complex limit cycle is observed coexisting with the $\boldsymbol{\gamma}_1$ limit cycle in Fig. 11(a). Such periodic oscillations exhibits several subsequent minimal OFF-phases. The corresponding trajectories are in Fig. 11(b). The circuit works in a bi-stability regime as in [11] and the start-up phase becomes crucial.

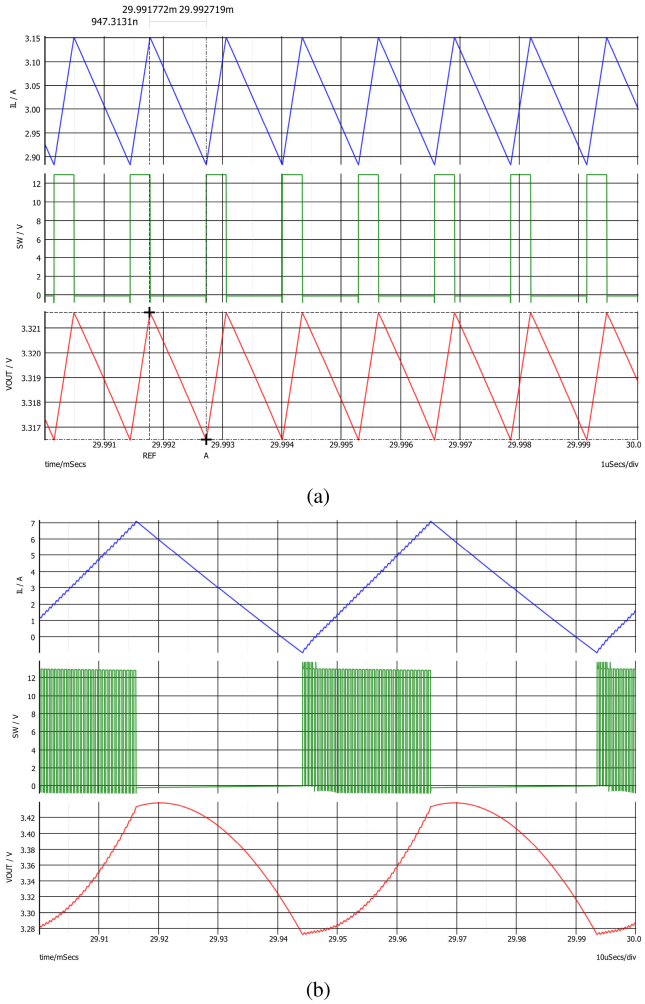

FIGURE 11. The circuit parameter values are those reported in Table 1 but $k = 1$, $R_e = 20\,\text{m}\Omega$, and $v_{in} = 13.00\,\text{V}$. Two coexisting steady-state behaviours are shown. (a) A γ_1 limit cycle. (b) A complex periodic oscillation exhibiting several subsequent minimal OFF-phases.

V. MATHEMATICAL DETAILS

In this section we provide mathematical details to derive the limit conditions presented in Section III. Neglecting the current flowing in R_a, the state equations governing the COT converter dynamics in CCM are

$$\begin{bmatrix} \dot{\imath}_L \\ \dot{v}_C \\ \dot{v}_{C_m} \end{bmatrix} = \begin{bmatrix} \frac{\imath_L R_o - v_C}{C_o(R_e+R_o)} \\ -\frac{R_o(\imath_L R_e + v_C)}{L_o(R_e+R_o)} \\ \beta\left(\frac{R_o(\imath_L R_e+v_C)}{R_e+R_o} - \hat{v}_r\right) \end{bmatrix} + \xi \underbrace{\begin{bmatrix} 0 \\ \frac{v_{in}}{L_o} \\ 0 \end{bmatrix}}_{b}, \quad (11)$$

where $\beta = \frac{g_m}{C_m}$, $\hat{v}_r = v_r \frac{R_a+R_b}{R_b}$, $\xi = 1$ during the ON-phase, and $\xi = 0$ during the OFF-phase.

In the $(\imath_L, v_C, v_{C_m})$ state space the $\hat{v}_r - v_{g_m} = 0$ and $\hat{v}_r - v_{g_m} = -H_y$ switching conditions induced by the `cntr` block lead to the planes (see Fig. 14)

$$\rho_\gamma(\imath_L, v_C, v_{C_m}) : \hat{v}_r - \underbrace{\left(\frac{R_o(\imath_L R_e + v_C)}{R_e + R_o} + v_{C_m}\right)}_{v_{g_m}(\imath_L, v_C, v_{C_m})} = \gamma H_y, \quad (12)$$

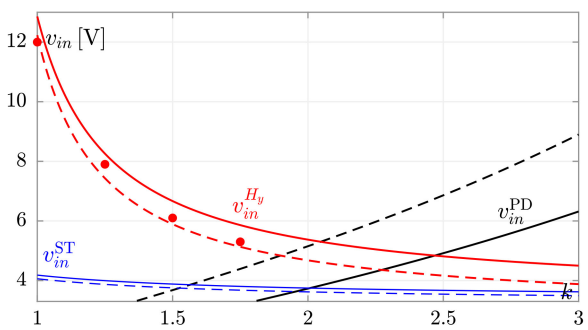

FIGURE 12. The solid and dashed curves represent the v_{in}^{PD}, $v_{in}^{H_y}$, and v_{in}^{ST} stability boundary obtained by adopting (1) and (8), respectively. The red dots are derived through MPLAB Mindi simulations. For such (k, v_{in}) pairs, the circuit exhibits pulse-bursting behavior. These points were achieved by fixing k and sweeping the v_{in} voltage, with a 100 mV step starting from 24 V.

respectively for $\gamma = 0$ and $\gamma = -1$. The unit vector normal to $\rho_\gamma(\imath_L, v_C, v_{C_m})$ is

$$\eta = \mu^{-1}(R_e, R_o R_e, R_e + R_o)^{\text{T}}, \quad (13)$$

where $\mu = \sqrt{R_e^2 + 2R_e R_o + (2 + R_e^2)R_o^2}$.

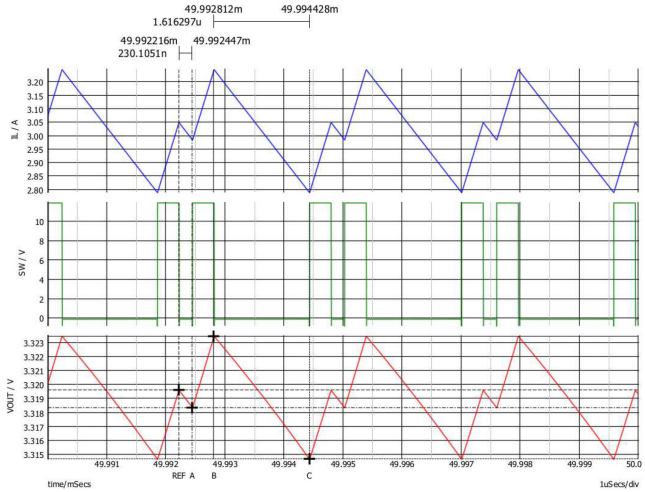

FIGURE 13. The circuit parameter values are those reported in Table 1 but $k = 1.0$, $R_e = 20\,\text{m}\Omega$ and $v_{in} = 12.00\,\text{V}$.

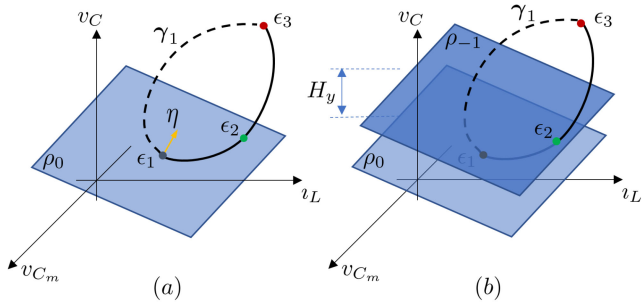

FIGURE 14. Switching manifolds. At ϵ_1 the ON-phase starts and η is the unit vector normal to the ρ_0 plane. The ON-phase ends at ϵ_3. At ϵ_2 the output of the comparator is set to zero since the trajectory hits the ρ_{-1} plane.

At first, to derive both the stability conditions reported in Section III, it is necessary an estimate of the ϵ_1 point in Fig. 14. It represents the state vector at the beginning of the ON-phase.

The v_o output voltage is typically assumed to be fixed at $\hat{v}_o$ during the overall periodic steady-state evolution of the COT converter, and the voltage drop across R_e is neglected. Thus, the v_C component of ϵ_1 is $v_C^{\epsilon_1} = \hat{v}_o$. Concerning $\imath_L$, $\imath_L^{\epsilon_1}$ is computed as the $\hat{v}_r/R_o$ ideal output current (assuming C_o as an open-circuit) minus half the $\Delta\imath_L$ steady-state ripple of the L_o inductor current. The latter is given by

$$\Delta\imath_L = \frac{v_{in} - \hat{v}_r}{L_o}\Delta t_{\text{ON}}, \tag{14}$$

approximating as linear w.r.t. time the charging of the inductor. Figure 15 shows a sketch of $\imath_L$ in the $T = \Delta t_{\text{ON}} + \Delta t_{\text{OFF}}$ working period. An approximation of the duration of the OFF-phase in CCM can be derived by assuming that the ripple of $\imath_L$ in this phase must be equal to $\Delta\imath_L$. This yields

$$\Delta t_{\text{OFF}} = \frac{\left(R_o v_{in} - \left(R_o + R_p\right)\hat{v}_o\right)}{\left(R_o + R_p\right)v_{in}}\Delta t_{\text{ON}}. \tag{15}$$

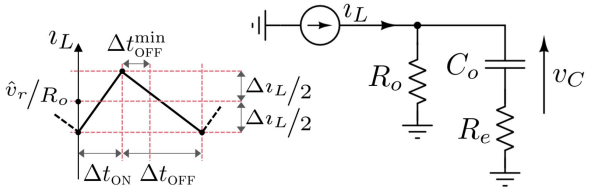

FIGURE 15. Equivalent circuit used for the computation of the approximate steady-state evolution of the v_C voltage.

According to (12) with $\gamma = 0$, we compute the v_{C_m} component of ϵ_1 as

$$v_{C_m}^{\epsilon_1} = \frac{R_e\left(R_o v_{in} - \hat{v}_r\left(R_o + R_p\right)\right)}{2L_o(R_e + R_o)}\Delta t_{\text{ON}}. \tag{16}$$

To obtain the condition reported in (6), since v_C is assumed to be constant during the overall working period, the differential equation governing the evolution of v_{C_m} (see (11)) becomes

$$\dot{v}_{C_m} = \beta\frac{R_e R_o\left(\imath_L - \frac{\hat{v}_r}{R_o}\right)}{R_e + R_o}. \tag{17}$$

Taking into account the right panel of Fig. 15, it is easy to derive that the integral of $\imath_L - \frac{\hat{v}_r}{R_o}$ over the Δt_{ON} time interval is null. Consequently, the Δv_{C_m} variation of v_{C_m} during the ON-phase is null too. More in detail, being $v_{C_m} = v_{C_m}^{\epsilon_1}$ at the beginning of the ON-phase, it decreases below this value for $\imath_L < \hat{v}_r/R_o$. Then, it starts increasing for $\imath_L > \hat{v}_r/R_o$ till reaching again $v_{C_m}^{\epsilon_1}$ for $\imath_L = \hat{v}_r/R_o + \Delta\imath_L/2$. As a consequence, v_{g_m} (see (12)) is maximum at the end of the ON-phase. Since, according to (5) and (12), we aim at ensuring that a t_{H_y} time instant exists such that $\hat{v}_r - v_{g_m}(t_{H_y}) = -H_y$, it translates in guaranteeing that the minimum value of $v_{g_m}(t_{H_y}) - \hat{v}_r$ is at least $-H_y$ during the ON-phase. The limit case leading to (6), i.e., $t_{H_y} = t_{\text{ON}} + \Delta t_{\text{ON}}$, occurs if

$$\frac{R_e R_o}{R_e + R_o}\Delta\imath_L + \Delta v_{C_m} = \frac{R_e R_o}{R_e + R_o}\Delta\imath_L = H_y. \tag{18}$$

In Fig. 14 the ϵ_2 point represents the circuit trajectory at $t = t_{H_y}$ trespassing the switching manifold, viz. the output of the comparator is set to zero.

To guarantee that t_{H_y} belongs to the ON-phase it is thus sufficient to transform (18) into an inequality and to ensure that it is satisfied as a function of the circuit parameter values. Under the hypothesis that Δt_{ON} is governed by (1), this inequality can be rewritten in terms of v_{in} thus obtaining the operational boundary in (6). In case of a more generic dependance of Δt_{ON} on v_{in} and possibly on other design parameters, this operational boundary could be derived only numerically.

Coming back to the control saturation condition provided in (7), it was derived by imposing $\Delta t_{\text{OFF}} = \Delta t_{\text{OFF}}^{\min}$ and reformulating it by resorting to (15) and (1).

To derive the operational boundary in (4), the $\Phi_{\boldsymbol{\gamma}_1}$ monodromy matrix associated to a generic $\boldsymbol{\gamma}_1$ limit cycle is

necessary. It can be computed as

$$\Phi_{\boldsymbol{\gamma}_1} = \mathcal{S}_{\text{OFF}} e^{A\Delta t_{\text{OFF}}} \underbrace{\left(e^{A\Delta t_{\text{ON}}} + \mathcal{T}_{\text{ON}}\right)}_{\mathcal{S}_{\text{ON}}}, \tag{19}$$

where $\mathcal{S}_{\text{OFF}}$ is a standard saltation matrix inserted at the switching event corresponding to the transition from the OFF-phase to the ON-phase [18], $\mathcal{S}_{\text{ON}}$ (with $\mathcal{T}_{\text{ON}}$) is a generalized saltation matrix inserted at the end of the ON-phase when the (delayed) event scheduled at the begging of this very phase occurs [20], A is the matrix that can be easily derived by setting $\xi = 0$ in (11) and recasting the r.h.s. of such equation in matrix form. In particular,[5]

$$\mathcal{S}_{\text{OFF}} = I_3 + \frac{b\eta^{\text{T}}}{\eta^{\text{T}} A\epsilon_1}, \text{ and } \mathcal{T}_{\text{ON}} = -\frac{b\eta^{\text{T}}}{\eta^{\text{T}}(A\epsilon_1 + b)}, \tag{20}$$

where I_3 is the 3×3 identity matrix. An accurate approximation of both ϵ_1 and T thus allow as to monitor the evolution of the eigenvalues of $\Phi_{\boldsymbol{\gamma}_1}$ (*Floquet multipliers*) since T and ϵ_1 are in fact the only missing elements in (19). The COT buck converter is an autonomous system, viz. the r.h.s. of (11) does not depend explicitly on time. Hence, one of the eigenvalues of $\Phi_{\boldsymbol{\gamma}_1}$ is always equal to 1. Local bifurcations of $\boldsymbol{\gamma}_1$ occur whenever one of the remaining two eigenvalues of $\Phi_{\boldsymbol{\gamma}_1}$ is either 1 (*fold bifurcation*) or -1 (*period-doubling bifurcation*), or these two eigenvalues are complex conjugate and their modulus is equal to 1 (*Neimark-Sacker bifurcation*) [17]. The appearance of sub-harmonic $\boldsymbol{\gamma}_2$ limit cycles is typically related to a period-doubling bifurcation. The v_{in}^{PD} stability boundary in Section III-C was derived by numerically computing the locus of point in a given parameter plane such that -1 is one of the eigenvalues of $\Phi_{\boldsymbol{\gamma}_1}$. To do this, it is crucial to remark that it is not necessary to compute the $\boldsymbol{\gamma}_1$ limit cycle trajectory, for instance through a proper time-domain shooting method [19], but just use (1) and (15) for T, and an estimate of ϵ_1.

To this aim, our numerical analysis revealed that the approximation used to derive (2) is not sufficiently accurate to obtain a good approximation of the Floquet multipliers. A more accurate approximation of $v_C^{\epsilon_1}$ and hence of $v_{C_m}^{\epsilon_1}$ is necessary. If the steady state evolution of the $\imath_L$ current is assumed to be *robust*, in the sense that the sketch reported in Fig. 15 is reliable in almost all CCM operation conditions, viz. the linear charging of the inductor is a realistic assumption, $v_C^{\epsilon_1}$ can be derived by solving the linear circuit in Fig. 15. In particular, a periodic boundary value problem is solved w.r.t. $v_C(t_{\text{ON}}) = v_C^{\epsilon_1}$ by imposing $v_C^{\epsilon_1} = v_C(t_{\text{ON}} + \Delta t_{\text{ON}} + \Delta t_{\text{OFF}}; v_C^{\epsilon_1})$. Since the problem is linear w.r.t. the $v_C^{\epsilon_1}$ unknown it can be solved in closed form. The solution is in (21), shown at the bottom of the page with the new $v_{C_m}^{\epsilon_1}$ value derived by substituting $\imath_L^{\epsilon_1}$ and $v_C^{\epsilon_1}$ in (12) with $\gamma = 0$.

5. For evident space limitation it is not possible to go more in details concerning $\mathcal{S}_{\text{OFF}}$, $\mathcal{S}_{\text{ON}}$, and $\mathcal{T}_{\text{ON}}$. The interested reader may refer to [20].

TABLE 3. Eigenvalues of the $\Phi_{\boldsymbol{\gamma}_1}$ monodromy matrix.

γ_1	λ_1	$\hat{\lambda}_1$	λ_2	$\hat{\lambda}_2$	λ_3	$\hat{\lambda}_3$
a	1.0000	1.0000	0.8413	0.8413	−0.9662	−0.9661
c	1.0000	1.0000	0.8412	0.8412	−0.9836	−0.9818
e	1.0000	1.0000	0.9171	0.9171	−0.1091	−0.1092

To appreciate the effectiveness of the proposed approach, in Table 3 we compared the $\{\hat{\lambda}_i\}$ eigenvalues of $\Phi_{\boldsymbol{\gamma}_1}$ computed through the discussed approximation with the $\{\lambda_i\}$ ones derived as a byproduct of the shooting method for the accurate $\boldsymbol{\gamma}_1$ limit cycles considered in Section III-C.

VI. CONCLUDING REMARKS

This paper provides a set of feasible operative boundaries that allow the designer to tune the COT converter architecture (*internal parameters*), and the user to choose specific application (*external parameters*) that are under his/her control.

As a major final consideration, it deserves to remark that a significant contribution to the circuit instability has been proven to derive from the converter control algorithm, which involves a minimum OFF-phase duration, and interplays with the hysteresis of the comparator driving the input of the block implementing the circuit control algorithm itself.

The availability of an accurate estimate of the period doubling bifurcation condition, in which the effect of switching dynamics clearly appears through saltation matrices, could be used to revisit the ramp-compensation approaches proposed in the literature, in the light of recent results proposed for different control strategies of this kind of circuits.

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$$v_C^{\epsilon_1} = \frac{\hat{v}_r\left(2C_o\left((R_e+R_o)\left(R_p+R_o\right)\right) + 2L_o + \Delta t_{\text{ON}}\left(R_o+R_p\right)\right) - \Delta t_{\text{ON}} v_{in} R_o - \dfrac{2v_{in}C_oR_o(R_e+R_o)\left(e^{\frac{\Delta t_{\text{ON}}}{C_o(R_e+R_o)}}-1\right)}{\frac{v_{in}\Delta t_{\text{ON}}R_o}{e^{\hat{v}_rC_o(R_e+R_o)(R_o+R_p)}-1}}}{2L_o}$$

$$v_{C_m}^{\epsilon_1} = \frac{R_o\left(\Delta t_{\text{ON}} v_{in} - \hat{v}_r\left(2C_oR_p + \Delta t_{\text{ON}}\right)\right) - \Delta t_{\text{ON}}\hat{v}_rR_p + 2C_oR_o^2\left(\dfrac{v_{in}\left(e^{\frac{\Delta t_{\text{ON}}}{C_o(R_e+R_o)}}-1\right)}{\frac{v_{in}\Delta t_{\text{ON}}R_o}{e^{\hat{v}_rC_o(R_e+R_o)(R_o+R_p)}-1}} - \hat{v}_r\right)}{2L_o} \tag{21}$$

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