



PLL-Free Voltage Oriented Control Strategy for Voltage Source Converters Tied to Unbalanced Utility Grids

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Asymmetrical working conditions of the utility grid introduce the large-amplitude negative-sequence component to the output current of the voltage source converter (VSC), causing power semiconductor devices to suffer from thermal fatigue and thermal damage. Though the conventional phase-locked loop (PLL) based voltage oriented control (VOC) solution can suppress the steady-state negative-sequence current effectively, it has a weak suppression ability of transient overload current, and even aggravates the transient current asymmetry and causes more severe transient impact to the VSC. This paper first analyzes the transient performance of the conventional VOC strategy, especially its dynamic response time and the main factors for performance limitation. On this basis, the PLL-free VOC strategy for VSCs tied to unbalanced grids is proposed, and its critical parts, namely, the reference current calculation and the fast detection of the grid voltage sequence components, are implemented. Besides, to improve the frequency adaptability, a high-performance grid frequency detection strategy is developed based on the difference-frequency phase caused by the frequency variation. Finally, experiments are performed to verify the effectiveness and advancement of the proposed method. Specifically, the results proved the rapidity, accuracy, and frequency adaptability of the proposed method in suppressing the VSC negative-sequence current, both in transient and steady-state conditions.

Keywords: PLL-free, frequency detection, grid-connected VSC, unbalanced grid, converters

1 INTRODUCTION

With the bulk application of wind power, photovoltaic power, energy storage, flexible AC transmission systems, and other devices in the power systems, there has been an increasing proportion and importance of grid-tied voltage-source-converters (VSCs), Xiong et al. (2020a); Zhang K. et al. (2021). At the same time, the overhead power lines used for distributed power collection are scattered in a wide geographic space, causing high susceptibility of the utility grids to various asymmetric disturbances and requiring the grid-tied VSCs to be equipped with the ability to suppress unbalanced disturbances Xiu et al. (2021a). Different from the electromechanical equipment with excellent overload performance and strong resistance to faulty impact, VSCs

with the semiconductor device as the core have weak overload capacity. Long-term overload operation will cause equipment performance degradation or even complete damage, Xiu et al. (2021b). Therefore, it is necessary to detect the amplitude, phase, and frequency information of the main electrical components in the transient process as quickly as possible and use advanced VSC control strategies to suppress random disturbances and various faults, so as to effectively reduce the time and intensity of the VSC subjected to the transient impact, ensure that the VSC can enter the new stable state quickly and safely, and improve the system reliability and security, Xiong et al. (2020b).

In recent years, many investigations have been performed on the detection and control strategies for the VSC system under unbalanced utility grid conditions. Wai et al. (2015) proposed a neural fuzzy network based online compensation method for suppressing the three-phase unbalanced current on the grid side. In order to effectively suppress the negative impact of harmonics on the VSC control performance, Xiong et al. (2016c) compares the performance of two typical harmonic elimination algorithms, and lays out the basis for the optimal algorithm selection in engineering applications. Dedeoglu and Konstantopoulos (2018) extended the rotational coordinate frame and used two sets of dynamically changing reference frames to control the negative-sequence component, effectively suppressing the secondary fluctuation of the DC side voltage. In the aforementioned works, the VSC control is realized by making use of the phase-locked loop (PLL), which can generate inaccurate or delayed phase information under the event of unbalanced utility grid faults, especially the single synchronous reference frame (SRF) PLL, leading to reduced power transmission efficiency of the grid-tied VSCs, or even worse, their inability to work. To this end, Rodriguez et al. (2007) proposes a decoupled double SRF PLL (DDSRF-PLL) to completely eliminate the detection errors of conventional single SRF PLL, yet leading to the complex control loop design and significantly long response time. In order to simplify the control system structure, Chaudhary et al. (2012) utilized the second-order generalized integrator based PLL (SOGI-PLL) to obtain the real-time phase of the unbalanced utility grid. However, Zhang C. et al. (2021) pointed out the concealed stability issue of SOGI-PLLs arising from different implementations of the frequency-feedback-path. To avoid the negative-sequence component from affecting the accuracy, stability and rapidity of the PLL, Li Z. et al. (2018) improved the conventional SRF-PLL, yet the detection time is still too long and the VSC will still suffer from the transient overload current for a long time. To achieve the desired multi-objective control and the optimal overall performance, Lin et al. (2019) introduced the particle swarm algorithm to further optimize the control parameters of the VSC system. Besides that, in order to increase the adaptability to the non-ideal grid conditions, Mishra and Lal (2021) proposed an enhanced control method to suppress the effect of distorted grid voltage.

In addition to the continuous improvement of the various PLL methods, there are several advanced detection technologies and control strategies trying to directly remove the PLLs. Xiong et al.

(2016b) was the first to realize the high-performance amplitude and phase detection without PLL, yet it cannot adapt to the working condition of grid frequency fluctuation or provide the real-time grid frequency information. Wu et al. (2020b) proposed a fast phase detection scheme and successfully extracted the real-time phase of the fundamental-frequency positive-sequence component of the utility voltage under unbalanced and distorted conditions. In order to realize a PLL-free scheme in the VSC system, Nian et al. (2016) achieved the suppression of negative-sequence current under unbalanced utility grids, yet this scheme requires extensive dynamic response time as long as 4 grid cycles in the presence of grid frequency fluctuations. Li L. et al. (2018) successfully developed the PLL-free direct power control strategy to compensate for the unbalanced current generated by the unbalanced utility grids. Cheng et al. (2020) realized the PLL-free control of the converter in the unbalanced grid, yet it is still limited to the condition with insignificant grid frequency fluctuations. Further, Wu et al. (2020b) designed an independent control system for VSC power transmission, which can deal with the power fluctuation issue under unbalanced utility grids.

In this paper, a PLL-free VOC strategy for VSCs tied to unbalanced grids, which can minimize the overload current and hence the time and intensity of the VSC suffering from its impact, is developed. In **Section 2**, the basic PLL based VOC strategy for the grid-tied VSC is introduced, and its technical challenges are analyzed. In **Section 3**, the PLL-free VOC strategy of the grid-tied VSC is designed, and the command current calculation and the fast detection method of grid voltage sequence components are also presented. In **Section 4**, a fast frequency detection scheme based on the detected difference-frequency phase is developed, enhancing the frequency adaptability performance of the PLL-free VOC strategy. Finally, the effectiveness and advancement of the proposed scheme are verified in **Section 5**.

2 PLL-BASED VOC STRATEGY AND ITS TECHNICAL CHALLENGES

2.1 Basic Principle

The main circuit topology of the grid-tied VSC is shown in **Figure 1**, where R , L , and C are the equivalent series resistance, inductance, and DC-side capacitance of the VSC system; U_{dc} and I_{dc} are the DC-side capacitor voltage and DC input current of the VSC, respectively; u_{abc} and v_{abc} are the three-phase grid voltage and the output voltage of the VSC system, respectively.

When the utility grid is operating in the ideal state, the three-phase grid voltage is balanced, and only the positive-sequence component exists. In this case, the grid voltage can be formulated as

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} U_m^+ \sin \theta \\ U_m^+ \sin(\theta - 2\pi/3) \\ U_m^+ \sin(\theta + 2\pi/3) \end{bmatrix} \quad (1)$$

$$\theta = \omega t + \phi \quad (2)$$

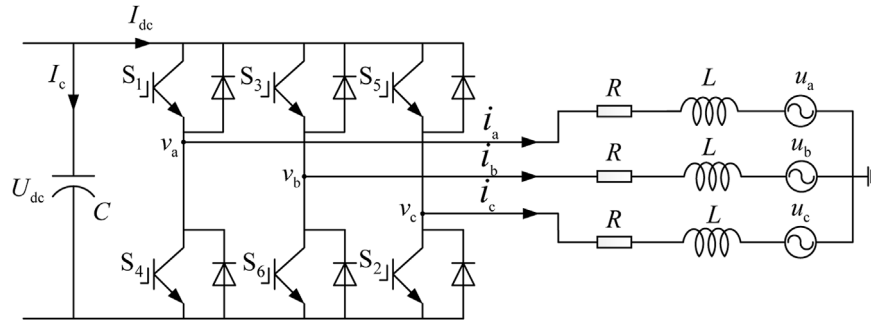


FIGURE 1 | System topology of the grid-tied VSC.

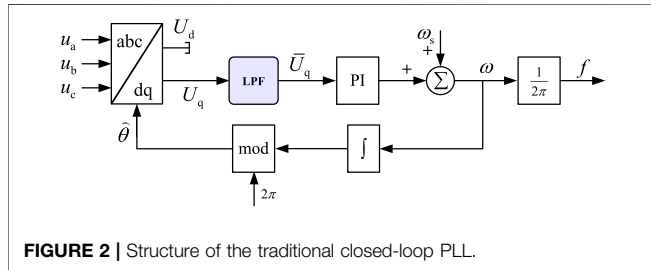


FIGURE 2 | Structure of the traditional closed-loop PLL.

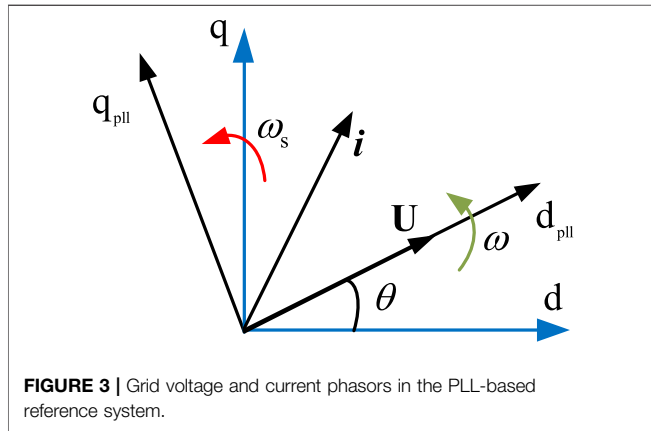


FIGURE 3 | Grid voltage and current phasors in the PLL-based reference system.

where U_m^+ , θ , ϕ , and ω are the amplitude, real time phase, initial phase, and angular frequency of the grid voltage, respectively, and $\phi \in [0, 2\pi)$.

To maintain synchronous operation of the VSC w.r.t. the utility grid, it is necessary to primarily obtain the phase (θ) and frequency (ω) information of the grid voltage, based on which the output voltage and power of the VSC can be adjusted, thereby achieving stable grid-tied operation. To this end, the PLL with the structure shown in **Figure 2** is usually used, where k_p and k_i are the proportional and integral coefficients of the PI controller, respectively, mod is the modulo operation that calculates the remainder after division, and the abc/dq transformation matrix is given by

$$T_{abc/dq} = \frac{2}{3} \begin{bmatrix} \sin \hat{\theta} & \sin(\hat{\theta} - 2\pi/3) & \sin(\hat{\theta} + 2\pi/3) \\ \cos \hat{\theta} & \cos(\hat{\theta} - 2\pi/3) & \cos(\hat{\theta} + 2\pi/3) \end{bmatrix} \quad (3)$$

Since θ is time-variant (see **Eq. 2**), the PLL dynamically adjusts its output phase through a PI controller-based closed-loop control system, and tracks the phase of the grid voltage in real time by making $\hat{\theta}$ approach to θ . When $\hat{\theta} = \theta$, i.e., the phase is synchronized, the phase and frequency of the PLL output are those of the grid voltage (see **Figure 3**).

Using the transformation matrix in **Eq. 1** and the PLL output phase, the grid voltage in **Eq. 1** can be converted into

$$\begin{bmatrix} U_{d_pll} \\ U_{q_pll} \end{bmatrix} = U_m^+ \begin{bmatrix} \cos(\theta - \hat{\theta}) \\ \sin(\theta - \hat{\theta}) \end{bmatrix} \quad (4)$$

According to **Eq. 4**, when the phase is locked, the PLL-based dq-coordinate frame has its d-axis aligned with the grid voltage vector, and a null q-axis component. At this time, the dq-frame is grid voltage oriented.

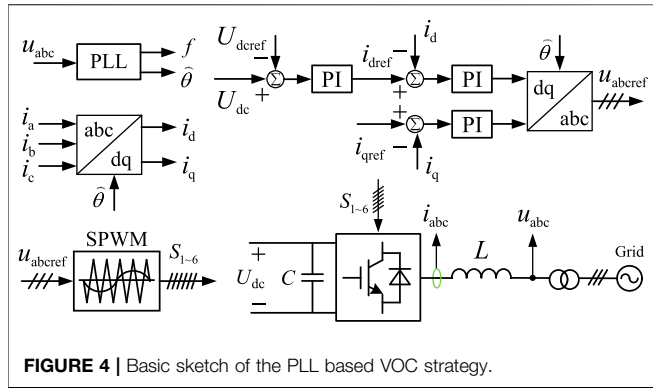
In such a frame, the active power and reactive power transmitted from the VSC to the grid can be calculated as

$$\begin{cases} p = \frac{3}{2}(U_{d_pll}I_{d_pll} + U_{q_pll}I_{q_pll}) = \frac{3}{2}U_m^+I_{d_pll} \propto I_{d_pll} \\ q = \frac{3}{2}(U_{q_pll}I_{d_pll} - U_{d_pll}I_{q_pll}) = -\frac{3}{2}U_m^+I_{q_pll} \propto I_{q_pll} \end{cases} \quad (5)$$

If the power loss of the VSC system is ignored, the active power output by the VSC is equal to that on the DC-side, namely

$$p = U_{dc}I_{dc} = \frac{3}{2}U_m^+I_{d_pll} \quad (6)$$

In the grid voltage-oriented dq-frame, the active power and reactive power output by the VSC are only proportional to their d- and q-axis current components, and the d-axis current is proportional to the DC-side voltage of the VSC. Hence, the d- and q-axis current components of the VSC can be controlled separately, by adjusting the DC capacitor voltage or the reactive power output by the VSC. The relevant control methods are only valid in the grid



voltage-oriented dq-frame, and are referred to as the VOC strategies (see Figure 4).

2.2 Dynamic Response Time

Preliminary assumptions are made prior to obtaining the dynamic response time of the PLL based VOC strategy. The PLL is a key component of the VOC strategy, and the dynamic responses of the capacitor voltage control and the current control, which are based on the output phase of the PLL, can be neglected due to their fast speeds. Therefore, the response time of the VOC strategy mainly depends on the PLL. The small-signal model of the PLL with single SRF for dynamic characteristics analysis is shown in Figure 5.

When the steady-state phase error of the PLL is negligible, we have

$$U_{q_pll} = U_m^+ \sin(\theta - \hat{\theta}) \approx U_m^+ \Delta\theta \tag{7}$$

According to Figure 5, the closed-loop phase transfer function and the phase error transfer function can be expressed respectively as

$$H_\theta(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{8}$$

$$E_\theta(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{9}$$

where ζ is the damping factor and ω_n is the natural frequency, and

$$\omega_n = \sqrt{k_i} \tag{10}$$

$$\zeta = \frac{k_p}{2\sqrt{k_i}} \tag{11}$$

In the under-damped state, the phase errors corresponding to the phase step and frequency step of the PLL can be respectively expressed as

$$\theta_e^{\Delta\theta}(t) = \frac{\Delta\theta}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n \sqrt{1-\zeta^2} t + \gamma) \tag{12}$$

$$\theta_e^{\Delta\omega}(t) = \frac{\Delta\omega}{\omega_n \sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \sin(\omega_n \sqrt{1-\zeta^2} t) \tag{13}$$

where

$$\gamma = \arctan(\sqrt{1-\zeta^2} t) \tag{14}$$

Hence, the 2% dynamic response time t_s and the system bandwidth ω_b of the PLL based VOC strategy can be expressed as Freijedo et al. (2009), Wang and Wei Li (2011).

$$t_s = \frac{-\ln 0.02 - \ln \sqrt{1-\zeta^2}}{\xi\omega_n} \approx \frac{4}{\xi\omega_n} \tag{15}$$

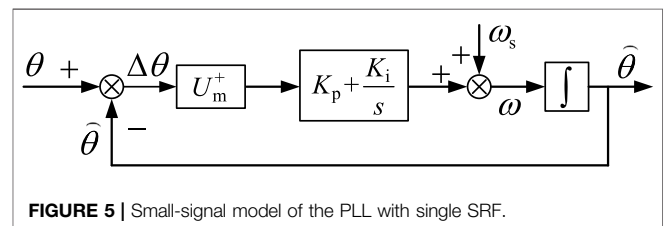
$$\omega_b = \omega_n \sqrt{1+2\zeta^2 + \sqrt{2+4\zeta^2+4\zeta^4}} \tag{16}$$

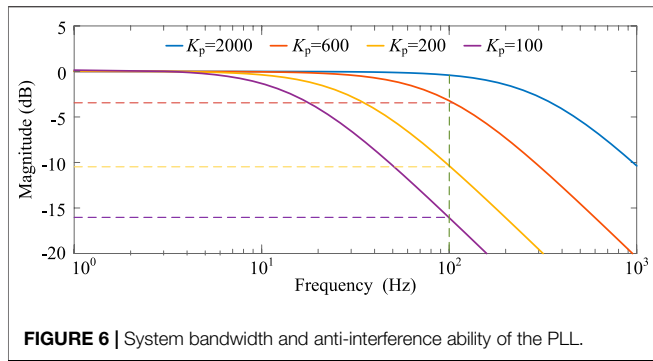
It can be seen from Eqs 15, 16 that the larger the damping factor ζ and natural frequency ω_n , the larger the system bandwidth and the faster the response speed, and vice versa. In fact, the damping factor and natural frequency of the VOC strategy are determined by the proportional gain k_p and the integral gain k_i of the PLL's PI controller. The larger these gain values, the higher the bandwidth, and the faster the response speed.

2.3 Technical Challenges

The measured signal inevitably contains various random noises, making it necessary to equip the system with anti-interference ability. With reference to Eq. 8, the PLL exhibits the low-pass filter (LPF) feature, hence the VOC strategy can partially suppress the detection error caused by the random noise and high-order harmonics. Under the common grid conditions of symmetrical operation, the low-order harmonics do not have large amplitudes, and the VOC strategy-based VSC system can obtain satisfactory dynamic performance and anti-noise ability by adjusting the proportional and integral parameters, Wu et al. (2020a); Xiong et al. (2016b). However, under the asymmetric disturbance conditions that can easily occur, electrical quantities are characterized by low-frequency harmonics with large amplitudes in the dq coordinate frame, especially the second harmonic. The basic principle is analyzed as follows.

According to the symmetrical component analysis, the three-phase unbalanced voltage can be decomposed into the positive-sequence, negative-sequence, and zero-sequence components. Without loss of generality, the influence of negative-sequence component on the VOC strategy is illustrated here as an example. The zero-sequence component can be analyzed similarly. Based on this





assumptions, the three-phase asymmetrical grid voltage \mathbf{U} can be expressed by the positive-sequence component \mathbf{U}^+ and the negative-sequence component \mathbf{U}^- as

$$\begin{cases} \mathbf{U} = \mathbf{U}^+ + \mathbf{U}^- \\ \mathbf{U} = [u_a(t) \ u_b(t) \ u_c(t)]^T \\ \mathbf{U}^+ = \begin{bmatrix} U_m^+ \sin \theta \\ U_m^+ \sin(\theta - 2\pi/3) \\ U_m^+ \sin(\theta + 2\pi/3) \end{bmatrix} \\ \mathbf{U}^- = \begin{bmatrix} U_m^- \sin(\theta + \delta) \\ U_m^- \sin(\theta + 2\pi/3 + \delta) \\ U_m^- \sin(\theta - 2\pi/3 + \delta) \end{bmatrix} \end{cases} \quad (17)$$

where U_m^- is the amplitude of the negative-sequence component of the grid voltage, and δ is the angle difference between the negative-sequence component and the initial phase of the positive-sequence component.

Accordingly, in the dq coordinate frame of the PLL, the asymmetrical grid voltage shown in (17) will be transformed into

$$\begin{bmatrix} U_{d_pll} \\ U_{q_pll} \end{bmatrix} = \begin{bmatrix} U_m^+ \cos(\theta - \hat{\theta}) - U_m^- \cos(2\omega t + \theta - \hat{\theta} + \delta) \\ U_m^+ \sin(\theta - \hat{\theta}) + U_m^- \sin(2\omega t + \theta - \hat{\theta} + \delta) \end{bmatrix} \quad (18)$$

When the real time phase is locked by the PLL, i.e., $\theta = \hat{\theta}$, we have

$$\begin{bmatrix} U_{d_pll} \\ U_{q_pll} \end{bmatrix} = \begin{bmatrix} U_m^+ - U_m^- \cos(2\omega t + \delta) \\ U_m^- \sin(2\omega t + \delta) \end{bmatrix} \quad (19)$$

According to Eqs 18, 19, the unbalanced grid voltage always has a double-frequency AC component with large amplitude in the dq coordinate frame, both during the transient and steady state. For the PLL system that achieves zero q-axis component as the target, the double-frequency component will have a significant impact on its synchronization performance and tracking error. For better accuracy of the output phase and frequency information, the system bandwidth must be significantly reduced in the unbalanced grid case to effectively suppress the double-frequency AC component, as shown in Figure 6. This can be achieved by reducing the proportional gain k_p and the integral gain k_i in the PI controller of the PLL; however, this improvement of system anti-interference ability substantially extends the dynamic response time of the VOC strategy. To address this issue, a

variety of LPFs (see the purple region in Figure 2) have been proposed to suppress the negative effect of the double-frequency component. Since the filter is contained in the control loop, they are interacted in the dynamic control process, thus sharply increasing the system complexity, and making it difficult to effectively analyze and control the system dynamic performance. The most widely used SOGI-PLL and DDSRF-PLL solutions take nearly two grid cycles to return to the steady state, under the premise of working in their optimal states.

It is obvious that a conflict is inevitable between the response speed (depending on the system bandwidth) and the anti-interference ability for a closed-loop dynamic control system, and thus, the art of compromise is needed for designing the PLL based VOC strategy. However, under severely unbalanced utility grid conditions, the more common result is that the two indicators have been both significantly jeopardized, making it difficult to achieve a satisfactory compromise for performance design. Since the root of such issues lies in the complex dynamic process introduced by the PLL, one solution would be adopting a PLL-free VOC scheme.

In this paper, a PLL-free VOC scheme is developed by using the constant-speed rotational coordinate frame to replace the traditional dq-coordinate frame of the PLL. To avoid the complex dynamic adjustment process of the PLL, this constant-speed rotational frame is coherent with the rotation speed of the grid voltage vector (i.e., the synchronous speed of the grid, ω_s), ensuring that the electrical quantities are converted into constant values in this frame. The dq-axis components of the grid voltage no longer participate in the closed-loop control process, eliminating the dynamic loops used for phase and frequency measurement. Accordingly, the dynamic response speed of the VOC strategy can be greatly improved.

Figure 3 shows the dq-axis components of the grid voltage \mathbf{U} in different dq frames. These quantities can be related as

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \cos \varphi & -\sin \varphi \\ \sin \varphi & \cos \varphi \end{bmatrix} \begin{bmatrix} U_{d_pll} \\ U_{q_pll} \end{bmatrix} \quad (20)$$

Based on Eq. 20, the two coordinate frames can be converted through a linear transformation, and when the PLL is in steady state, $\varphi = \phi$. Accordingly, there is no essential difference between the two frames; grid quantities merely have different projection results in corresponding coordinate frames. However, the dq-axis components of the grid voltage are invariant in the constant-speed rotational frame, yet involved in the complex dynamic process when using the rotational frame of the PLL. In the latter case, the dq-components exhibit complex time-variant behaviors, and only transition to the steady state after a long time, restricting the performance of subsequent VSC voltage and current control, causing the VSC equipment to withstand a long-term overload impact under severe asymmetric disturbances, and introducing a serious threat to the reliability and safety of the equipment.

3 IMPLEMENTATION OF PLL-FREE VOC STRATEGY FOR VSCS TIED TO UNBALANCED GRIDS

3.1 Calculation of VSC Control Reference Values

Since the circuit topology of the grid-tied VSC (see **Figure 1**) has no neutral point or neutral line, the effect of the zero-sequence component of the VSC system can be neglected. Therefore, in the PLL-free constant-speed rotational coordinate frame, the positive- and negative-sequence circuits of the VSC system can be described as

$$\begin{cases} \mathbf{v}_{dq}^+ = \mathbf{u}_{dq}^+ + R\mathbf{i}_{dq}^+ + L \frac{d\mathbf{i}_{dq}^+}{dt} \mp j\omega L\mathbf{i}_{qd}^+ \\ \mathbf{v}_{dq}^- = \mathbf{u}_{dq}^- + R\mathbf{i}_{dq}^- + L \frac{d\mathbf{i}_{dq}^-}{dt} \mp j\omega L\mathbf{i}_{qd}^- \end{cases} \quad (21)$$

The instantaneous power at the VSC grid-side is

$$\begin{cases} P = P_0 + P_{\sin} \sin(2\omega t) + P_{\cos} \cos(2\omega t) \\ Q = Q_0 + Q_{\sin} \sin(2\omega t) + Q_{\cos} \cos(2\omega t) \end{cases} \quad (22)$$

From **Eq. 22**, the active and reactive powers output by the VSC system, under the unbalanced grid voltage condition, include not only the constant power components P_0 and Q_0 under the balanced condition, but also the double-frequency oscillatory components P_{\sin} , P_{\cos} , Q_{\sin} , and Q_{\cos} , with the expression of

$$\begin{bmatrix} P_0 \\ P_{\sin} \\ P_{\cos} \\ Q_0 \\ Q_{\sin} \\ Q_{\cos} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} U_d^+ & U_q^+ & U_d^- & U_q^- \\ U_q^- & -U_d^- & -U_q^+ & U_d^+ \\ U_d^- & U_q^- & U_d^+ & U_q^+ \\ U_q^+ & -U_d^+ & U_q^- & -U_d^- \\ -U_d^- & -U_q^- & U_d^+ & U_q^+ \\ U_q^- & -U_d^- & U_q^+ & -U_d^+ \end{bmatrix} \begin{bmatrix} I_d^+ \\ I_q^+ \\ I_d^- \\ I_q^- \end{bmatrix} \quad (23)$$

In order to suppress the power fluctuations, we have

$$\begin{cases} P_0 = P_{ref} \\ Q_0 = Q_{ref} \\ P_{\sin} = P_{\cos} = Q_{\sin} = Q_{\cos} = 0 \end{cases} \quad (24)$$

where the subscript ref represents the reference value of the corresponding physical quantity.

By substituting **Eq. 24** into **Eq. 23**, the VSC output current reference when the power oscillation is suppressed can be obtained, yielding

$$\begin{bmatrix} I_{dref}^+ \\ I_{qref}^+ \\ I_{dref}^- \\ I_{qref}^- \end{bmatrix} = \frac{2}{3} \cdot \frac{1}{MN} \cdot \begin{bmatrix} -NU_d^+ & MU_q^+ \\ -NU_q^+ & MU_d^+ \\ NU_d^- & MU_q^- \\ NU_d^- & -MU_q^- \end{bmatrix} \begin{bmatrix} P_{ref} \\ Q_{ref} \end{bmatrix} \quad (25)$$

where

$$\begin{cases} M = [(U_d^-)^2 - (U_d^+)^2 + (U_q^-)^2 - (U_q^+)^2] \\ N = [(U_d^-)^2 + (U_d^+)^2 + (U_q^-)^2 + (U_q^+)^2] \end{cases} \quad (26)$$

The core component of the VSC system, i.e., the semiconductor power device, has extremely weak overcurrent capability and high sensitivity to temperature rise. Hence, under severely unbalanced utility grid conditions, the negative-sequence current is usually suppressed first to ensure that the current amplitude of each phase is balanced and not overloaded, avoiding the overcurrent-related thermal fatigue and thermal damage of power semiconductor devices. Accordingly, the negative-sequence current and power commands of the VSC are given by

$$\begin{cases} P_0 = P_{ref} \\ Q_0 = Q_{ref} \\ I_{dref}^- = I_{qref}^- = 0 \end{cases} \quad (27)$$

By substituting **Eq. 27** into **Eq. 23**, the positive-sequence current command of the VSC when the negative-sequence current is suppressed can be obtained as

$$\begin{bmatrix} I_{dref}^+ \\ I_{qref}^+ \end{bmatrix} = \frac{2}{3} \cdot \frac{1}{\Theta} \cdot \begin{bmatrix} U_d^+ & U_q^+ \\ U_q^+ & -U_d^+ \end{bmatrix} \begin{bmatrix} P_{ref} \\ Q_{ref} \end{bmatrix} \quad (28)$$

where

$$\Theta = (U_d^+)^2 + (U_q^+)^2 \quad (29)$$

In general, to achieve DC-side voltage stability of the grid-tied VSC, the VOC strategy uses a capacitor voltage control loop to calculate the active power command of the VSC, yielding

$$P_{ref} = \left(K_{pp} + \frac{K_{pi}}{s} \right) (U_{dc} - U_{dcref}) \quad (30)$$

where K_{pp} and K_{pi} are the proportional and integral gains of the outer voltage loop, respectively.

At the same time, in order to achieve unity power factor of the grid-tied operation, the reactive power command of the VSC is set to 0, i.e., $Q_{ref} = 0$. However, when the reactive power is required to be provided by the VSC, its reference value can be set according to the specification. When the VSC is required to actively support the stable operation of the grid voltage, the reactive power command Q_{ref} is usually calculated by an AC-side voltage U_{ac} control loop, namely

$$Q_{ref} = \left(K_{qp} + \frac{K_{qi}}{s} \right) (U_{acref} - U_{ac}) \quad (31)$$

where K_{qp} and K_{qi} are the proportional and integral gains of the outer AC voltage loop, respectively.

3.2 Grid Voltage Sequence Component Detection

When calculating the VSC output current command according to **Eqs 25, 28**, it is necessary to first detect the sequence components of the unbalanced grid voltage. To this end, this paper resorts to the fast open-loop detection algorithm proposed by Xiong et al. (2016b) and Xiu et al. (2021a), and uses the grid voltage \mathbf{U} and its orthogonal component \mathbf{U}_\perp to directly extract the sequence components in the stationary coordinate frame. This gives

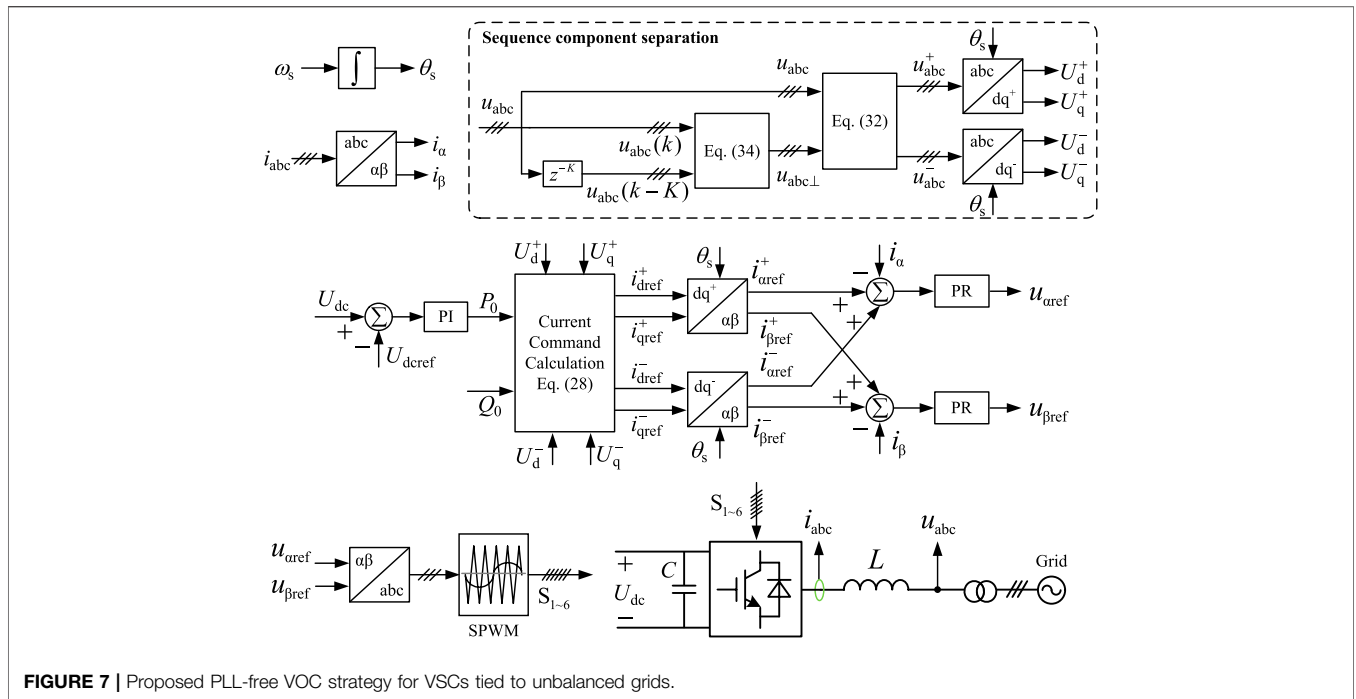


FIGURE 7 | Proposed PLL-free VOC strategy for VSCs tied to unbalanced grids.

$$\begin{cases} \mathbf{U}^+ = \mathbf{T}_\alpha^+ \mathbf{U} + \mathbf{T}_\beta^+ \mathbf{U}_\perp \\ \mathbf{U}^- = \mathbf{T}_\alpha^- \mathbf{U} + \mathbf{T}_\beta^- \mathbf{U}_\perp \end{cases} \quad (32)$$

where

$$\mathbf{T}_\alpha^+ = \frac{1}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}, \quad \mathbf{T}_\beta^+ = \frac{\sqrt{3}}{6} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}$$

$$\mathbf{T}_\alpha^- = \frac{1}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & -1 & 2 \\ -1 & 2 & -1 \end{bmatrix}, \quad \mathbf{T}_\beta^- = \frac{\sqrt{3}}{6} \begin{bmatrix} 0 & -1 & 1 \\ -1 & 1 & 0 \\ 1 & 0 & -1 \end{bmatrix}$$

Similar to the grid voltage \mathbf{U} , which is composed of the positive-sequence component \mathbf{U}^+ and the negative-sequence component \mathbf{U}^- , the orthogonal voltage \mathbf{U}_\perp is composed of the pertinent orthogonal components \mathbf{U}_\perp^+ and \mathbf{U}_\perp^- , namely

$$\begin{cases} \mathbf{U}_\perp = \mathbf{U}_\perp^+ + \mathbf{U}_\perp^- \\ \mathbf{U}_\perp = [u_{a\perp}(t) \ u_{b\perp}(t) \ u_{c\perp}(t)]^T \\ \mathbf{U}_\perp^+ = \begin{bmatrix} U_m^+ \cos\theta \\ U_m^+ \cos(\theta - 2\pi/3) \\ U_m^+ \cos(\theta + 2\pi/3) \end{bmatrix} \\ \mathbf{U}_\perp^- = \begin{bmatrix} U_m^- \cos(\theta + \delta) \\ U_m^- \cos(\theta + 2\pi/3 + \delta) \\ U_m^- \cos(\theta - 2\pi/3 + \delta) \end{bmatrix} \end{cases} \quad (33)$$

The grid voltage \mathbf{U} in the stationary coordinate frame can be obtained through real-time detection, and its pertinent orthogonal voltage \mathbf{U}_\perp is generally obtained through the differential method or the delay method; these methods are subjected to high random noise amplification or long response time. To improve the response speed and anti-noise ability, the

fast and accurate orthogonal signal generator (OSG) scheme proposed by Xiong et al. (2016a) is chosen here. This gives

$$u_\perp(k) = \frac{u(k)\cos(\omega kT_s) - u(k-K)}{\sin(\omega kT_s)} \quad (34)$$

where T_s is the sampling period, k is the discrete time step, and K is the scaling factor that takes a positive integer. In this paper, K is chosen to be 5.

3.3 PLL-Free VOC Strategy

Figure 7 shows the proposed PLL-Free VOC strategy for VSCs tied to unbalanced grids. The strategy mainly includes a constant-speed rotational coordinate frame block, a grid voltage sequence component measurement block, a VSC output current transformation block, a DC-side capacitor voltage control block, VSC output current command calculation blocks, a VSC output current control block, and a PWM signal generation block.

Unlike the basic VOC strategy (see Figure 4), the voltage and current are here formulated, measured, calculated and controlled in the constant-speed rotational coordinate frame with the proposed control strategy, which completely eliminates the PLL and its complex dynamic adjustments. This helps to significantly improve the control speed of the VSC output current, suppress the overload of the output current, and minimize the time and intensity of the overcurrent impact on the VSC.

To enable the fast and accurate tracking of the current command for the grid-tied VSC, the PLL-Free VOC strategy proposed in this paper adopts the inner current loop control

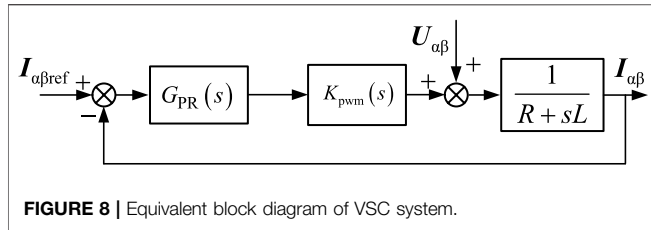


FIGURE 8 | Equivalent block diagram of VSC system.

based on the proportional resonant (PR) controller, Cheng et al. (2020), whose transfer function writes

$$G_{PR}(s) = \frac{K_{pk}s^2 + K_{ik}s}{s^2 + 2\omega_c s + (\omega_n)^2} \quad (35)$$

where ω_c is the bandwidth parameter of the PR controller with a typical value of 5–15 rad/s; K_{pk} and K_{ik} are the primary and secondary resonance coefficients, respectively, Cheng et al. (2020), and:

$$K_{pk} = \frac{L}{R} K_{ik} \quad (36)$$

The introduction of the PR controller enables the direct, real-time implementation of the current control in the stationary coordinate frame, thereby eliminating the coordinate frame transformation process related to the sequence component extraction of the grid current, and reducing the computation burden of the control strategy. Besides, to further reduce the number of control loops and the corresponding calculation amount, this paper makes use of the zero-sequence current-free characteristic of the VSC (see Figure 1) to design the current control algorithm (see Figure 7) in the $\alpha\beta$ coordinate frame. The transformation from the abc coordinate frame to the $\alpha\beta$ frame is given by

$$\mathbf{T}_{abc/\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \quad (37)$$

To simplify the analysis of current loop control parameters and their adaptability to frequency fluctuations, the influence of the outer capacitor voltage loop is neglected, since the bandwidth of the inner current loop is usually 5 times larger than that of the outer loop. Accordingly, the VSC system can be described by the equivalent block diagram in Figure 8, where $K_{pwm}(s)$ is the transfer function of the pulse width modulation (PWM) enabled VSC circuit, expressed as the ratio of its output AC voltage to the input DC voltage. In the digital realization of the PWM block, a delay of one sampling period T_s is caused by the fixed-time sampling and calculation. Besides, the modulation signal needs to remain unchanged in the next sampling period when it is loaded, and this process can be described by a zero-order holder (ZOH) with the average delay of $T_s/2$, Pan et al. (2014). Therefore,

$$K_{PWM}(s) = \frac{1}{T_s} \cdot e^{-sT_s} \cdot \frac{1 - e^{-sT_s}}{s} \cdot \frac{U}{U_{dc}} \approx \frac{1}{1.5T_s s + 1} \cdot \frac{U}{U_{dc}} \quad (38)$$

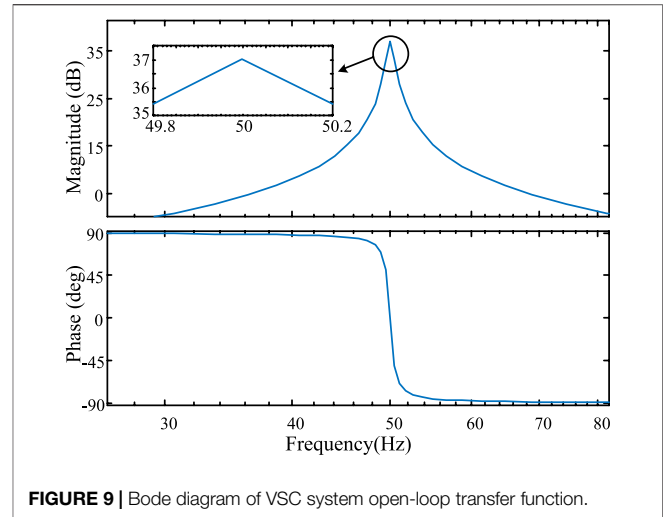


FIGURE 9 | Bode diagram of VSC system open-loop transfer function.

Accordingly, after adopting the PR controller, the output voltage of the VSC system can be described as

$$\mathbf{V}_{\alpha\beta} = K_{PWM}(s) \cdot G_{PR}(s) \cdot (\mathbf{I}_{\alpha\beta ref} - \mathbf{I}_{\alpha\beta}) + \mathbf{U}_{\alpha\beta} \quad (39)$$

The open-loop transfer function of the current control loop of the VSC system is

$$G_{ol}(s) = \frac{K_{pk}s^2 + K_{ik}s}{s^2 + 2\omega_c s + (\omega_n)^2} \cdot \frac{1}{1.5T_s s + 1} \cdot \frac{U}{U_{dc}} \cdot \frac{1}{sL + R} \quad (40)$$

The Bode diagram of the system open-loop transfer function can be obtained (see Figure 9), by substituting the VSC system parameters (see Table 1) into Eq. 40. The current loop has a gain of 37 dB at the synchronous frequency (50 Hz), indicating that the PR controller has a sufficient gain to adjust the current command value without difference. When the grid frequency fluctuates within ± 0.2 Hz, the lowest resonance gain is 35.5 dB, indicating efficient suppression of the negative-sequence current via the PR controller when the grid frequency fluctuates within the range limited by the grid code. Besides, the phase of the open-loop current transfer function at the resonant frequency is 0° , and the phase response is always maintained between -90° and 90° . This proves that the PLL-free VOC strategy proposed in this paper can effectively ensure the VSC system stability.

4 FREQUENCY ADAPTIVE SCHEME

Based on the Bode diagram in Figure 9, when the grid frequency fluctuates within the range limited by the grid

TABLE 1 | System parameters.

| Parameter | Value | Parameter | Value |
|-----------------------------|--------|------------------------------|--------------|
| DC-side voltage | 700 V | DC-side capacitor | 3.5 mF |
| Rated grid power | 7 kW | Equivalent series resistance | 0.1 Ω |
| Sampling frequency | 10 kHz | Equivalent series inductance | 2.4 mH |
| Outer voltage loop K_{PP} | 0.8 | Outer voltage loop K_{PI} | 100 |
| First resonant coefficient | 240 | Second resonant coefficient | 1 |

code, the PR controller can effectively suppress the negative-sequence current, yet ensuring the VSC system stability. However, under extreme fault disturbances, the grid voltage is severely unbalanced, and the grid frequency may also exceed the range limited by the grid code. At this time, in the absence of a frequency adaptive strategy, the current command tracking ability of the VOC strategy will be sharply reduced, thereby weakening the overcurrent suppression capability of the VSC. Focusing on this issue, this paper proposes a frequency adaptive strategy based on the frequency detection method in Xiu et al. (2021b).

First, the open-loop phase detection method in Xiong et al. (2016b) is used to obtain the real-time phase of the positive-sequence component of the grid voltage. The corresponding expression can be derived from Eq. 2, yielding

$$\begin{aligned}\sin \theta &= \sin(\omega t + \phi) \\ &= \sin[\omega_s t + (\omega - \omega_s)t + \phi] \\ &= \sin(\omega_s t + \phi_0)\end{aligned}\quad (41)$$

where ϕ_0 is the angle between the grid voltage vector and the d-axis of the constant-speed rotational coordinate frame, i.e., the initial phase of the grid voltage in the coordinate frame. Analogous to the initial phase in Eq. 2, here ϕ_0 must satisfy $\phi_0 \in [0, 2\pi)$. Therefore

$$\phi_0 = \text{mod}[(\omega - \omega_s)t + \phi, 2\pi] \quad (42)$$

It can be seen that when the grid frequency changes, the initial phase of the grid voltage is no longer invariant in the constant-speed rotational coordinate frame, but changing continuously over time.

Besides, when the grid frequency changes, the dq-axis components of the positive-sequence component of the grid voltage in the constant-speed rotational coordinate frame are

$$\begin{cases} U_d^+ = U_m^+ \cos[(\omega - \omega_s)t + \phi] \\ U_q^+ = U_m^+ \sin[(\omega - \omega_s)t + \phi] \end{cases} \quad (43)$$

Accordingly,

$$\phi_0 = \arctan\left(\frac{U_q^+}{U_d^+}\right) + \theta_{\text{ex}} \quad (44)$$

where θ_{ex} is the extra phase introduced to meet the condition $\phi_0 \in [0, 2\pi)$, and is given by Xiong et al. (2016b) as

$$\theta_{\text{ex}} = \begin{cases} 0, & U_d^+ > 0, U_q^+ > 0 \\ \pi, & U_d^+ < 0 \\ 2\pi, & U_d^+ > 0, U_q^+ < 0 \end{cases} \quad (45)$$

However, direct calculation of grid phase by Eqs 44, 45 may lead to its instability, due to the sudden transition of extra phase at the specific boundaries. The presence of random noise can cause jitters in the detected phase. To solve this issue, the extra phase $\theta_{\text{ex}}(t)$ is calculated by a hysteresis logic that considers the dead-band $[-\xi, \xi]$ (with $\xi > 0$ being the dead-band parameter) and the previous output

$\theta_{\text{ex}}(t - T_s)$. The detailed implementation is shown in **Algorithm 1**.

Algorithm 1

```

1: Input:  $\theta_{\text{ex}}(t - T_s), U_d^+(t), U_q^+(t), \xi$ 
2: if  $U_d^+(t) < -\xi$  or  $U_d^+(t) > \xi$  then
3:   if  $U_d^+(t) > 0$  then
4:     if  $U_q^+(t) < -\xi$  or  $U_q^+(t) > \xi$  then
5:       if  $U_q^+(t) > 0$  then
6:          $\theta_{\text{ex}}(t) \leftarrow 0$ 
7:       else
8:          $\theta_{\text{ex}}(t) \leftarrow 2\pi$ 
9:       end if
10:    else
11:       $\theta_{\text{ex}}(t) \leftarrow \theta_{\text{ex}}(t - T_s)$ 
12:    end if
13:  else
14:     $\theta_{\text{ex}}(t) \leftarrow \pi$ 
15:  end if
16: else
17:    $\theta_{\text{ex}}(t) \leftarrow \theta_{\text{ex}}(t - T_s)$ 
18: end if

```

To further reveal the relationship between the frequency fluctuation and the real-time phase θ , θ in Eq. 41 can be decomposed into the synchronous-frequency component θ_s and the difference-frequency component θ_d , namely

$$\theta = \theta_s + \theta_d \quad (46)$$

where

$$\theta_s = \omega_s t = 2\pi \int f_s dt \quad (47)$$

$$\theta_d = 2\pi \int (f - f_s) dt + \phi \quad (48)$$

Since ϕ is unknown, the difference-frequency phase θ_d cannot be directly calculated by Eq. 48. However Eq. 48 shows that the difference-frequency phase θ_d has a linear relationship with the grid frequency deviation, namely, increasing (or decreasing) the frequency deviation can correspondingly increase (or decrease) the difference-frequency phase. Therefore, a closed-loop system can be designed to obtain the frequency f , based on which the calculated difference-frequency phase $\hat{\theta}_d$ can be made to follow its actual value θ_d , namely

$$\hat{\theta}_d = 2\pi \int (\hat{f} - f_s) dt \quad (49)$$

When the difference-frequency phase has been tracked (i.e., $\hat{\theta}_d = \theta_d$), we have $\hat{f} = f$. The corresponding control principle can be designed as

$$\hat{f} = K_{\text{fp}}(\theta_d - \hat{\theta}_d) + K_{\text{fl}} \int (\theta_d - \hat{\theta}_d) dt \quad (50)$$

The successful implementation of this frequency detection algorithm depends on whether the difference-frequency phase θ_d can be accurately obtained. From Eqs 42, 48, we have

$$\theta_d = (\omega - \omega_s)t + \phi = 2\pi n + \phi_0 \quad (51)$$

where n (with an initial value 0) is a time-variant integer number for phase compensation, with the aim to generate a continuous θ_d over time starting from the result of ϕ_0 (calculated via Eq. 44 and Algorithm 1 and limited in 2π). Specifically, the difference between $\phi_0(t)$ in the current sampling period and $\phi_0(t - T_s)$ in the previous sampling period is evaluated; when its absolute

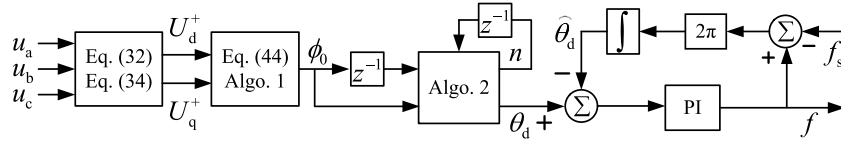


FIGURE 10 | Proposed frequency adaptive strategy.

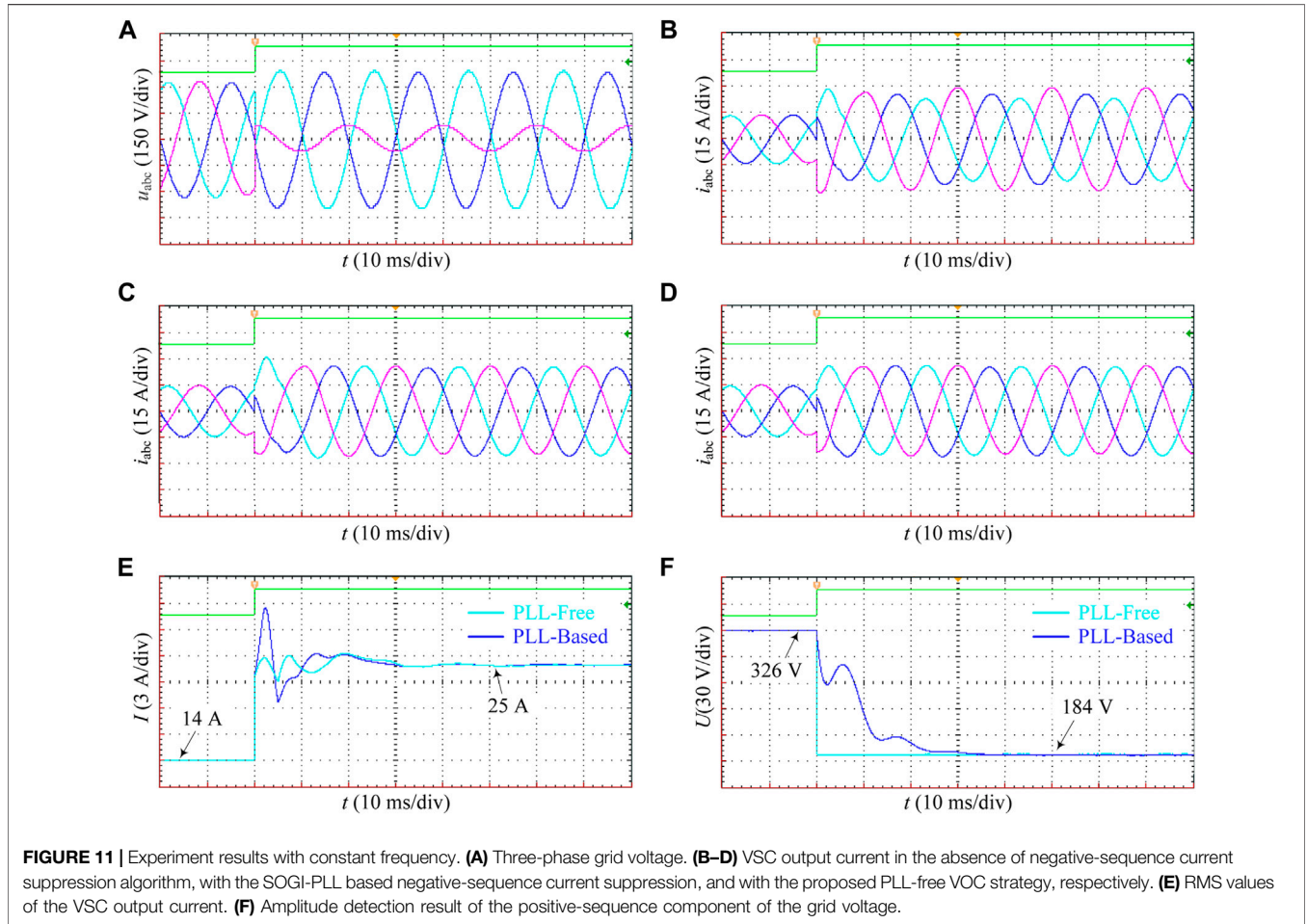


FIGURE 11 | Experiment results with constant frequency. **(A)** Three-phase grid voltage. **(B–D)** VSC output current in the absence of negative-sequence current suppression algorithm, with the SOGI-PLL based negative-sequence current suppression, and with the proposed PLL-free VOC strategy, respectively. **(E)** RMS values of the VSC output current. **(F)** Amplitude detection result of the positive-sequence component of the grid voltage.

value exceeds 2π , n is increased/decreased by 1. In discrete sampling, a small positive value σ is considered (in this paper, $\sigma = 0.01$) to be the error tolerance for detecting the absolute value change (see **Algorithm 2**). The difference-frequency phase θ_d is then calculated by **Eq. 51**.

Algorithm 2

- 1: **Input:** $\phi_0(t), \phi_0(t - T_s), n(t - T_s), \sigma$
- 2: **if** $\phi_0(t) - \phi_0(t - T_s) \leq -2\pi + \sigma$ **then**
- 3: $n(t) \leftarrow n(t - T_s) + 1$
- 4: **end if**
- 5: **if** $\phi_0(t) - \phi_0(t - T_s) \geq 2\pi - \sigma$ **then**
- 6: $n(t) \leftarrow n(t - T_s) - 1$
- 7: **end if**
- 8: $\theta_d \leftarrow \phi_0 + 2\pi n$

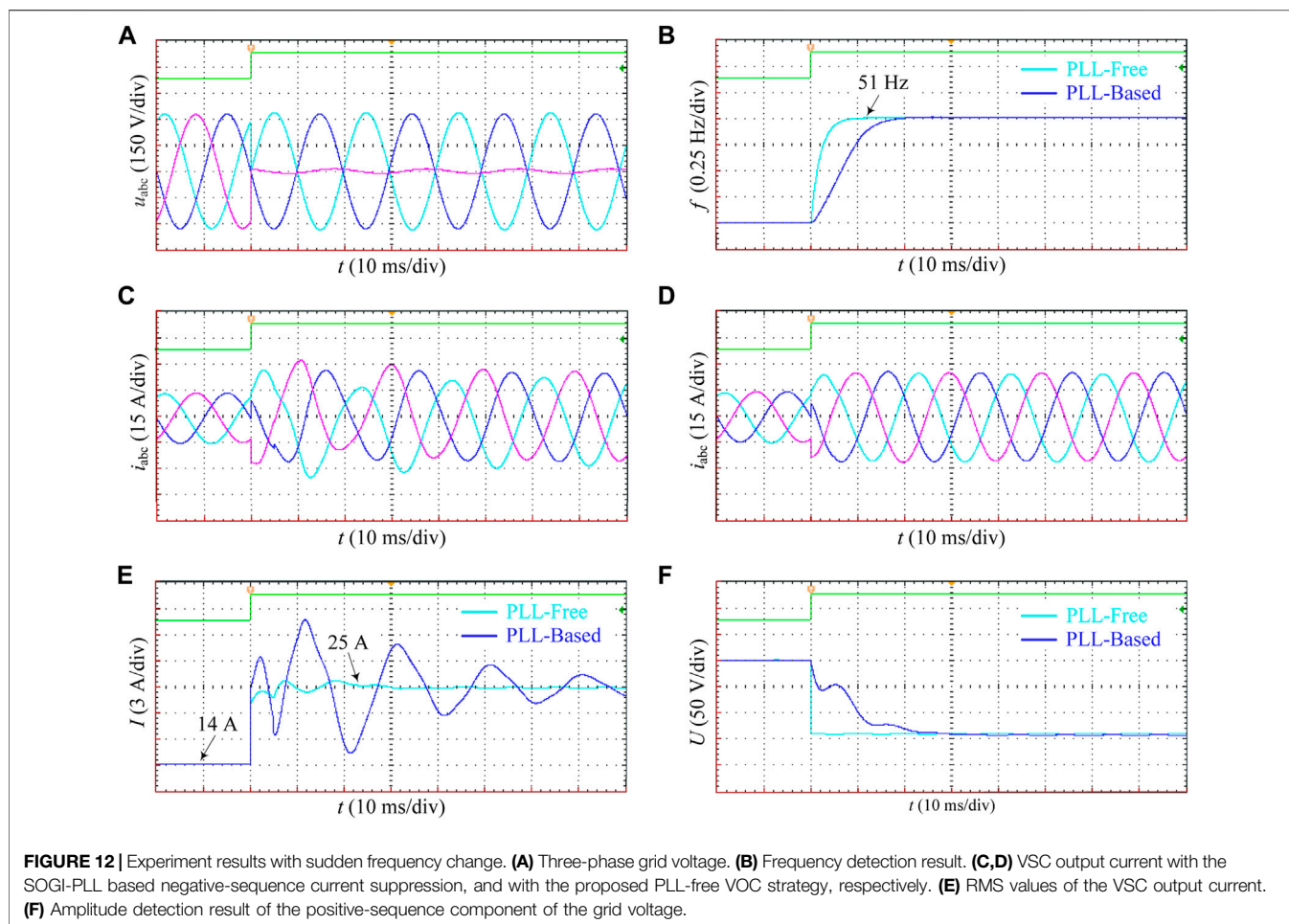
Based on the above analysis, the frequency adaptive strategy with real-time frequency detection ability is obtained, as shown in **Figure 10**.

5 EXPERIMENT RESULTS

In order to prove the feasibility and advancement of the proposed strategy, experiments have been carried out under the condition that the power grid changes from symmetrical operation to asymmetrical operation. The main parameters of the VSC system are collected in **Table 1**.

5.1 Constant Grid Frequency Scenario

In the first study, the grid is disturbed while the grid frequency is kept the same (see **Figure 11A**), and the performance of the proposed PLL-free VOC strategy is compared versus two scenarios, i.e., without the negative-sequence current suppression algorithm, and when the



negative-sequence current is suppressed based on the SOGI-PLL. The pertinent experiment results are shown in **Figure 11**.

After being disturbed, the utility grid changes from the symmetrical operation to the asymmetrical operation (see **Figure 11A**), where the voltage becomes severely unbalanced. In the absence of proper measures, this asymmetry inevitably leads to serious imbalance also in the output current of the grid-tied VSC, resulting in a significant increase in the current amplitude of some phases of the VSC, as shown in **Figure 11B**. As a result, the VSC temperature rises sharply until the equipment damages due to severe overcurrent, or the VSC is automatically disconnected by the overcurrent/overheat protection.

After using the SOGI-PLL based negative-sequence current suppression strategy, the VSC avoids the impact of long-term asymmetric current, as shown in **Figure 11C**. Though the VSC output current has been significantly improved w.r.t. the previous case, the adopted SOGI-PLL algorithm causes a long dynamic adjustment process (about 25 ms) of the VOC strategy, and the transient has a large overshoot, causing the VSC to undergo a long-term, severe current overload condition. Indeed, the

maximum VSC current during the transient even exceeded that with no negative-sequence current suppression. Hence, this SOGI-PLL based method, though effectively improves the steady-state current quality of the VSC, exhibits a poor transient adjustment ability. At this time, the VSC still suffers from the severe transient current impact that threatens the equipment performance, reliability, and safety.

When the proposed PLL-free VOC strategy is used, the VSC connected to the unbalanced grid nearly always outputs three-phase symmetrical current waveforms, as shown in **Figure 11D**. This solves both the steady-state and transient unbalance issues; the VSC completely avoids the overcurrent and overheating impacts caused by the negative-sequence current, and maintains remarkable power quality. The key reason lies in the complete removal of the PLL block that requires a complex dynamic process. The relevant physical quantities are directly measured, calculated, and controlled in the constant-speed rotational coordinate frame, requiring no longer the dynamic adjustment process, and maintaining relatively constant even during the transient. To further prove this, amplitudes of the VSC output currents are provided and compared in **Figure 11E**. The amplitude variation range has been obviously reduced from 7 A (with the SOGI-PLL based

strategy) to less than 1 A (with the PLL-free VOC strategy), and the response time has been reduced to less than 10 ms. Also, the detection speed of the positive-sequence component of the grid voltage has been significantly improved, as shown in **Figure 11F**. Though different dq coordinate frames (and thus, inconsistent dq-axis components) are used by these strategies, they provide coherent magnitude results of the positive-sequence component of the grid voltage, with the exception of calculation times.

5.2 Grid Frequency Fluctuation Scenario

To test the frequency adaptability of the proposed method, the above experiments are performed under the condition of sudden frequency change of the utility grid, and the results are shown in **Figure 12**. After the asymmetric disturbance, the grid voltage frequency is changed from 50 to 51 Hz, as shown in **Figure 12A**. Under the influence of such large frequency fluctuations, the waveform quality of the output current of the grid-tied VSC, if no measures are taken, will be severely reduced. When the SOGI-PLL based strategy is used, the grid frequency can be obtained within about 20 ms, as shown in **Figure 12B**, which is a longer time and leads to even worse transient current feature of the VSC compared to the previous constant-frequency condition. Even if better steady-state waveform quality of the VSC output current is obtained, the dynamic response time of the system is extended to nearly 80 ms, as shown in **Figure 12C**. Due to the complex dynamic tracking process of the PLL, a longer time is needed to dynamically track the amplitude, phase, and frequency of the grid voltage, due to the sudden frequency change in the grid frequency. Owing to the removal of the closed-loop detection structure, the proposed frequency detection method, which is critical for the frequency adaptability of the proposed PLL-free VOC strategy, can quickly and accurately track the grid voltage frequency; both the detection time and the transient overshoot are significantly improved compared to the SOGI-PLL, as shown in **Figure 12B**. Obviously, when the proposed strategy is adopted, the VSC maintains excellent control ability of the negative-sequence current, which is effectively suppressed in both the steady state and transient state. The control performance of the strategy is virtually unaffected by the frequency change, as shown in **Figure 12D**. Similarly, to intuitively observe the transient process, the VSC transient current amplitudes with the two strategies are compared in **Figure 12E**. After adopting the proposed strategy, the overshoot range of the transient current amplitude is reduced remarkably to less than 1 A, and the transient response time is reduced to 12 ms. The control ability of VSC under asymmetric utility grid conditions has been significantly improved. Similarly, the detection speed of the positive-sequence component of the grid voltage has also been significantly improved, which is achieved almost instantaneously, as shown in **Figure 12F**.

6 CONCLUSION

This paper analyzes the technical challenges faced by the conventional PLL-based VOC strategy under unbalanced grid conditions, and proposes a PLL-free VOC strategy, along with its detailed implementation, for VSCs tied to unbalanced utility grids. Finally, experiments are conducted for verification. The main conclusions are as follows.

1. Under the severely asymmetrical working condition of the utility grid, the PLL is difficult to achieve a good compromise between the response speed and the anti-interference ability, due to the large amplitude of the double-frequency voltage component. Accordingly, the PLL-based VOC scheme is difficult to effectively suppress the negative-sequence current in the transient process, and even aggravates the transient current asymmetry and the resulting overcurrent problem, causing the power semiconductor devices to suffer from a significant thermal fatigue and damage for a long time.
2. The proposed PLL-free VOC strategy for VSCs tied to unbalanced grids completely removes the PLL and its complex dynamic adjustment process. The voltage and current required for VSC control are described, measured, calculated, and controlled in a constant-speed rotational coordinate frame. This significantly increases the control speed of the VSC output current and mitigates its overload, thereby minimizing the time and intensity of VSC suffering from overcurrent impact.
3. Unlike the conventional PLL method that measures the frequency first and then calculates the phase, the frequency detection method proposed in this paper dynamically tracks the grid frequency information based on the difference-frequency phase, which is caused by the frequency variation and can be quickly captured. Therefore, the VSC system can obtain the phase information necessary for the VOC strategy faster, and also accurately capture the grid frequency information, making the proposed PLL-free VOC strategy adaptive to large fluctuations of the grid frequency.
4. Experimental results prove the rapidity and accuracy of the proposed PLL-free VOC strategy in suppressing the VSC transient/steady-state negative-sequence current, and the effectiveness and superiority of the proposed frequency detection method. Also, the frequency adaptability of the proposed strategy is illustrated.

DATA AVAILABILITY STATEMENT

The original contributions presented in the study are included in the article/supplementary material, further inquiries can be directed to the corresponding author.

AUTHOR CONTRIBUTIONS

All the authors conceived and designed the study. LsX, BW, and LcX performed the simulation and experiment, and wrote the manuscript with the guidance from XL. BW and DW conceived and designed the experiments.

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Conflict of Interest: Author DW was employed by the State Grid Jiangsu Maintenance Company.

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