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High sensitivity transparent photoconductors in voltage-controlled silicon waveguides

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On-chip optical power monitors are essential elements to calibrate, stabilize and reconfigure photonic integrated circuits (PICs). Many applications require in-line waveguide detectors, where a trade-off has to be found between large sensitivity and high transparency to the guided light. In this work, we demonstrate a transparent photoconductor integrated on standard low-doped Silicon-on-Insulator waveguides that reaches a photoconductive gain of more than 10^6 and an in-line sensitivity as high as -60 dBm. This performance is achieved by compensating the effect of electric charges in the cladding oxide though a bias voltage applied to the chip substrate or locally through a Gate electrode on top of the waveguide, allowing to tune on demand the conductivity of the core to the optimum level.

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The evolution of integrated photonics towards large scale of integration and programmable circuits requires the development of sophisticated tools for the calibration, stabilization and reconfiguration of PICs. Power monitors integrated on chip are key devices providing the required feedback signal to implement control algorithms [1]. To increase the topological complexity of PICs without increasing control complexity in proportion, in-line detectors can be used to provide a multipoint monitoring of the PIC and enable control partitioning into local feedback loops, disentangling large multivariable problems to subsets of simpler cases operated in parallel. The ideal in-line waveguide monitor measures the light power in an optical waveguide (WG) with a high sensitivity, but without absorbing photons in excess with respect to the native loss of optical waveguides.

In silicon PICs operating in the near-IR wavelength range, in-line monitoring is conventionally performed by using germanium photodiodes (PD), that absorb a small portion of the light spilled out of the WG through power taps [2]. Although being simple and effective, tap detectors cannot be used to monitor the light inside those photonic architectures where insertion losses are a critical parameter, such as in high quality factor resonators or meshes of Mach-Zehnder interferometers [3]. To solve this issue, examples of (quasi)transparent detectors in silicon have been reported in literature, exploiting the native free-carriers generation occurring in the WG core due to surface state absorption to realize integrated photodiodes [4] and photoresistors [5–7]. The main drawback of sub-band gap detectors is the small signal they provide, that increases the complexity of the read-out electronics. This aspect can be solved by exploiting the intrinsic gain mechanism of photoresistor [8]. Transparent photoresistors have been demonstrated in literature but they have often been proposed with an additional doping of the WG core to about 10^{17} cm^{-3}, a level that increases the WG attenuation.

We propose an integrated photoresistor directly made on the low-doped silicon layer of a standard Silicon Photonics SOI technology, that overcomes these limitations and demonstrates extremely high sensitivity to light. In contrast to doped devices, the proposed photoresistor has the advantage of using the native silicon layer without additional technological steps, of reducing the optical losses generated when doping the WG and of ensuring much lower operating currents even at the high bias voltages necessary to decrease the carriers transit time. Fig. 1 illustrates the cross-section of the photoconductor. The device is embedded in a rib WG with 500 nm × 220 nm core, 900 nm × 90 nm

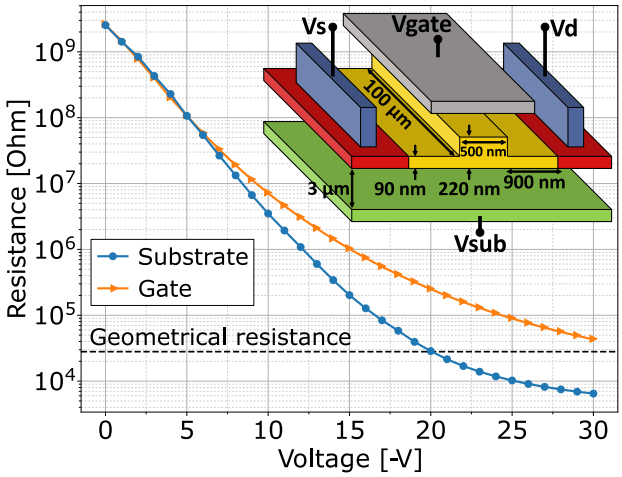

Fig. 1. Measured resistance of a transparent photoconductor embedded in a silicon rib waveguide (inset) as function of the control voltage applied to the Gate electrode or chip substrate.

slabs and a total length of 100 µm. The photoresistor has been designed with a p-i-p structure: the silicon WG core and the optical slabs have the same 10^{15} cm^{-3} p-type doping of the original SOI wafer, while the external slab regions (named Drain and Source) are heavily p-doped (10^{20} cm^{-3}) to ensure ohmic electrical contacts. The 900 nm distance of the electrical contacts from the WG core guarantees that no additional propagation losses are introduced. The box oxide is 3 µm thick.

Two are the key features of the proposed device: a "Gate" metal electrode deposited 700 nm over the WG and an ohmic contact to the substrate of the chip. They have been introduced to counteract the effects of the unavoidable positive electric charges present within the oxide surrounding the WG and at the Si/SiO_2 interface. These charges have been demonstrated to modify the actual carrier concentration in the device with respect to the local doping level, by electrostatically repelling the free holes towards the contacts [9]. Consequently, the resistance of the WG is much larger than what expected, in the order of few GΩ in our case with respect to the expected 28 kΩ value given by the doping level and the geometry of the device. However, by applying a voltage to one of the additional electrodes, the effect of oxide charges can be compensated (Fig. 1) and the resistance of the photoconductor can be tuned: as the substrate or Gate potential goes negative with respect to the Source contact, the fixed positive oxide charges are electrostatically counteracted and the holes concentration in the WG increases, consequently decreasing the device resistance towards the nominal value of 28 kΩ or even lower if oxide charges are overcompensated. The Gate electrode and the chip substrate can both be effectively used to perform this action, the substrate operating on all the devices in the chip simultaneously while the Gate having a more local effect. The weaker effect of the Gate, noticed in Fig. 1, is likely due to its smaller area as compared to the chip substrate and to the shape of the WG.

Fig. 2 reports the sensitivity curve (photocurrent vs light intensity in the WG) of the device when operated with $V_{sub} = -30$ V (blue curve). The photoconductor allows to reach in-line detection of light intensities down to −60 dBm. To highlight the extraordinary performance that can be achieved with a low doped photoresistor, we have compared it with a commonly doped device and with a p-i-n photodiode. The three devices differ just for the doping type and level of WG and slab regions while they all have the same geometry. The doped photoresistor in particular has a n^+-n-n^+ structure: n^+-doped slabs with a doping concentration of 10^{20} cm^{-3} and n-doped core with a doping concentration of 10^{17} cm^{-3}, leading to a resistance around 60 Ω. Its sensitivity curve is shown in Fig. 2 in green at the same V_{ds} voltage of 1 V. It is clearly seen that the produced photocurrent is lower by more than one order of magnitude with respect to the low-doped device, thus resulting in a light intensity detection capability limited to about −35 dBm. The same figure also reports the photodiode sensitivity as a reference for the primary current I_0 directly generated in the WG without the amplification mechanism of the photoresistors.

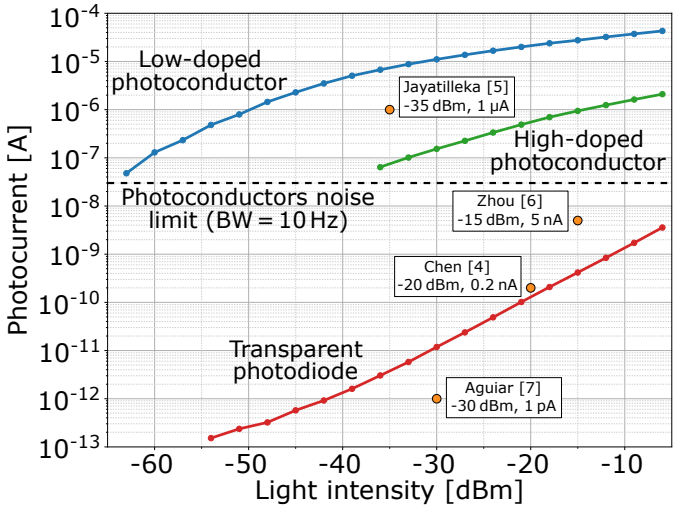

Fig. 2. Sensitivity of the low-doped photoconductor operated at $V_{sub} = -30$ V (blue), compared to a 10^{17} cm^{-3} n-doped photoconductor (green) of identical geometry. Both devices are biased with the same V_{ds} of 1 V. The current of an in-line transparent p-i-n photodiode of identical geometry (red) is plotted as reference. For comparison, the performance of other state-of-the-art transparent detectors is also indicated.

To better understand the reasons for the much better performance of a low-doped photoresistor compared to a standard doped one and to highlight the importance of the substrate/Gate voltage tuning on the photogenerated current I_{pr}, it can be useful to recall the expression of I_{pr} in terms of primary current I_0 and photoresistive gain G_r [10]:

$$I_{pr} = I_0 G_r$$
$$G_r \propto \frac{\tau_{life}}{\tau_{transit}} \quad \textbf{(1)}$$

where τ_{life} is the life time of the intra-gap trap site that generates the free carrier in the WG and $\tau_{transit}$ is the time spent by a free carrier to cross the device (holes in this case). According to the equation, the primary current I_0 is amplified by the photoresistive gain G_r, proportional to the ratio between the trap life time and the carriers transit time. The ohmic contacts of the photoconductor, guaranteed by the high doping of the slabs, allow a charge to be injected and to recirculate in the WG when one free carrier reaches the end of the device. This ensures electrostatic balance for the entire life time of the photogenerated trap site, which can be much longer than the carrier transit time. Thus, differently from a photodiode, a single event of photogeneration gives its contribution to the total current for a time longer than the carrier transit time. This recirculating gain mechanism amplifies the signal at the expense of a slower response [11], i.e. a smaller detection bandwidth, limited by the trap life time.

Concerning the role of the substrate/Gate voltage on the sensitivity of the low doped photoconductor, Fig. 3 shows the sensitivity curve at $V_{ds} = 1$ V for 3 different values of the substrate voltage. The figure highlights how the photocurrent can be increased by several orders of magnitude by properly tuning the WG conductivity with the substrate/Gate voltage, reaching an amplification factor of about 10^6 when −30 V are applied. The figure again reports, for comparison, the photocurrent I_{pd} of the p-i-n photodiode. Being the geometry of the devices the same, the photodiode current I_{pd} is equal to the primary current I_0 in eq. 1. The ratio I_{pr}/I_{pd} is thus a direct measurement of the photoresistive gain G_r, whose dependence on the light intensity is shown in the inset of Fig. 3.

Simulations of the device with Sentaurus TCAD Software (Synopsys Inc., Mountain View, USA) where performed to gain a better insight on the behaviour of the photoconductor as a function of the substrate/Gate voltage. Fig. 4 shows the velocity of the holes in their motion from Source to Drain at different

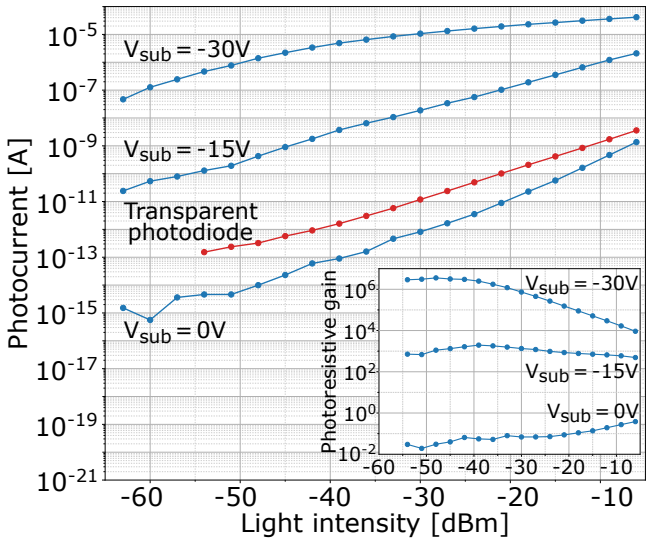

Fig. 3. Sensitivity curve of the p-i-p photoresistor (blue) at $V_{ds} = 1\,\mathrm{V}$ with different substrate voltages (0 V, −15 V, −30 V) and of the p-i-n photodiode (red). The inset highlights the photoresistive gain at different substrate voltages as function of WG light intensity, computed as ratio I_{pr}/I_{pd}.

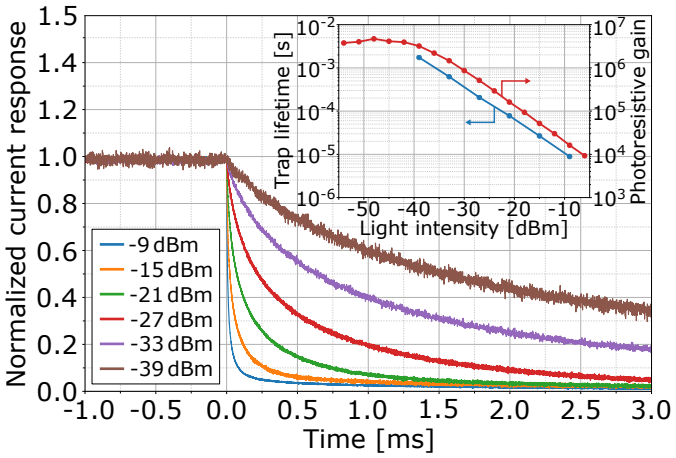

Fig. 5. Normalized photocurrent of the photoconductor ($V_{sub} = -30\,\mathrm{V}$) when the input light is a step-like signal of different intensities. The trap life time extracted from the time constant of the responses is plotted in the inset together with the photoresistive gain, revealing the same dependence on light.

substrate voltages. The simulations show that at small substrate potentials, when the device is depleted from carriers by the oxide charges, the externally applied voltage $V_{ds} = 1\,\mathrm{V}$ drops almost entirely on the thin slab regions, leaving only a small fraction across the thicker WG core and consequently limiting the velocity of the carriers in this region. This causes the photoresistive gain to be very low since the photogenerated charges experience a very long transit time with respect to traps life time. Note from Fig. 3 that in the case of $V_{sub} = 0\,\mathrm{V}$ the photogenerated current is even lower than I_{pd}, meaning that a fraction of the photogenerated carriers does not even reach the contacts before recombining. Instead, when the substrate/Gate voltage is increased sufficiently, the waveguide recovers its original doping level and the external $V_{ds} = 1\,\mathrm{V}$ is distributed over the full section of the device, increasing the carriers velocity to its maximum and thus ensuring the highest photoconductive gain, as highlighted in Fig. 3 for the case of $V_{sub} = -30\,\mathrm{V}$.

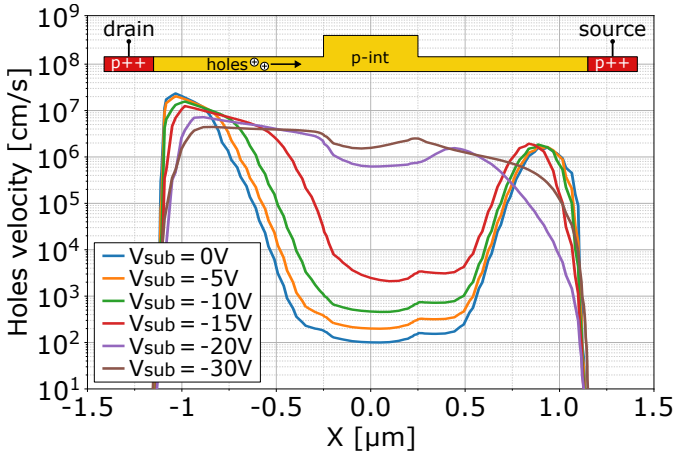

Fig. 4. Transversal holes velocity in the low-doped photoconductor operating at $V_{ds} = 1\,\mathrm{V}$ for different chip substrate voltages. The WG cross-section is also shown for reference.

The photoconductive gain G_r in the inset of Fig. 3 shows a dependence on the light intensity, with a reduction at high optical power. Referring to eq. (1), the gain decrease can be attributed to a reduction of the traps life time when light with an intensity higher than −40 dBm propagates in the WG. In these conditions, photogeneration increases the concentration of free carriers in the core to a level much higher than the dark baseline, causing a reduction of traps life time [12] and consequently of the gain G_r. This effect is more pronounced at high V_{sub} and V_{Gate}, where the transit time is short and well defined. The dependence of the traps life time on the light intensity in the WG has been further assessed by analysing the device response to step-like light signals of different amplitudes. Fig. 5 shows the normalized current responses of the device for optical powers ranging from −39 dBm to −9 dBm. Being the bandwidth of the transimpedance amplifier (TIA) used for the measurements around 100 MHz, the transient time of the observed responses is limited by the traps life time in the device under test. The inset of the figure shows the traps life times as function of the light intensity, computed by fitting the device step responses. On the same graph, the photoresistive gain at $V_{sub} = -30\,\mathrm{V}$ (as in Fig. 3) is also plotted. Since the traps life time changes by an equal factor with respect to the photoresistive gain, this result confirms that the reduction of the photoresistive gain observed in Fig. 3 is due to a reduction of the traps life time. According to this discussion, doping the WG core, as it happens in the n^+-n-n^+ photoresistor, has no beneficial effect on device performance. On the contrary, it further reduces the traps life time and consequently the photoresistive gain, leading to a lower sensitivity to light as confirmed by the experimental measurements.

To now stress the interplay between carrier transit time and photoresistive gain, Fig. 6 shows the increase of the photocurrent when the voltage V_{ds} goes up to 5 V. A high voltage across the device produces a low transit time of free carriers, that translates into a high photoconductive gain and thus current signal. Thanks to the low doping of our photoconductor, values of V_{ds} up to 5 V can be applied without having to handle large dark currents. The doped device instead, having a much smaller resistance, would generate a much higher standing current, requiring

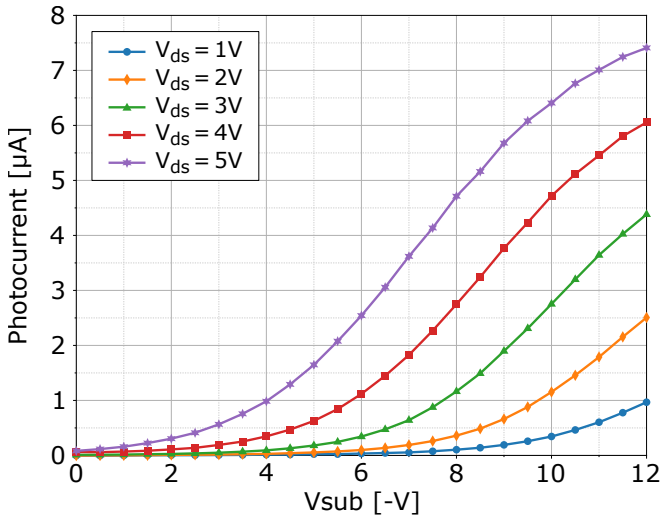

Fig. 6. Increase of the photogenerated current when V_{ds} is raised up to 5 V, as a function of the chip substrate voltage. The estimated light intensity in the WG was −10 dBm.

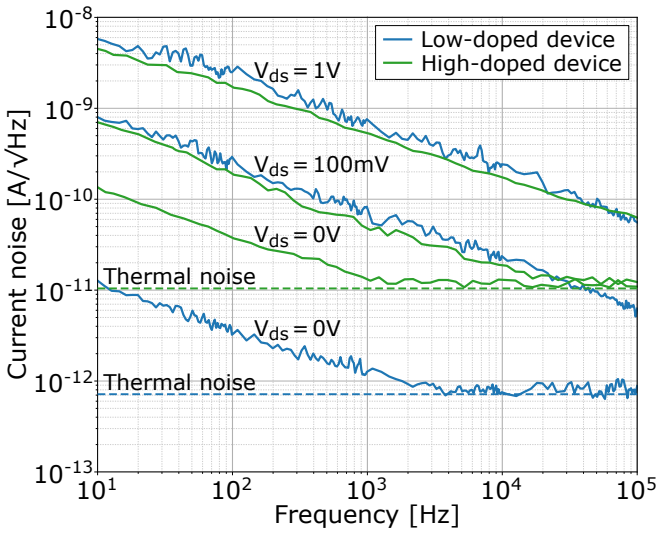

Fig. 7. Current noise power spectral densities of the two photoconductors when V_{ds} is 0 V, 100 mV and 1 V, revealing a bias-dependent $1/f$ component ($V_{sub} = -30$ V for the low-doped device).

a readout TIA with small transconductance gain not to reach saturation. A small gain makes it harder to detect small photocurrent variations, contributing to worsening the performance of the device. In addition, the high dark current also translates into a high power dissipation in the device, that heats up the WG and changes its refractive index. The p-i-p device instead, having a dark current more than two orders of magnitude lower, can be instead operated at negligible power dissipation.

As a final aspect in the comparison between the two types of photoresistors, their noise behaviour have been investigated. In terms of thermal noise, the low-doped photoconductor shows a much lower current noise $i_n = \sqrt{4kT/R}$ than the high-doped one, in proportion to their resistances. This aspect would play in favour of the low-doped device and would additionally justify its higher sensitivity. Fig. 7 shows the current noise power spectral density measured at V_{ds} bias voltages of 0 V, 100 mV and 1 V in both devices [13]. The measurements confirm that, when $V_{ds} = 0$ V, the noise of both photoresistors is in agreement with their thermal noises (the residual $1/f$ noise measured at very low frequencies is in this case attributed to the measuring instrument). However, as soon as the devices are biased, they both show an unexpected yet comparable bias-dependent $1/f$ component. This $1/f$ component follows Hooge's law [14] and the corner frequency is proportional to the square of the current in the device. Because of this, the two photoconductors are equivalent in terms of noise when operated at the same bias voltage, unless a readout frequency larger than the noise corner of the doped device is targeted. The better performance in terms of sensitivity of the low-doped sensor should thus be attributed only to its higher photoconductive gain.

In conclusion, a low doped silicon layer allows to realize in-line photoconductors with a much higher sensitivity than the commonly used doped devices, as a consequence of the larger ratio between traps life time to carriers transit time. All these aspects allow to detect light variations down to −60 dBm, with the only requirement of adding a Gate electrode over the WG core or to access the substrate voltage to compensate the effect of oxide charges. The higher sensitivity of the low-doped device is achieved thanks to its larger photoconductive gain, while the noise level has been observed to be the same as the doped detector due to a bias-dependent $1/f$ component.

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Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper may be obtained from the authors upon reasonable request.

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