A Stability Condition for Constant-On Time Buck Converters Suitable for Automotive Applications

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***Abstract*—Approximate stability boundaries for Constant ON-Time buck converters are derived and verified against numerical results obtained by bifurcation analysis. These boundaries are given as analytical expressions involving the main Constant ON-Time (COT) buck converter parameters. They allow the designer to avoid the appearance of the pulse bursting phenomenon. A case study is proposed having in mind automotive applications, which are charaterized by a wide input-voltage range. The input-voltage and the output-capacitor equivalent series resistance, that is typically poorly controlled for many types of capacitors, were chosen as bifurcation parameters.**

***Index Terms*—Constant on time buck converter, COT, pulse bursting, hybrid dynamical systems, bifurcation analysis.**

I. Introduction

Constant ON-Time (COT) buck converters are popular in wide input-voltage range applications for many reasons, e.g., the ease of control design over varying input voltage conditions, the absence of jittery ON-time behavior which affects constant-frequency control methods when incurring in minimum controllable ON-time limitations, and, provided that the ON-time is adapted to the input voltage, the ability to maintain a reasonably constant switching frequency over the input-voltage range. Many wide-input-range adaptive COT regulators, targeted to automotive and other wide-input-range applications, are available from various IC vendors [1]–[4].

It was found, both experimentally and from circuit simulations, that the architecture described in Fig. 1 can experience some stability issues at high duty cycle values, especially when the converter nominal switching frequency is intentionally lowered to maximize the duty cycle range achievable under minimum ON-time limitations. Instability is experienced in terms of pulse-bursting [5]–[8], viz. sub-harmonic oscillations.

It is well known that for a given output capacitor value, its equivalent series resistance (ESR) (R_e in this paper) is a critical parameter for stable operation. Unfortunately, R_e is typically poorly controlled for ordinary types of capacitors, and might also be heavily affected by temperature variations.

Using space-state and bifurcation analysis, this paper reveals an articulated relationship between the allowable input voltage range and the R_e of the output capacitor(s) for stable operation of the COT buck converter. Notably the stability boundaries, involving bifurcations of the circuits dynamics, were approximately derived in closed form, and presented in graphical form. This is a significant added-value for the designer since these formulae are easy to handle and quite accurate w.r.t. the exact results from time-consuming bifurcation analysis.

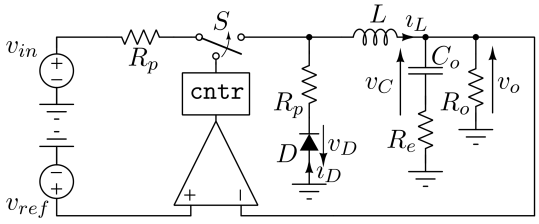

Figure 1. Schematic of the buck COT converter.

II. The buck COT converter dynamics

The dynamic evolution of the v_C and $\imath_L$ state variables of the COT converter in Fig. 1 is governed by the hybrid planar dynamical system [9] yielding the following ordinary differential equations (ODEs)

$$\begin{cases} \dot{\imath}_L = \dfrac{\varpi}{L_o}\left[\xi v_{in} - \imath_L\left(\dfrac{R_e R_o}{R_e+R_o}+R_p\right) - \dfrac{R_o v_C}{R_e+R_o}\right] \\ \dot{v}_C = \dfrac{\imath_L R_o - v_C}{C_o(R_e+R_o)} \end{cases}, \tag{1}$$

where the dot is a shorthand for the time derivative (i.e., $\dot{\imath}_L = {}^{d\imath_L}/_{dt}$), the r.h.s. can be collected in the $\boldsymbol{f}^{(\varpi,\xi)}(\imath_L, v_C)$ vector field, and both ξ and ϖ can be either 0 or 1. These binary variables can be interpreted as digital state variables [10]. In particular, ϖ is ruled by the D diode in Fig. 1, which avoids a negative $\imath_L$ current[1]. This component is modeled through a piecewise-linear ideal driving-point characteristic, $\imath_D = 0$ for $v_D \leq 0$ and $v_D = 0$ for $\imath_D \geq 0$. Whenever the switch S is open, and $\imath_L = 0$, we have $\varpi = 0$ and consequently $\dot{\imath}_L = 0$. In the $(\imath_L, v_C)$ state-plane, the solution of system (1) starts sliding on the vertical axis $\imath_L = 0$. The ϖ control variable is set to 1 as soon as $\imath_L > 0$ and this occurs since a further control logic is implemented by the `cntr` block in Fig. 1. If the COT converter admits a periodic steady-state, i.e., a limit cycle, during which $\varpi = 0$ for a certain time interval, the

[1]Actually, in modern architectures such as synchronous buck converters, to enhance converter efficiency the diode is replaced by a low-side MOSFET which is operated as a synchronous rectifier.

COT converter is said to work in discontinuous current mode (DCM). In this paper we focus on the continuous current mode (CCM) working condition only, which is obtained if the sliding condition $\varpi = 0$ is never observed.

The `cntr` block governs the ξ control variable as follows.

`Step 1:` ξ is set to 1 any time the output of the comparator becomes positive, i.e., the controller catches the positive edge of the $v_{ref} - v_o$ signal. The S switch is closed for the Δt_{ON} *fixed* time interval (ON-phase). In adaptive COT control (i.e., pseudo constant-frequency in CCM operation and low losses), the duration of this interval is given by

$$\Delta t_{\text{ON}} = \frac{k}{f_{sw}} \frac{v_{ref}}{v_{in}} \ , \tag{2}$$

where v_{ref} is the desired output voltage, v_{in} is the input voltage, f_{sw} is the maximum nominal switching frequency, and $k \in [1, k_{\text{MAX}}]$. k allows an optional adjustment of the desired switching frequency below its maximum nominal value, and it is under user control (typically implemented by adding or changing external resistors). In wide-input-range applications, this adjustment is frequently used to extend the maximum achievable duty cycle under given minimum OFF-time constraints, to maintain output voltage regulation even at the lower end of the input voltage range. It is also used to optimize the switching frequency for best efficiency in a particular (i.e., nominal) operating condition and under given circuit size constraints.

`Step 2:` At the end of the ON-phase, S is opened and is kept open for the $\Delta t_{\text{OFF}}^{\text{min}}$ *fixed* time interval (minimum OFF-phase). ξ is set to 0. This phase is necessary in practical designs for various reasons, which include, for example, reliable implementation of anti-cross conduction control of the power switches, the recharge of the bootstrap capacitor in N-channel high-side topologies, or the acquisition of the current signal during the OFF-phase for circuit protection purposes.

`Step 3:` At the end of the $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\text{min}}$ time interval, the controller checks the output of the comparator. If $v_{ref} - v_o < 0$, the S switch remains open (OFF-phase with $\xi = 0$) until the condition at `Step 1` becomes true. Otherwise, if $v_{ref} - v_o$ is still positive, the S switch is immediately re-closed and a new ON-phase starts. The overall duration of the OFF-phase is $\Delta t_{\text{OFF}} \geq \Delta t_{\text{OFF}}^{\text{min}}$. To be able to properly and efficiently adjust the v_o output voltage, keeping it as close as possible to the v_{ref} reference voltage, it is necessary to avoid $\Delta t_{\text{OFF}} = \Delta t_{\text{OFF}}^{\text{min}}$ minimum duration OFF-phases.

The $v_{ref} - v_o > 0$ condition naturally induces the manifold $\Sigma = \{(\imath_L, v_C) | h(\imath_L, v_C) = 0\}$ (see Fig. 2), where

$$h(\imath_L, v_C) = v_{ref} - v_o = v_{ref} - \frac{R_o(\imath_L R_e + v_C)}{R_e + R_o} \ , \tag{3}$$

whose normal vector is $\boldsymbol{\eta} = (1, R_e)^{\text{T}}$. The Σ' manifold in Fig. 2 is a straight line and it is the locus of points that can be reached in the Δt_{ON} time interval, starting from Σ.

On the whole, the dynamics of the COT converter is described by an autonomous piecewise linear dynamical system whose $\boldsymbol{\gamma}_1$ *simplest* steady-state trajectory, in CCM, generically

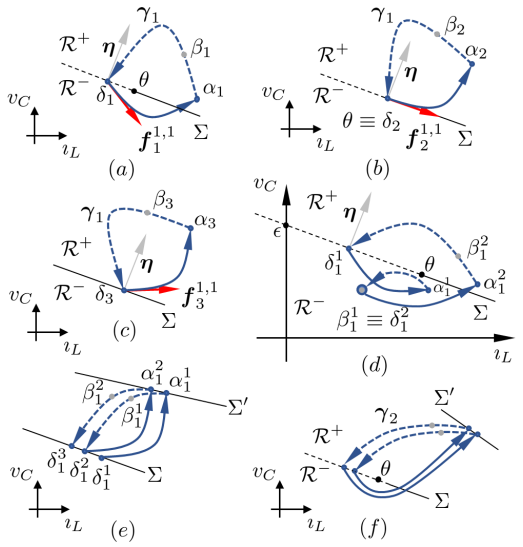

Figure 2. (a)-(c) Sketches of CCM $\boldsymbol{\gamma}_1$ limit cycles whose positioning w.r.t. Σ depends on the sign of the $\boldsymbol{f}_j^{(1,1)} \cdot \boldsymbol{\eta}$ ($j \in \{1,2,3\}$) scalar product (for compactness the $^{(1,1)}$ superscript is dropped). The scalar product is null at θ. (d) A limit cycle made up of four "segments"and one of those (from α_1^1 to β_1^1) lasts $\Delta t_{\text{OFF}}^{\text{min}}$. (e) A $\boldsymbol{\gamma}_2$ limit cycle is not allowed if $\boldsymbol{f}^{(1,1)} \cdot \boldsymbol{\eta} > 0$ in the neighborhood of δ_1^1 and δ_1^2. To have $\delta_1^3 \equiv \delta_1^1$ the dashed trajectories should intersect. (f) A $\boldsymbol{\gamma}_2$ limit cycle is potentially admitted if δ_1^1 a δ_1^2 are sufficiently close to θ.

belongs to the $\imath_L > 0$ half-plane. Some examples of this kind of dynamics are sketched in Fig. 2(a,b,c). In particular, three different situations are depicted in which at δ_j, which corresponds to the beginning of the ON-phase, we have $\boldsymbol{f}_j^{(1,1)} \cdot \boldsymbol{\eta} \lessgtr 0$ ($j \in \{1,2,3\}$). The sign of this scalar product reveals whether the orbit, during the ON-phase, is allowed to visit the $\mathcal{R}^-$ region or it is confined in $\mathcal{R}^+$. This scalar product is null at θ, negative in the dashed portion of the manifold, and positive in the solid one.

III. Stability analysis

Since the dynamical system in (1) is piecewise linear, limit cycles exist thanks to the interaction between its discontinuous vector field and the decision process governing the switching events. Bifurcations inducing changes in the stability of these limit cycles can be detected both through their Floquet multiplier (e.g., flip and fold bifurcations) and monitoring the interaction between the orbits and the switching boundaries in the state space (e.g., grazing, contact, and border collision bifurcations) [9], [10]. Furthermore, the COT converter exhibits delayed switching events too [11]. They are triggered (and scheduled) as a consequence of the interaction between the trajectory and a manifold in the state, but they actually occur after a finite amount of time. More specifically, in our case this happens at the beginning of the ON-phase, when the Σ manifold is hit at δ_j (see Fig. 2(a)-(c)). This implies an *immediate effect*, i.e., ξ is set to 1, and two *delayed effects*. (i) ξ is set to 0 after the Δt_{ON} fixed amount of time (see the α_j points); (ii) after $\Delta t_{\text{ON}} + \Delta t_{\text{OFF}}^{\text{min}}$ (see the β_j points) the `cntr` block checks whether or not $v_{ref} - v_o$ is still lower than 0

(i.e., β_j is below Σ as β_1^1 in Fig. 2(d)), and this may trigger the sudden beginning of a new ON-phase.

The stability boundaries the designer is interested in are those corresponding to the appearance of the pulse-bursting phenomenon [5], [6], viz. the generic $\boldsymbol{\gamma}_1$ limit cycle in Fig. 2(a)-(c) becomes unstable, undergoing, for instance, a period-doubling bifurcation.

The dynamics becomes more complex and the spectrum of the v_o output voltage becomes richer as shown in Sec. IV. This may occur also in case a limit cycle as the one in Fig. 2(d) appears through a global bifurcation. At β_1^1 the trajectory is still in $\mathcal{R}^-$ and thus, according to `Step 3` of the `cntr` block logic, a new ON-phase begins. This is the reason why $\delta_1^2 \equiv \beta_1^1$. The subsequent β_1^2 belongs to $\mathcal{R}^+$ and the limit cycle finally closes in its starting point δ_1^1. It is worth noticing that this kind of trajectory can be observed only if visiting $\mathcal{R}^-$ is allowed, viz. $\boldsymbol{f}^{(1,1)} \cdot \boldsymbol{\eta} < 0$ at δ_1^1.

From the applications' perspective, it is profitable to choose R_e and the v_{in} supply voltages as bifurcation parameters thus deriving stability boundaries on the (R_e, v_{in}) plain. Despite the fact that this approach provides accurate results, it is not feasible to adopt it to derive simple design rules, viz. closed form constraints involving circuit parameters, which in turn could be easily used to (approximately) identify the aforementioned bifurcation curves.

In [12], [13] a sufficient condition to avoid the arising of the pulse-bursting phenomenon was presented by imposing that $\theta \equiv \epsilon$ in Fig. 2(d). The rationale of that condition is that if the dynamics of the system can take place only in $\mathcal{R}^+$, one can observe $\boldsymbol{\gamma}_1$ limit cycles only. Indeed, Fig. 2(e) and Fig. 2(f) reveal that a $\boldsymbol{\gamma}_2$ limit cycle, viz. the simplest sub-harmonic steady-state orbit that one could sketch, may exist only if it appears in the neighborhood of the θ point. Furthermore, to have a limit cycle as the one in Fig. 2(d), the trajectory must penetrate Σ at the beginning of the ON-phase. The dynamics of the systems is constrained in $\mathcal{R}^+$ by imposing that Σ is fully *reflective* for $\imath_L > 0$, i.e.,

$$\boldsymbol{f}^{(1,1)}\Big|_{\Sigma|_{\imath_L>0}} \cdot \boldsymbol{\eta}^{\mathrm{T}} > 0 \ . \tag{4}$$

In practice, whenever the OFF-phase ends on Σ, the vector field pushes it to evolve above the manifold itself during the subsequent ON-phase. The condition was derived without a particular rule governing Δt_{ON}, that remained a free parameter. Here we assume that (2) holds and thus (4) is equivalent to

$$R_o(\imath_L \Theta + C_o R_e (v_{in} - v_{ref})) - L_o v_{ref} > 0 \ , \tag{5}$$

where $\Theta = L_o - C_o R_e R_p$. Under the reasonable assumption $\Theta > 0$, if (5) is verified for $\imath_L = 0$ then it is satisfied for any $\imath_L \geq 0$ and it can be written as:

$$v_{in} - v_{ref}\left(1 + \frac{L_o}{C_o R_e R_o}\right) > 0 \ . \tag{6}$$

This condition, which induces the Γ_s boundary in Fig. 3, despite being a sufficient condition to avoid pulse-bursting, not subject to any approximation, as shown, is extremely

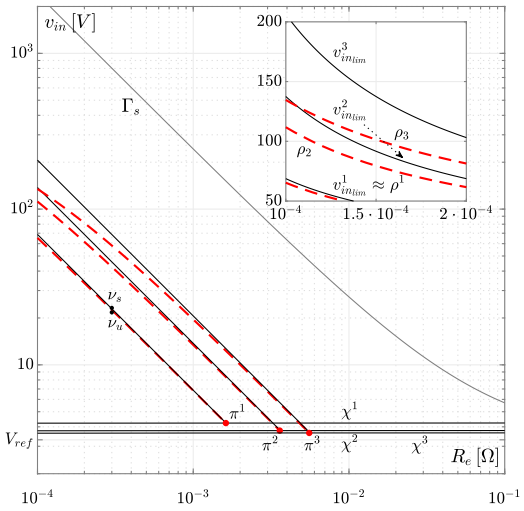

Figure 3. Stability boundaries on the (R_e, v_{in}) parameter plane. In all the curves the superscript ^{k} reflects the value of the buck COT converter parameter k. The value of the circuit constant parameter are specified in Table I. The Γ_s and $v_{in_{lim}}^k$ curves were derived from (6) and (8), respectively. The ρ^k represent flip bifurcations of $\boldsymbol{\gamma}_1$. The χ^k curves were obtained by imposing the border collision bifurcation condition $\beta_1^1 \in \Sigma$ (see Fig. 2) having approximated the $\imath_L$ current at δ as $\frac{v_{ref}}{R_o} - \frac{\Delta \imath_{L_{\text{ON}}}}{2}$ (see Eq. (7)). The axes in the inset are both in linear scale.

restrictive and it becomes more and more restrictive the lower the ESR. To derive an approximate but less restrictive condition, we computed (5) for an estimated value of the $\imath_L$ inductor current at the beginning of the ON-phase, viz. we derived an estimate of the δ point. Unfortunately, this value cannot be exactly derived analytically but it can be safely approximated by writing it as the v_{ref}/R_o ideal output current (assuming C_o as an open-circuit) minus half the $\Delta \imath_{L_{\text{ON}}}$ steady-state ripple of the L_o inductor current. The latter is given by

$$\Delta \imath_{L_{\text{ON}}} = k \frac{v_{in} R_o - v_{ref}(R_o + R_p)}{f_{sw} L_o R_o v_{in}} v_{ref} \ , \tag{7}$$

approximating the charging of the inductor as linear w.r.t. time, assuming v_o fixed to v_{ref} during the overall periodic steady-state evolution of the COT converter, and neglecting the voltage drop across R_e. Since in general we must have $v_{in} > v_{ref}$ for step-down operation, and $R_p \ll R_o$, by using this approximate value for $\imath_L$, the inequality in (5) turns out to be satisfied if

$$v_{in} - \frac{k \Theta v_{ref}}{2 C_o f_{sw} L_o R_e} > 0 \ , \tag{8}$$

and on the (R_e, v_{in}) plane (see Fig. 3) this produces the $v_{in_{lim}}^k$ curves. Here and in the following the superscript ^{k} refers to the value of the k buck COT converter parameter[2].

The $v_{in_{lim}}^k$ curves are relevant only if the $\boldsymbol{\gamma}_1$ steady-state solutions are *not-minimal*, i.e., $\Delta t_{\text{OFF}} > \Delta t_{\text{OFF}}^{\min}$ ($\delta_1 \neq \beta_1$ in

[2]The well known stability boundary $C_o R_e - \Delta t_{\text{ON}}/2 > 0$ described in [8], [14] reduces to (8) if $R_p = 0$, and Δt_{ON} is chosen as in (2). Nevertheless, at the best of the authors knowledge, in the literature Δt_{ON} is left free and not necessarily adapted for constant-frequency operation emulation. Therefore, it should be used with care since it retains the dependency on C_o and R_e only.

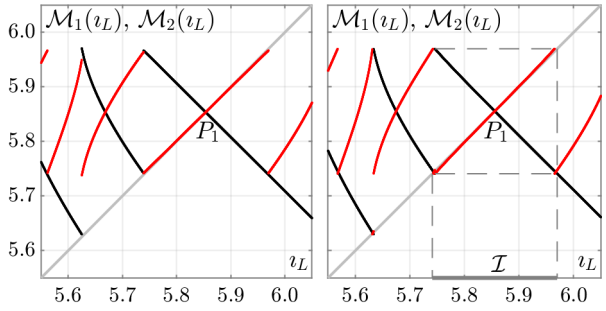

Figure 4. First- and second-return maps ($\mathcal{M}_1$ in black and $\mathcal{M}_2$ in red) obtained for $v_{in} = 23.21\,\mathrm{V}$ (left panel) and $v_{in} = 21.73\,\mathrm{V}$ (right panel) and $R_e = 0.3\,\mathrm{m\Omega}$. The equilibrium point P_1 in the left panel and in the right panel, respectively, corresponds to the stable and unstable $\boldsymbol{\gamma}_1^s$ limit cycle in Fig. 5. $\mathcal{I}$ is the absorbing interval that appears after the flip bifurcation.

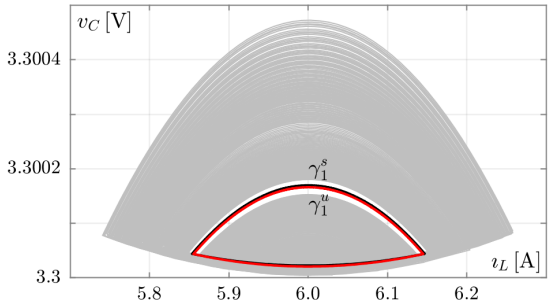

Figure 5. The $\boldsymbol{\gamma}_1^s$ (in black) and $\boldsymbol{\gamma}_1^u$ (in red) were derived for $v_{in} = 23.21\,\mathrm{V}$ and $v_{in} = 21.73\,\mathrm{V}$, respectively. The former is stable (with the second Floquet multiplier $\mu_2 = -0.99$) and the latter is unstable ($\mu_2 = -1.01$). The chaotic trajectory is obtained for $v_{in} = 21.73\,\mathrm{V}$.

Fig. 2). This is due to the fact that, if this occurs, in the COT buck converter the saturation of the controller is observed, viz. the regulation of the output voltage is lost. The appearance of a minimal $\boldsymbol{\gamma}_1$ limit cycle is due to a border collision bifurcation corresponding to the boundary induced by the $\beta \in \Sigma$ condition. It can be estimated through δ: the $\boldsymbol{f}^{(1,\xi)}$ vector field can be explicitly integrated for a $\Delta t_{\mathrm{ON}} + \Delta t_{\mathrm{OFF}}^{\mathrm{min}}$ time interval, by properly switching ξ, thus obtaining an estimate of β. On the (R_e, v_{in}) plane this yields the χ^k curves. The generic ρ^k curve intersects the corresponding χ^k curve in the codimension-2 π_k point (see Fig. 3). For parameter values below the χ^k-curves the system becomes unfeasible.

IV. Numerical Results and Discussion

The stability boundaries presented in Sec. III are verified against the results obtained through bifurcation analysis.

The estimated boundaries $v_{in_{lim}}^k$ shown in Fig. 3 turned out to be a good approximation of the corresponding bifurcation curves ρ^k, especially for $k \in 1, 2$. This can be noticed in the inset in Fig. 3. The discrepancies for low values of R_e and extremely high values of v_{in} are negligible since the latter are significantly larger than realistic operation limits of the COT buck converter even in wide input-voltage range applications.

The ρ^k curves represent flip bifurcations of γ_1 limit cycles. In a smooth system this would imply the presence, in the neighborhood of a given γ_1, of either a stable (supercritical bifurcation) or an unstable (subcritical bifurcation) γ_2 limit cycle [15]. Also in our piece-wise smooth system, a flip bifurcation occurs. A numerical analysis has been performed via the one-dimensional first- and second-return maps ($\mathcal{M}_1$ and $\mathcal{M}_2$, respectively) from Σ to Σ in the neighborhood of $\boldsymbol{\gamma}_1$ close to the bifurcation value, vertically crossing the ρ^1 curve from the ν_s to the ν_u point in Fig. 3. Fig. 4 (left panel) shows the shape of the map just before the bifurcation of γ_1, and P_1, the equilibrium point of $\mathcal{M}_1$, denotes the limit cycle, still attracting. Since the map $\mathcal{M}_2$ is convex (resp. concave) before (resp. after) the point P_1 the flip bifurcation is of supercritical type. Fig. 4 (right panel) shows the shape of the map after the bifurcation of γ_1, and the repelling equilibrium point P_1 now shows an unstable limit cycle. Moreover, one more unstable limit cycle exists, due to another (decreasing) branch of map $\mathcal{M}_1$, and an invariant absorbing interval $\mathcal{I}$ is clearly observable, denoting the existence of bounded dynamics. Since the slopes of the map $\mathcal{M}_1$ in $\mathcal{I}$ seem larger that one in modulus, the dynamics inside $\mathcal{I}$ is chaotic. Fig. 5 shows γ_1 before and after the bifurcation, and the chaotic attractor corresponding to the dynamics inside $\mathcal{I}$.

Table I
COT CONVERTER CIRCUIT PARAMETER VALUES

Name	Value	Name	Value	Name	Value
C_o	300 µF	R_e	$[0.1, 10]\,\mathrm{m\Omega}$	k	[1, 3]
L_o	12 µH	R_o	$0.55\,\Omega$	v_{ref}	3.3 V
R_p	$20\,\mathrm{m\Omega}$	UVLO	3.6 V	v_{in}	[UVLO, 75 V]
$\Delta t_{\mathrm{OFF}}^{\mathrm{min}}$	230 ns	f_{sw}	800 kHz		

As a major consequence of this mechanism, the pulse bursting phenomenon is characterised by electrical variables whose frequency spectrum is very rich. Of course this effect mainly involves $\imath_L$ since the inductor current ripple is much more significant than both the v_o and v_C ones.

The analysis reveals that the safe region for stable operation exhibits an additional dependency on the input voltage. In particular, the additional limitation coming from the input voltage starts to be relevant where the total ESR approaches values which are typically achieved when ordinary multilayer ceramic capacitors are connected in parallel. As an example, referring to Fig. 3, it should be noted that even the normal operating range of 12 V battery systems ($8 - 9\,\mathrm{V}$ to $16\,\mathrm{V}$) might fall below the $v_{in_{lim}}^k$ and ρ^k curves in a region which is potentially unstable for R_e values achieved by the parallel combination of a few (namely, three) 100 µF ceramic capacitors (capacitance vs. voltage bias effects having been neglected for simplicity). This would be a reasonable output capacitor combination for an automotive $12\,\mathrm{V}$ to $3.3\,\mathrm{V}$, $6\,\mathrm{A}$ buck converter exposed to load transients, but unfortunately Fig. 3 predicts that it cannot be safely used with COT control, at least without additional "helping" circuits such as ripple injection. Alternatively, if output voltage ripple specifications and other design/cost constraints permit, other capacitor types providing higher R_e (such as polymer) can be used.

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