Fully-printed, all-polymer, bendable and highly transparent complementary logic circuits

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In this contribution we show a simple approach for the development of all-polymer based complementary logic circuits fabricated by printing on plastic, at low temperature and in ambient conditions. This is achieved by patterning, with a bottom-up approach, solely syn-thetic carbon-based materials, thus incorporating earth-abundant elements and enabling in perspective the recycling – a critical aspect for low-cost, disposable electronics. Though very simple, the approach leads to logic stages with a delay down to 30 μs, the shortest reported to date for all-polymer circuits, where each single component has been printed. Moreover, our circuits combine bendability and high transparency, favoring the adoption in several innovative applications for portable and wearable large-area electronics.

Keywords:
Printed electronics
Transparent electronics
Flexible electronics
Organic electronics
Organic field-effect transistor

1. Introduction

The field of flexible microelectronics, where bendable and even conformable substrates are adopted, has the appealing potentiality of facilitating the integration of electronic functionalities into innovative light-weight products. To this purpose, organic materials represent one of the most suitable candidates because of clear advantages such as their good mechanical flexibility and the chemical tunability of the opto-electronic properties, achieved by exploiting a vast library of molecules and functional groups. Furthermore, their solubility in organic solvents enables the use of printing and coating techniques, highly desirable in the context of large area and low-cost technologies [1,2]. Printing enables device mass-production requiring low capital investments, as well as highly customized applications at sustainable costs thanks to digital techniques, such as inkjet printing [3]. Polymer-based opto-electronic devices on plastic substrates, such as flexible displays [4], large-area chemical and physical sensors [5,6], and photodetectors [7,8] have been widely explored. Polymer logic gates and circuits are necessary to obtain fully-integrated systems, as they provide essential data computation and matrix addressing functionalities [9]. Recent progress in this area has led to field-effect transistors with impressive mobilities, greater than 1 and 10 $cm^2/V\ s$ for *n*- and *p*-type donor–acceptor co-polymers, respectively [10]. Thus, high performance electronic elements are at hand, since hole/electron mobilities are now a far less limiting aspect than it was only a few years ago. However, major efforts are necessary to move the field from a single high-performance transistor to more

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complex circuits, essential for commercial applications [11]. Yet, most of transistor integration studies combine hybrid approaches, where besides the organic semiconductor, either the dielectric, the electrical contacts, and the substrate are fabricated by vapor deposition, or are mechanically rigid. These limitations, combined with the use of non-scalable techniques, undermine the whole printed electronics concept [12]. Transparency, or semi-transparency, is also a highly demanded feature for flexible electronics as it would allow delivering active electronic circuits on top of labels or graphic illustrations. Furthermore, polymer electronics is one of the best candidates for cheap, short life-time cycle, disposable mass products. Therefore a reasonable question about the environmental impact of the supply of raw materials and of the dispersion of large quantity of plastic arises, imposing to develop earth-abundant and recyclable materials [13].

Reports combining all the requirements highlighted above are very rare in the literature, and usually comprise discrete, often very low performance, devices, which operate at frequencies well below the kHz regime. Here we address the challenge of fabricating robust, complementary logic circuits by adopting only scalable techniques in ambient conditions and at low temperatures (maximum processing temperature $\sim$ 120 °C). These devices are based on well known model polymers such as poly([N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene) (P(NDI2OD-T2)), as the electron-transporting polymer and diketopyrrolopyrrole-thieno[3,2-b]thiophene copolymer (DPPT-TT) as the hole semiconductor. In the light of realizing fully carbon-based and highly transparent circuits, we used highly conductive formulations of poly(3,4-ethylenedioxythiophene): polystyrene sulfonate (PEDOT:PSS) for the electrodes. While efficient hole injection is expected through PEDOT:PSS, thanks to a suitable nominal matching of the highest occu-pied molecular orbitals (HOMO) of most high-performance semiconducting polymers, its use for complementary circuits is less obvious because of a nominally less favorable matching with the lowest occupied molecular orbitals (LUMO), which usually requires low work function electrodes. We show that optimal device performances are achievable in both cases for channels down to a few tens of micrometers, thanks to a surprisingly low contact resistance of 33 kΩ cm in the case of *n*-type devices. Such value is achieved without the need of an additional charge injection layer [14,15], thanks to interfacial effects reducing the nominal barrier for electron injection.

Regarding the deposition techniques of the functional materials, we employed ink-jet printing, which is a non-contact digital technique requiring minimum amount of inks [3] to pattern the electrodes and the semiconductors. Since inkjet printing is less suitable for fast uniform coat-ings, required e.g. for the dielectric and passivating layers, we have adopted bar-coating [16], a rugged coating tech-nique which enables the fine control of film thickness over large areas.

Our approach is very simple, and it is compatible with the fabrication of complementary inverters and ring-oscillators and more complex circuits such as logic latches, i.e. dynamic storage elements. Thanks to the good mobility of the selected semiconductors and the optimal characteristics of the resulting devices, logic gates show stage delays down to 30 μs, by far the shortest reported to date for truly all-printed, all-organic circuits on plastic substrates. Moreover, these circuits are highly transparent (>90% not consid-ering the substrate) and flexible (no mobility degradation up to 1% of tensile strain). Thus, these results form a solid base for the further development of transparent, all-poly-mer circuits enabling complex logic functionalities to be integrated in future cost-effective, wearable, portable and ubiquitously integrated electronic devices.

2. Materials and methods

2.1. Materials

P(NDI2OD-T2) was purchased from Polyera and DPPT-TT was synthesized using the method explained by Chen et al. [17]. Poly(methyl methacrylate) (PMMA) was purchased from Sigma Aldrich (average $M_w \sim 120{,}000$). PEDOT:PSS formulations Clevios Pjet700 and Clevios PjetN were purchased from Heraeus, while Orgacon ICP1050 was purchased from Sigma Aldrich. The 125 μm thick poly (ethylene 2,6-naphthalate) (PEN) substrate was purchased from DuPont.

2.2. Device fabrication

We inkjet printed all the PEDOT:PSS formulations for conductivity characterization and source/drain/gate patterning by means of a Fujifilm Dimatix DMP2831. After printing, the PEDOT:PSS features were baked at 110 °C for 30 min. Both semiconductors were deposited by inkjet printing and subsequently baked: P(NDI2OD-T2) was dissolved in mesitylene with a concentration of 5 mg/ml and baked at 120 ° C for 12 h; DPPT-TT was dissolved into mesitylene at a concentration of 5 mg/ml and baked at 120 ° C for 12 h. PMMA was dissolved in anhydrous n-butyl acetate with a concentration of 80 mg/ml. Dielectric coating of the devices was performed through a custom bar-coater with a 50 mm/s speed and a bar with a 12 μm wire diameter. After deposition, PMMA film was annealed at 80 ° C for 30 min. Finally, PEDOT:PSS (Pjet700) was inkjet printed to make the gate electrode and annealed at 110 °C for 30 min to remove the excess solvent. For cir-cuits, via-holes interconnections were realized through chemical drilling by inkjet printing the solvent directly onto the PMMA surface and filling the holes with PEDOT:PSS.

2.3. Measurements

The work function of the three PEDOT:PSS formulations (Pjet700, PjetN and ICP1050), as well as the electronic structure at the interface with the *n*- and *p*-type semiconductors were evaluated by means of ultraviolet photoemission spectroscopy (UPS). More details on the preparation of the samples and on the experimental setup for the photoemission measurements are included in the Supplementary Information. The transparency of all-printed devices was

measured by UV–Vis absorption spectroscopy. The characterization of discrete transistors and circuits was performed in an inert nitrogen atmosphere. Measurements of the transistors characteristic curves and of the inverters voltage transfer curve (VTC) were performed by means of an Agilent B1500A Semiconductor Parameter Analyzer. The noise margin calculation was performed according to the maximum equal criterion (MEC). Bending measurements were performed by bending the substrates on multiple bars with decreasing radii. The dynamic response of circuits was measured using a Tektronix P5122 high impedance probe with low parasitic capacitance connected to a Tektronix DPO2014 Oscilloscope. This configuration ensures a load capacitance of ≈4.6 pF; moreover, the use of such probe eliminates the need for output buffers in the circuit layout. The input signals and the voltage supply were applied to the circuits by an FLC Electronics Multichannel WFG600 High-Voltage Waveform Generator. The frequency response of the FETs was measured with a custom setup based on Agilent Technologies E5061B Network Analyzer.

3. Results and discussion

To fabricate fully printed field-effect transistors (FETs) on plastic we selected a top-gate, bottom-contact architec-ture, which allows for optimal charge injection [18] and controlled semiconductor–dielectric interfaces [19]. A schematic view of the FET cross-section is shown in Fig. 1a. Device fabrication involves exclusively additive pro-cesses which are fast, cost-effective and compatible either with sheet-to-sheet or roll-to-roll processing: (i) on top of a 125 μm thick PEN substrate, source and drain contacts were patterned by inkjet printing PEDOT:PSS (Fig. 1b), allowing to fabricate devices with channel lengths (L) down to 40 μm and channel widths (W) of ~1200 μm; (ii) the semiconductor patterning was performed by inkjet printing, resulting in a 40–50 nm thick layer (Fig. 1c); (iii) the polymer PMMA dielectric was then deposited by bar-coating on the whole device area with an average thickness of 700 nm; (iv) the device is completed by ink-jet printing a PEDOT:PSS gate electrode on the dielectric (Fig. 1d).

As a first step, we assessed the feasibility of n-channel FETs with a reduced voltage drop at the contacts, which is mainly determined by the electrode resistivity as well as the energy barrier to electrons injection into the semiconductor. A low contact resistance is a fundamental prerequisite for FET integration in fast, downscaled complementary logic circuits, which is not obviously reached with PEDOT:PSS electrodes, typically characterized by relatively low conductivity (compared to metals) and high work func-tion (W_f), nominally producing electron injection barriers. For this purpose we have explored various PEDOT:PSS formulations for source and drain contacts patterning, namely Clevios Pjet700, Clevios PjetN and Orgacon ICP1050, distinct for acidity and wettability of the PEN surface (i.e. ease of processability) and, more importantly, providing a wide range of film conductivities (from 0.5 S/cm to 180 S/cm). Contact angles on PET, pH and conductivity data are report-ed in Table 1. We have determined the work function of the printed conductors by UPS measurements, verifying that the acidic formulations (Pjet700 and ICP1050) produce electrodes with a higher W_f (5.1 eV and 5.0 eV, respectively) with respect to the neutral formulation (PjetN, 4.4 eV). Such dependence of the W_f on the pH is consistent with what pre-viously observed in literature [20]. The different W_f values for the three electrodes therefore size different nominal electron-injection barriers, defined as the nominal differ-ence between the electrodes work function and the semiconductor LUMO level. Quite interestingly, all P(NDI2OD-T2) FETs showed good n-channel behavior with

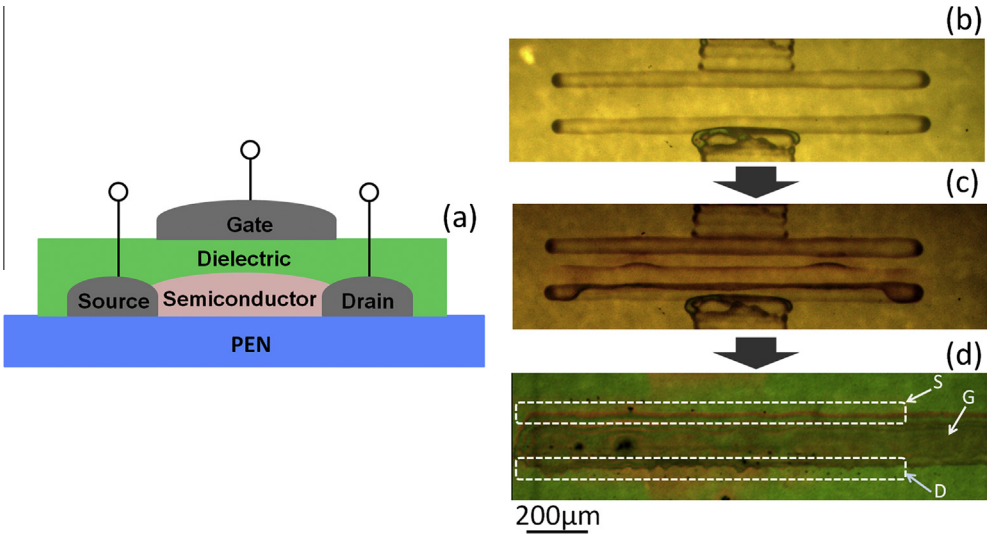

Fig. 1. (a) Schematic of all-printed, all-organic FETs. In the process flow, (b) source and drain electrodes are inkjet printed on the substrate, then (c) the semiconductor is inkjet printed on the electrodes. After the deposition of the dielectric by bar-coating, (d) the device is completed by inkjet printing the top gate electrode.

Table 1
Parameters of the different PEDOT:PSS formulations adopted in this work and electron mobilities of P(NDI2OD-T2) FETs with contacts printed with such formulations.

Formulation	pH	Contact angle on PEN (°)	Conductivity (S/cm)	Work function (eV)	Average linear mobility (cm^2/V s)	Average saturation mobility (cm^2/V s)	Maximum saturation mobility (cm^2/V s)
Clevios Pjet700	1–2	<20	180	5.1	0.15 ± 0.01	0.31 ± 0.06	0.4
Clevios PjetN	5–8	<20	5	4.4	0.12 ± 0.01	0.23 ± 0.03	0.25
Orgacon ICP1050	⩽2.5	65–70	0.5–1	5.0	0.05 ± 0.01	0.13 ± 0.04	0.18

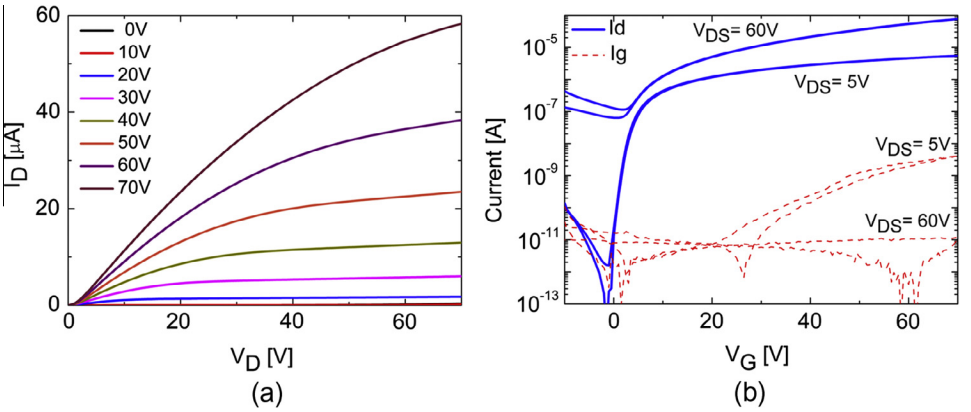

Fig. 2. *n*-type printed P(NDI2OD-T2) FET characteristics. Output curves (a) and transfer curves (b), based on printed Pjet700 electrodes with W = 1200 μm and L = 50 μm.

high electron field effect mobility values (μ_{el}), with a maximum value in saturation regime of 0.4 cm^2/V s (see transfer characteristic and output curves in Fig. 2 and mobility data in Table 1). These effective mobility values, i.e. extracted without taking into account the possible effect of the contact resistance, are comparable with state of the art ones obtained on optimized devices with the semiconductor spin-coated on glass and with metal electrodes and PMMA as gate dielectric [21]. Just slightly inferior mobilities were observed for Orgacon ICP1050, which actually displays the lowest conductivity of 0.5 S/cm among the three formula-tions. A rough estimation of the maximum voltage drop within the ICP1050 electrodes in a working FET suggests that a strong channel depolarization may occur due to ICP1050 high resistivity, probably reducing device perfor-mances (see the Supplementary Information for the detailed discussion, Fig. S1 and Table S1).

Transfer curves for the P(NDI2OD-T2) FETs employing the PJet700 formulation of PEDOT:PSS are showing proper field-effect behavior both in linear and saturation regimes (Fig. 2b). The presence of a parasitic *p*-type channel for high drain-source voltages must however be noted; this implies the non complete turn-off of the transistor at high V_{DS} values. This stray current (V_{GS} = 0 V; V_{DS} = 60 V) is more than two orders of magnitude lower than the full saturation current (V_{GS} = 60 V; V_{DS} = 60 V) and would have a limited effect on e.g. an inverter transfer curve. A similar behavior, but with an even less marked effect, will be found for DPPT-TT OFETs (Fig. 4b). Such non ideality requires in any case attention since it would have a relevant impact on large scale integrated circuits, also increasing the overall static power dissipation. For large scale of integration, the ambipolarity of the devices should be further reduced with proper engineering of the injection barriers.

We have employed the differential method [22] to extract the contact resistance (R_C) of the different electrodes (Fig. 3a). A detailed description of the extraction parameters are reported in the Supplementary Information (Fig. S5). We found that R_C scales with PEDOT:PSS conduc-tivity, clearly representing the main source of contact resistance for our P(NDI2OD-T2) FETs. More importantly, when Pjet700 is employed an impressively low R_C value of 33 kΩ cm at V_G = 60 V (L = 50 μm) is extracted. Atomic Force Microscopy (AFM) of P(NDI2OD-T2) film topography reveals that a typical fibrillar structure, induced by the presence of pre-aggregates in mesitylene solutions [21], is present both inside the channel and on top of PEDOT:PSS contact regions (Fig. S7). Importantly, a good structural continuity of the fibrillar texture across the contact edge toward the channel was found (Fig. 3b); such a defect-free morphological uniformity likely represents a key factor for the low R_C observed, since it excludes the presence of semi-conductor low-mobility regions in the electrodes proximity [23,24]. Additionally, the R_C value is comparable to the one extracted for P(NDI2OD-T2) on Au electrodes (22 kΩ cm at V_G = 60 V, L = 21.5 μm) [25], indicating a relatively small electron barrier at the PEDOT:PSS/semiconductor interface despite the high electrode W_f (5.1 eV).

The results above demonstrate that an efficient electron injection with reduced R_C can be achieved also with semi-transparent conducting polymer formulations. Next, we tested the same PEDOT:PSS formulation for hole injection in DPPT-TT-based *p*-type printed transistors (Fig. 4). As expected when high W_f electrodes are used with *p*-channel

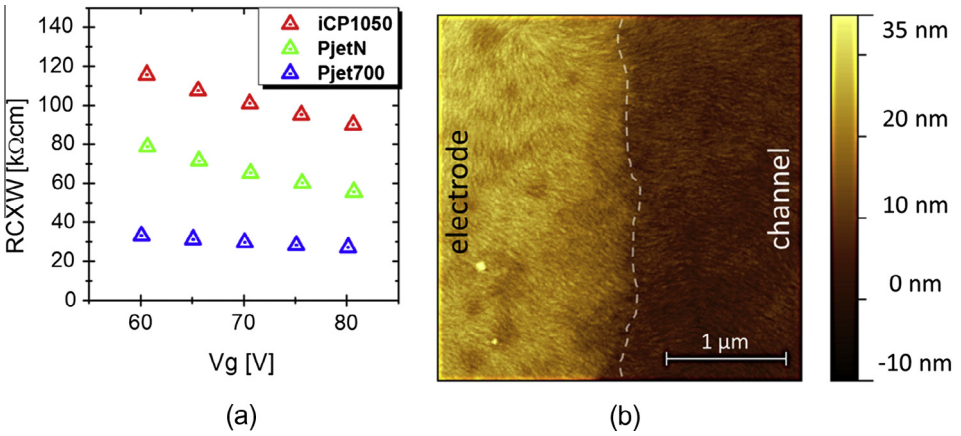

Fig. 3. (a) Normalized contact resistance ($R_C \times W$) at $V_D = 5$ V as a function of gate voltage ($L = 50$ µm). (b) AFM image of P(NDI2OD-T2) at the electrode-channel edge, where the coverage of the semiconductor is uniform from the electrode to channel.

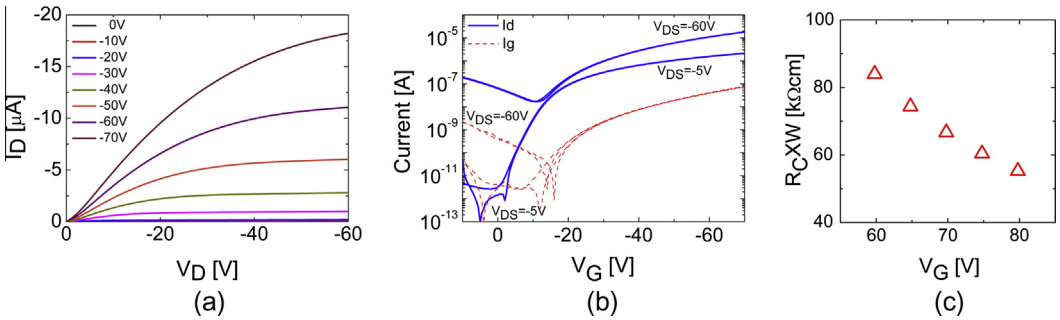

Fig. 4. (a) Output and (b) transfer characteristics of DPPT-TT based *p*-type FETs. Source, drain and gate electrodes were fabricated using the Pjet700 formulation. FET parameters were $L = 50$ µm and $W = 1150$ µm. (c) Normalized contact resistance ($R_C \times W$) at $V_D = 5$ V as a function of the gate voltage obtained with the differential method ($L = 50$ µm).

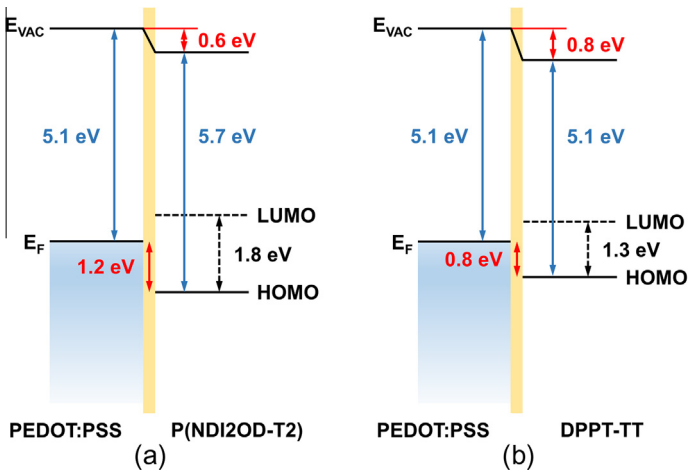

Fig. 5. Energy level alignment at the (a) P(NDI2OD-T2)/PEDOT:PSS and (b) DPPT-TT/PEDOT:PSS interfaces, in the case of the most conductive PEDOT:PSS formulation adopted in this work, PJet700.

semiconductors, good device characteristics were achieved, with a mean saturation field effect mobility of 0.19 $cm^2/V\,s$ (maximum $\mu_{hole} = 0.22$ $cm^2/V\,s$) and a mean threshold voltage of −14.4 V. However the S-shaped output curve of Fig. 4a suggests that, although a good alignment between PEDOT:PSS Fermi energy level and DPPT-TT HOMO level is expected, *p*-type FETs are affected by more substantial contact resistance. An $R_C = 82$ kΩ cm was extracted at

V_G = 60 V and L = 50 μm, exceeding the one extracted for P(NDI2OD-T2).

To gather insights into the actual energy barriers for electron and hole injection from PEDOT:PSS into P(NDI2OD-T2) and DPPT-TT, respectively, we have performed a detailed study of the energy level alignment at the PEDOT:PSS/semiconductor interfaces by performing UPS measurements in the case of the PJet700 formulation. Fig. 5a and b shows the results for the P(NDI2OD-T2)/PEDOT:PSS and DPPT-TT/PEDOT:PSS interface.

The sample work function and the HOMO level position have been directly inferred from the UPS spectra. In the P(NDI2OD-T2) case, the position of the LUMO level was obtained by assuming an energy gap of 1.8 eV, taken from the literature [26]. In the DPPT-TT case, a lower limit for the LUMO position was estimated from optical data (a value of 1.3 eV is reported for the DPPT-TT optical band gap) [17]. We retrieve a value of 5.7 eV and 5.1 eV for the P(NDI2OD-T2) and DPPT-TT ionization energies, respectively, in good agreement with the literature [17,27]. Importantly, for both polymers, a sharp decrease in the work function within the first polymer layer is observed (see the Supplementary Information for further details, Fig. S9), likely due to the formation of a dipolar layer at the interface, favouring electron injection in the P(NDI2OD-T2) case and increasing the hole barrier in the DPPT-TT case. From the data of Fig. 5, we determine an electron (hole) injection barrier of about 0.6 (0.8) eV into the *n*-(*p*-)type polymer, corroborating the low R_C values extracted from the electrical characterization and in agreement with our observation of a smaller R_C for the PEDOT:PSS/P(NDI2OD-T2) FETs with respect to the PEDOT:PSS/DPPT-TT ones. The present UPS results show also some interesting differences with respect to a previous study of the P(NDI2OD-T2)/PEDOT:PSS interface, where a larger injection barrier for electrons (>1 eV) was measured [27]. Similar to our findings, a strong interaction between the substrate and the first polymer layer was there observed. This comparison suggests that either (i) differences in the electronic characteristics of the PEDOT:PSS layer or (ii) morphological aspects (such as phase segregation at the PEDOT:PSS surface, or a different packing of the semiconducting polymer chains) may play a relevant role in the energy level alignment at the P(NDI2OD-T2)/PEDOT:PSS interface.

The results obtained so far underline that it is indeed possible to fabricate *n*- and *p*-type transistors with the same electrodes/substrate, scalable deposition techniques, and identical processing conditions. With such powerful combination, the most obvious step is the realization of complementary logic circuits, which need both *n*- and *p*-type transistors in the same circuit. Compared to unipolar logic, complementary logic benefits from faster switching speed, good immunity to signal variations, and reduced power dissipation.

The simplest complementary circuit which can be realized is the logic inverter. We have fabricated it with the same process flow described above, by integrating one *n*- and one *p*-type transistor. As Fig. 6a shows, the inverter structure is fabricated by driving the two transistors with the same gate electrode for providing the input signal and by making them share the drain contact that is, also, the output node of this logic gate. Fig. 6b shows the optical

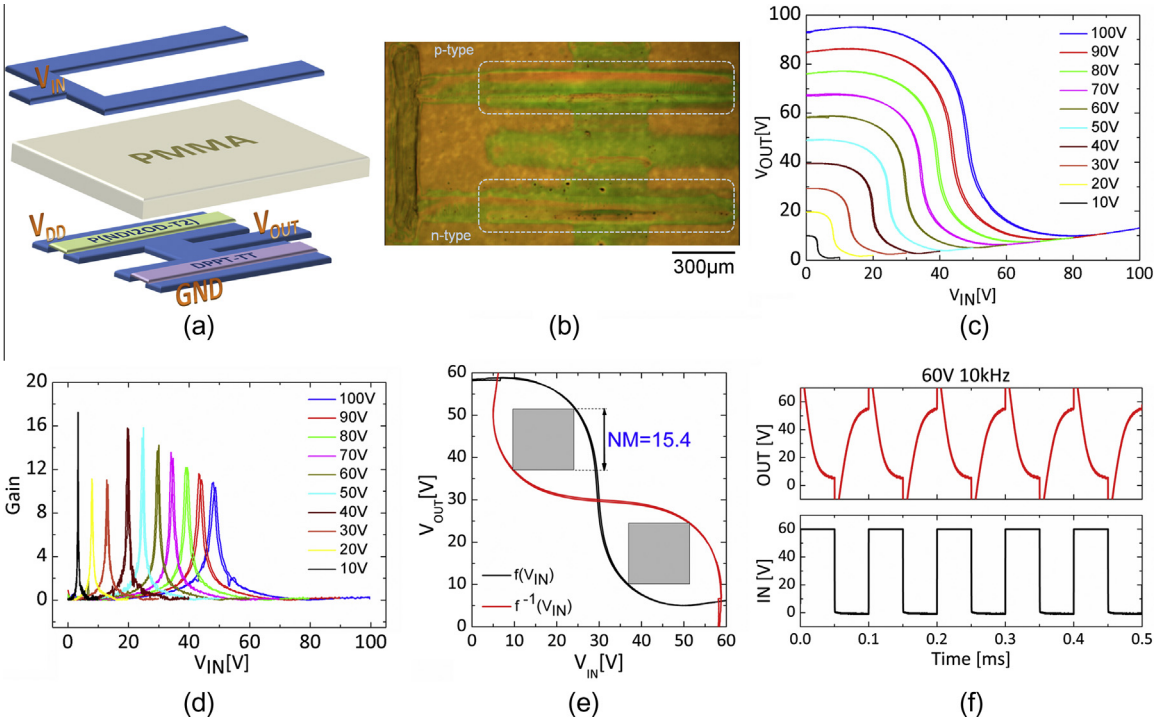

Fig. 6. (a) Schematic representation of our printed all-polymer inverter, (b) optical micrograph of real inverter, (c) inverter voltage transfer curves, (d) gains of the inverter, (e) noise margin calculation and (f) dynamic response of an inverter.

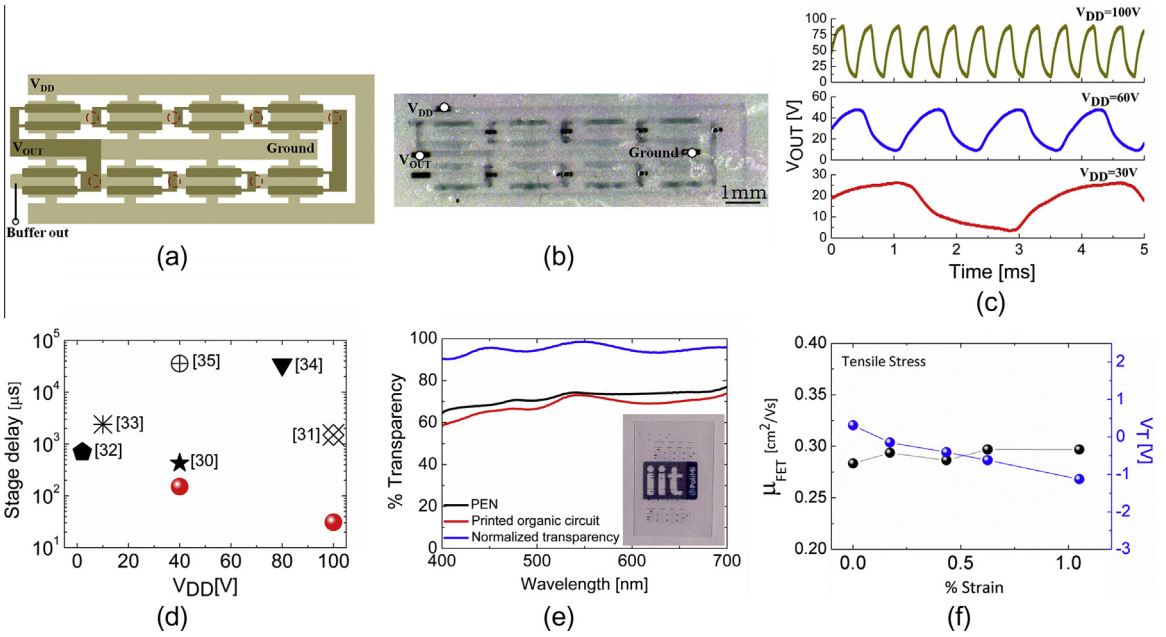

Fig. 7. (a) Schematic representation of a 7-stage RO, (b) optical micrograph of 7-stage RO, (c) frequency response of RO, (d) survey of the best stage delay values for truly all-printed, all-polymer RO (red circles represent this work), (e) transparency of the RO with respect to the PEN substrate and (f) field effect mobility and threshold voltage variations vs. strain (%). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

micrograph of the final printed device. A full static and dynamic characterization of the device was performed in order to understand the suitability of our approach for a robust complementary technology.

The static characterization was done by sweeping the input signal from a "0" logic value to a "1" at supply voltages ranging from 10 V to 100 V. The voltage transfer curves (VTC) obtained from these measurements (Fig. 6c) enable us to extract all the figures of merit to evaluate the robustness of the manufactured complementary logic, like rail-to-rail behavior, inverting threshold voltage, gain and noise margin [28]. The design of an inverter generally aims at balancing *n*- and *p*-type conduction so that the inverting threshold voltage results one half of the supply voltage ($V_{DD}/2$). Since our P(NDI2OD-T2) and DPPT-TT FETs exhibit balanced electron and hole mobility, respectively, for the same processing conditions, we could design an inverter with minimized area occupation by making equal channel widths and lengths for both FET types. The extrac-tion of the inverting threshold voltage is accomplished by intersecting the VTC at a given supply voltage with the $V_{OUT} = V_{IN}$ curve, resulting in very balanced VTCs with a global variation of 6.21% ± 8.24% of $V_{DD}/2$ that reduces to 1.16% ± 0.53% of $V_{DD}/2$, if only supplies from 40 V to 80 V are considered. The best performance is obtained at V_{DD} = 60 V with a perfectly balanced voltage threshold of 30 V. The VTCs denote a not complete rail-to-rail behavior that can be attributed to the slight ambipolar behavior of both P(NDI2OD-T2) and DPPT-TT transistors in the satura-tion region (Figs. 2b and 4b). Gain values, which corre-sponds to the derivative of the VTCs at the inverting threshold (Fig. 6d), results in a maximum gain of 17,

demonstrating the suitability of this approach to manufacture complementary logic circuits. We also tested the conformity of the measured gain values with its theoretical value obtainable from the Eq. (1):

$$\text{Gain} = \frac{v_{out}}{v_{in}} = (g_{mp} + g_{mn})\left(\frac{r_{out,p} r_{out,n}}{r_{out,p} + r_{out,n}}\right) \quad (1)$$

where g_{mp} and g_{mn} are the transconductance of the *p*- and *n*-type FETs respectively, calculated from the single devices transfer curves at the inverting threshold bias point. The output resistances $r_{out,p}$ and $r_{out,n}$ are calculated from the output transfer curves at the same bias point mentioned above [28]. The experimental value of 14.1 at a supply voltage of 60 V fits well the theoretical one of 14.9. Details of this calculation are provided in the Supplementary Information.

The complementary inverter has a maximum dynamic power consumption of 960 µW, when biased at V_{DD} = 60 V; static power dissipation is limited to few microwatts, mainly owing to the ambipolar behavior of the OFETs.

As the last figure of merit we have calculated the noise margin (NM), which gives an estimation of the immunity to the input signal variations. Using the maximum equal criterion [29], the NM results to be 15.4 V (Fig. 6e) that is equal to 50% of $V_{DD}/2$, well above the minimum required noise margin value for the correct operation of complementary logic circuits. In addition to the static characterization, we also carried out dynamic measurements (Fig. 6f): a square wave signal was fed to the inverter's gate electrode and the output waveform was sampled, demonstrating a correct inverting behavior up to 10 kHz at a supply voltage of 60 V. Measured waveforms at different frequencies can be found

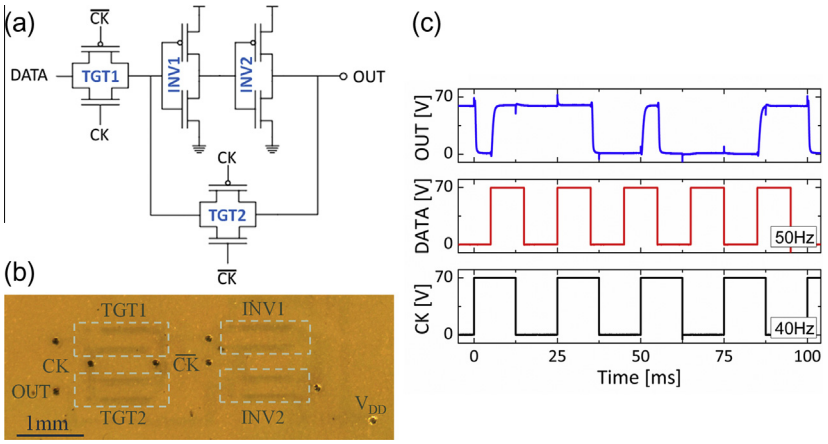

Fig. 8. (a) Schematic representation of our D-Latch circuit based on the pass-transistor logic, (b) optical micrograph of D-Latch circuit and (c) operation of our fully-printed, all-polymer and transparent D-Latch circuit.

in the Supplementary Information (Fig. S13). This result is crucial for the expected frequency behavior of the circuits we are going to discuss in the next section.

To further test the suitability of the fabricated inverters to be integrated in logic circuits, we have fabricated ring-oscillators (ROs). A ring oscillator is a self-oscillating circuit composed by an odd chain of inverters which produces an oscillation at a frequency (f_{RO}) which depends on the total number of stages and on the delay introduced by each stage (Stage Delay – SD), according to Eq. (2):

$$f_{RO} = \frac{1}{2 \cdot N \cdot SD} \tag{2}$$

where N and SD are the number of stages and the stage delay, respectively. The layout of the 7-stages ring-oscillator is displayed in Fig. 7a. A supplementary fabrication step, based on a jetted solvent for via-holes creation, was introduced after the dielectric deposition to allow interlayer connections. The resulting circuit is shown in Fig. 7b. Dynamic measurements were performed to study the oscillating behavior of the device and results are reported in Fig. 7c, showing an oscillation of a few hundred Hz for an applied voltage of 30 V and in excess of 2 kHz at 100 V. These values translate in a stage delay of 246 μs and 31 μs at V_{DD} = 30 V and 100 V (Fig. S15), respectively. To assess our results with respect to all-printed ROs reported in the literature [30–35], Fig. 7d compares the stage delay vs. V_{DD} for several studies, indicating that the present work achieves the shortest stage delays reported so far for all-printed, all-organic circuits.

Moreover, our circuits achieve such performances combining, at the same time, two appealing features for wearable electronics: transparency and bendability. To quantify transparency, we have measured the circuit transmittance by UV–Vis spectroscopy (Fig. 7e), where a transmittance higher than 60% on the whole visible range was measured. This value is actually limited by the 125 μm thick PEN substrate, where the printed layer contribution is minimal, displaying a transmittance of at least 90% on the same spectral range.

Along with transparency these devices are very flexible, despite the use of a rather thick PET substrate, as assessed by bending tests [36,37]. Thus, by applying a tensile stress >1% perpendicular to the FET array channel (bending radii down to 6 mm) a minimal variation of the electron mobility is measured (Fig. 7f), denoting the robustness of the all-polymeric approach. Moreover, negligible variations of the devices transfer curves is observed (Fig. S16), apart from a really modest shift of the sub-threshold region.

Finally, we demonstrate that our approach, which shows good complementary logic performance with good noise margins and viable gains, is suitable for the development of an all-printed complex logic circuitry by fabricating D-Latches circuits based on the pass-transistor logic (Fig. 8a and b) [38]. Among all the possible circuit design architectures, we chose the complementary pass-transistor logic as the optimal trade-off between circuit complexity and number of transistors per logic function. Such circuit was, for our knowledge, never developed so far in a fully-printed and complementary transistor approach. The basic building blocks for this architecture are the inverters, previously discussed, and the transmission gate. The latter is an active switch composed of two complementary transistors sharing the source and the drain contacts and driven by opposite gate signals (respectively CK for n-type and $\overline{CK}$ for p-type). The D-Latch (Fig. 8a) is a quasi-static memory element storing one bit of information and is a basic unit for important functional building blocks such as shift-registers, required for example in addressing electronic arrays such as display backplanes. It is composed by two inverters (respectively INV1 and INV2) and two transmission gates (respectively TGT1 and TGT2), the latter working with opposite phases, so that while TGT1 acts as an open circuit, TGT2 acts as a short circuit and vice-versa. The operation of the logic block can thus be subdivided in two main phases, highlighted in Fig. 8a. During the transparency phase, when the CK value is high ($\overline{CK}$ low), the input data passes through TGT1 and is inverted twice by INV1 and INV2, so that the output is a delayed replica of the input. At the clock transition (CK low, $\overline{CK}$ high), the data value is stored inside the forward feedback loop

formed by INV1, INV2 and TGT2, thus defining a memory behavior. Our measurements in Fig. 8c show the proper operation of our fully-printed, all-polymer and transparent D-Latch. Thus, during the transparency phase the output follows the input signal, while during memory phase data is properly stored and it is not affected by the input switching, apart from the expected, small capacitive coupling spikes that do not disturb at all the circuit performance.

4. Conclusions

We have demonstrated a simple and effective approach for the fabrication of bendable and highly transparent electronic circuits completely relying on carbon based materials, i.e. a highly conducting polymer as electrical contact, a polymer dielectric, and *p*-/*n*-type polymer semiconductors, which are all processed with scalable printing techniques at low temperatures on plastic substrates (PEN). In particular, we have combined a patterning (inkjet) and a coating (bar-coating) technique for the fabrication of complementary transistors based on good mobility co-polymers, namely P(NDI2OD-T2) and DPPT-TT, achieving saturation mobility of 0.4 $cm^2/V\,s$ and 0.22 $cm^2/V\,s$, respectively. A key aspect in obtaining such a well-balanced complementary transistor characteristics is the achievement of high performing *n*-type FETs despite the use of high work function conducting polymers. This result can be rationalized by considering the very low resistance of the conductor, the continuity of the semiconducting polymeric film microstructure across the electrode/channel edge and the low energy barrier for electron injection. All these effects combine to reduce the contact resistance for electrons to 33 $k\Omega\,cm$ for P(NDI2OD-T2) based FETs, a value which is even lower than the one measured in the *p*-type DPPT-TT devices.

These favorable features have enabled the development of complementary logic, where various ideal building blocks such as inverters and pass-transistors could be integrated into ring-oscillators and D-Latches. The minimum stage delay of 30 μs measured for the oscillators corresponds to the shortest one reported so far for truly all-printed polymer circuits on plastic, with the additional features of a 90% transparency and bendability up to 1% tensile strain.

While for real applications a downscaling of the dielectric thickness to reduce the operating voltages is required, this work combines in a single approach elements that are essential for the deployment of high-performance wearable and lightweight electronics such as electrophoretic flexible displays, distributed sensors, bio-medical and security devices. Since for many of these applications there is a request for low-cost production and disposable devices, meeting the requirements of such electronics with all-carbon based materials will favor the development of an environmentally friendly technology.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2015.02.006.

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