Symmetrical-Component Approach for Circuit Modeling of EMI Emissions in Three-Phase Inverters

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***Abstract*—This paper provides the circuit model of a three-phase inverter as a four-port network. Such model is used to derive equivalent circuits for differential and common mode noise emissions when parasitic capacitances are taken into account. Moreover, a rigorous methodology based on the symmetrical component transformation is proposed to investigate the interaction between the three-phase side and the single-phase side. This allows a proper understanding of interaction between differential and common mode noise. Furthermore, the relationship between the DC side differential mode noise and the three-phase load is made clear. A more complete and rigorous circuit representation is obtained with respect to the conventional behavioral modeling available in the relevant literature.**

Keywords—conducted emissions, electromagnetic interference, noise source, circuit modeling, three-phase inverters

I. Introduction

Nowadays the use of three-phase inverters is widespread in a huge number of power applications. One of the main issues related to power quality and electromagnetic compatibility of electrical systems based on three-phase inverters is the conducted emission (CE) usually described in terms of differential mode (DM) and common mode (CM) noise. The relevant technical literature is very rich about both modeling and mitigation of CE noise [1]-[6].

As far as modeling is concerned, the most common approach is a frequency-domain behavioral approach [7]. The DC side of inverters is treated as a black box, and proper measurements are performed in order to provide Thevenin/Norton equivalents. Such approach, however, does not allow to understand the mechanism of noise generation and the interaction between differential and common mode noise. Moreover, the impact of three-phase load on noise level cannot be clearly explained.

In recent papers some attempts have been done to provide a more rigorous and complete circuit representation of the inverter as a noise source. In particular, in [8] a three-phase inverter is correctly represented as a four-port element, but the circuit representation of such element was not appropriate. Nevertheless, such approach pointed out that the differential mode noise at the DC side is strongly dependent on the three-phase load. This confirms that a proper modeling requires to treat the inverter as a four-port element. This point was not properly investigated in the previous literature.

In this paper a rigorous circuit representation of a three-phase inverter as a four-port network is derived. Then, a general methodology is presented in order analyze the conducted emission once the three-phase inverter is connected to a voltage source and a load. The proposed methodology is based on the well-known Symmetrical Component Transformation (SCT). Indeed, in a previous work it was shown that the SCT can be properly used to analyze circuits consisting in the interconnections of three-phase and single-phase circuits [9]-[10]. This is exactly the case under analysis, since the three-phase AC side of the inverter is connected to its single-phase DC side. Thus, a rigorous circuit description between differential and common mode noise is obtained. In particular, it is made clear the analytical relationship between the three-phase load and the differential mode noise on the DC side. The theoretical results derived in the paper are validated by means of Simulink/Matlab simulation of a three-phase inverter including the main parasitic capacitances related to the noise paths.

II. Equivalent Circuit for Ideal Three-Phase Inverters

Let us consider the ideal three-phase inverter represented in Fig. 1. By assuming the bottom terminal as reference, the circuit can be modeled as a four-port network. Therefore, the hybrid mathematical formulation of the network consists in four voltage/current relationships:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \\ i_p \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & h_a \\ 0 & 0 & 0 & h_b \\ 0 & 0 & 0 & h_c \\ h_a & h_b & h_c & 0 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ v_p \end{bmatrix} \quad (1)$$

where h_m $(m = a, b, c)$ are the three switching functions of the three legs *a,b,c*, i.e., $h_m = 1$ when the upper switch of leg m is on and the lower switch is off, and $h_m = 0$ in the opposite case.

The circuit representation of (1) can be given in terms of four controlled sources as depicted in Fig. 2. Thus, the equivalent circuit foresees a current source on the DC side (i.e., the left side) and three voltage sources on the three-phase AC side (i.e., the right side). Notice that the current on the DC side is intrinsically dependent on the AC side currents.

III. Parasitic Capacitances and External Networks

As far as conducted emissions are concerned (i.e., common- and differential-mode noise emission) parasitic capacitances and the external networks connected to the three-phase inverter must be considered (Fig. 3). On the DC side, a battery is connected to the inverter through a Line Impedance Stabilization Network (LISN) used to perform noise measurement under controlled conditions, and a large link capacitor C_{dc}. On the AC side, a three-phase shielded cable

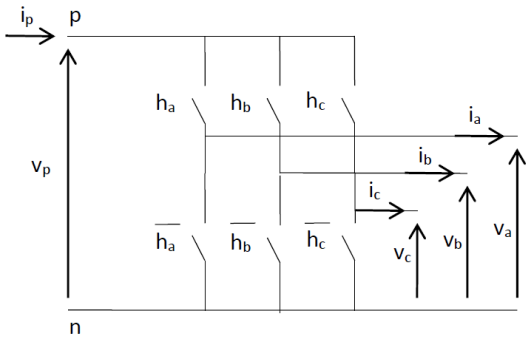

Fig. 1. Ideal three-phase inverter.

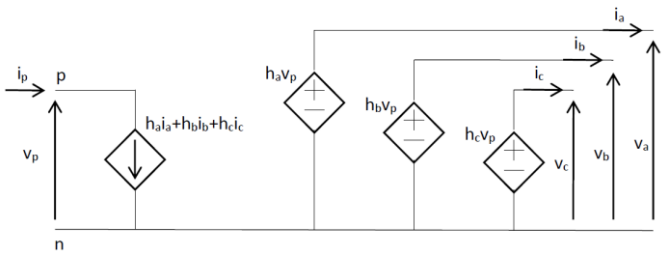

Fig. 2. Circuit representation of an ideal three-phase inverter as a four-port network.

connects the inverter to the load. Filters could be readily introduced in the circuit model, but at this point filters are not taken into account since the main objective of the proposed analysis is explaining the mechanism of interaction between differential and common mode noise.

The main parasitic capacitances are defined with respect to the cable shield (see dashed lines in Fig. 3). In particular, C_p and C_n are the parasitic capacitances of the positive and the negative (i.e., the inverter reference) terminals at DC side, whereas C_0 are the capacitances of the three inverter terminals at AC side. Finally, C_g is the total parasitic capacitance of the load with respect to the cable shield.

IV. Modal Analysis of the Equivalent Circuit

The equivalent circuit depicted in Fig. 3 can be regarded as a three-phase system (i.e., the AC side of the inverter, the three-phase components C_0, and the load) connected to a single-phase circuit (i.e., the DC side of the inverter, the parasitics C_p, C_n and C_g, the capacitance C_{dc}, the LISN, and the DC source).

In the relevant literature, a rigorous approach for the circuit analysis of three-phase systems interconnected with single-phase networks has been already proposed [9]-[10]. Such approach is based on the well-known Symmetrical Component Transformation (SCT) in its rational form (i.e., by assuming a unitary matrix as transformation matrix).

The SCT operates in the frequency domain, and the so-called zero-sequence components of the transformed voltages/currents correspond to the common mode voltages/currents in the noise analysis. As a consequence, the so-called positive- and negative-sequence components resulting from the SCT correspond to the differential mode noise [11]. The main results of such approach can be summarized in the following two points.

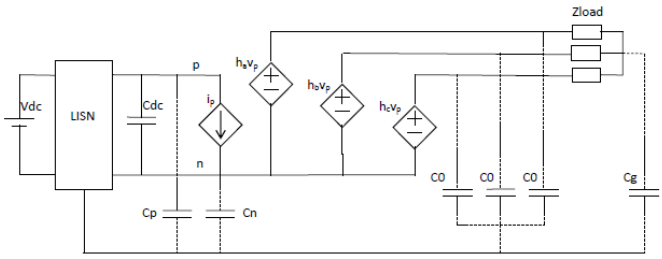

Fig. 3. Three-phase inverter connected to a DC source through a LISN and to a three-phase load. The main parasitic capacitances with respect the cable shield are also represented (dashed lines).

First, as far as positive- and negative-sequence components of the SCT are considered (i.e., the differential mode noise in the three-phase circuit), the star centers of the three-phase connections are all connected together to a common reference terminal. Thus, the single-phase network is not involved in such modal circuits. Second, as far as the zero-sequence components are considered (i.e., the common mode noise), it was derived in [9] that the interconnection between the three-phase and the single-phase networks can be represented as an ideal transformer with ratio $\sqrt{3}$. This simple result allows using the well-known properties of an ideal transformer to move electrical elements from one side to the other side of the transformer.

The results recalled above can be readily used in the modal analysis of the equivalent circuit in Fig. 3. First, the differential-mode noise analysis of the three-phase network can be easily performed by considering the equivalent circuits for the positive- and negative-sequence components of the SCT (see Fig. 4). Of course, only the three-phase circuit is represented since, as mentioned before, the single-phase circuit is not involved. The voltage source in Fig. 4 is the positive/negative sequence component obtained through the SCT of the three-phase voltage source in Fig. 3. Thus, it is worth noticing that the voltage source in Fig. 4 is proportional to the differential noise voltage v_p on the DC side. Therefore, the differential mode noise on the DC side affects the differential mode noise on the AC side.

Second, the common-mode noise analysis can be performed by considering the equivalent circuit for the zero-sequence components of the SCT. By using the results summarized above, the zero-sequence equivalent circuit can be represented as in Fig. 5. Simple analysis of such equivalent circuit leads to the following important point. The differential mode noise on the DC side is mainly due to the current source i_p which is controlled by the load currents i_a, i_b, i_c. Thus, the differential mode noise on the DC side is strongly dependent on the three-phase load. This point was already put into evidence in [8] where, however, an inappropriate circuit model was adopted since a voltage source instead of a current source was used on the DC side. A proper differential-mode noise model of the DC port, therefore, consists in a current source whose magnitude is strongly dependent on the three-phase load. Thus, any attempt to obtain a differential-mode noise source consisting in an independent source on the DC side is not correct from a methodological viewpoint. In the next Section some numerical simulations are provided to validate this point.

Notice that the proposed approach takes into account deterministic CE coming from circuit switching. Stochastic noise [12] effects will be investigated in future works.

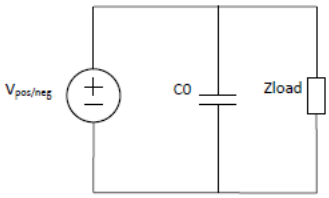

Fig. 4. Positive/negative-sequence circuit for the circuit in Fig. 3. This circuits takes into account differential mode noise on the AC side.

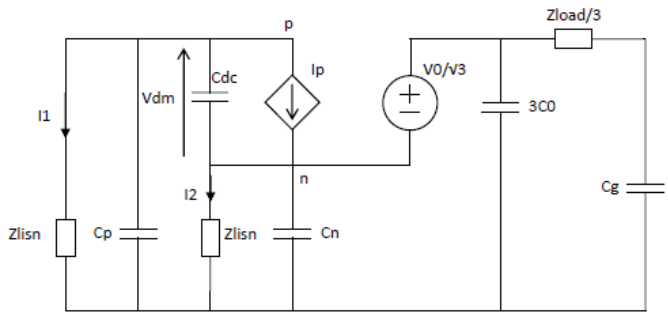

Fig. 5. Zero-sequence equivalent circuit for the circuit in Fig. 3. It clearly represents the interaction between common mode noise and differential mode noise on the DC side.

V. Numerical Validation

A three-phase inverter according to Fig. 3 was implemented in Simulink/Matlab (see Fig. 6). The DM noise current on the DC side is defined with reference to Fig. 5 as $I_{DM} = (I_1 - I_2)/2$, where I_1 and I_2 are the currents measured by the LISN. In order to validate the circuit model proposed in the paper, the simulated I_{DM} (obtained from the numerical values of I_1 and I_2 as mentioned above) is compared with the DM current I'_{DM} originating from the current source I_p calculated from the simulated load currents according to (1):

$$I_p = h_a I_a + h_b I_b + h_c I_c \tag{2}$$

By assuming $Z_{lisn} = 50\ \Omega$, due to the high impedance of parasitic capacitances C_p and C_n we can write:

$$I'_{DM} \cong I_p \frac{Z_{dc}}{Z_{dc}+2Z_{lisn}} \tag{3}$$

where Z_{dc} is the impedance of the link capacitor C_{dc}. In fact, at higher frequencies a capacitor can be represented as a series RLC equivalent circuit (see Fig. 6). Notice that due to the assumed symmetry of the two LISN impedances, the contribution of the zero-component voltage source in Fig. 5 to the DM current is null.

It is worth noticing that from (2) and (3) we expect that the DM current is dependent on the inverter modulation (i.e., h_a, h_b, h_c), and on the load (i.e., I_a, I_b, I_c). The following simulations were performed to validate this point.

The Simulink circuit in Fig. 6 was simulated in the discrete time domain with sampling frequency 400 MHz. Then the measured currents were processed in Matlab by evaluating the FFT in order to obtain the amplitude spectra in the frequency domain. The parameters in Fig. 6 were selected as follows: $V_{dc} = 100\ V$, $L_s = 1\ mH$, $R_{lisn} = 50\ \Omega$, $C_{lisn} = 1\ \mu F$, $R_{dc} = 10\ m\Omega$, $C_{dc} = 1\ mF$, $L_{dc} = 100\ nH$, $C_p = C_n = 1\ nF$, $C_0 = C_g = 10\ nF$, $R_{load} = 1\ \Omega$, $L_{load} = 1\ mH$.

The modulating frequency is 50 Hz and the carrier frequency is 1650 Hz (i.e., the frequency-modulation ratio is 33), whereas the amplitude-modulation ratio m is 0.95. The amplitude spectrum of the differential mode current is represented in Fig. 7 in the frequency range bounded by the conventional upper value 30 MHz. Comparison between simulations (blue curve) and analytical approximate results based on (3) (red curve) shows good agreement (getting worse as frequency increases).

Fig. 8 shows the effect of the three-phase load. The load resistance (of the three phases) was changed from 1 Ω to 0.1 Ω. Compared to Fig. 7 the emissions are larger, and the proposed model works properly, showing that the differential mode current on the DC side is a function of the three-phase load.

In Fig. 9 the value of the amplitude-modulation ratio m was changed with respect to Fig. 7 from 0.95 to 0.5. Lower emission levels can be observed. As it was expected, the conducted emissions are functions of the amplitude-modulation ratio as well.

Finally, Fig. 10 shows the impact of the value of the parasitic inductance L_{dc} in the high-frequency model of the link capacitor. Since the peaks in Figs. 7-9 are due to resonances, it is expected that by decreasing such parasitic inductance the resonance frequencies increase. Actually the main peak in Figs. 7-9 is around 6 MHz, whereas the frequency location of the same peak in Fig. 10 is shifted to a double value since the inductance was selected four times smaller (i.e., 25 nH instead of 100 nH as in Figs. 7-9).

VI. Conlusion

The proposed methodology shows in a clear and rigorous way the interaction between the AC and the DC sides of a three-phase inverter (including the main parasitics) when differential and common mode noise must be evaluated. In particular, it was shown that the differential mode noise on the DC side is dependent on the three-phase load and on the amplitude modulation. The proposed approach based on a four-port network modeling of a three-phase inverter is well suited for a better understanding of noise generation and propagation. Future work will be devoted to further investigation of the role of parasitics and experimental validation of the analytical results derived in the paper.

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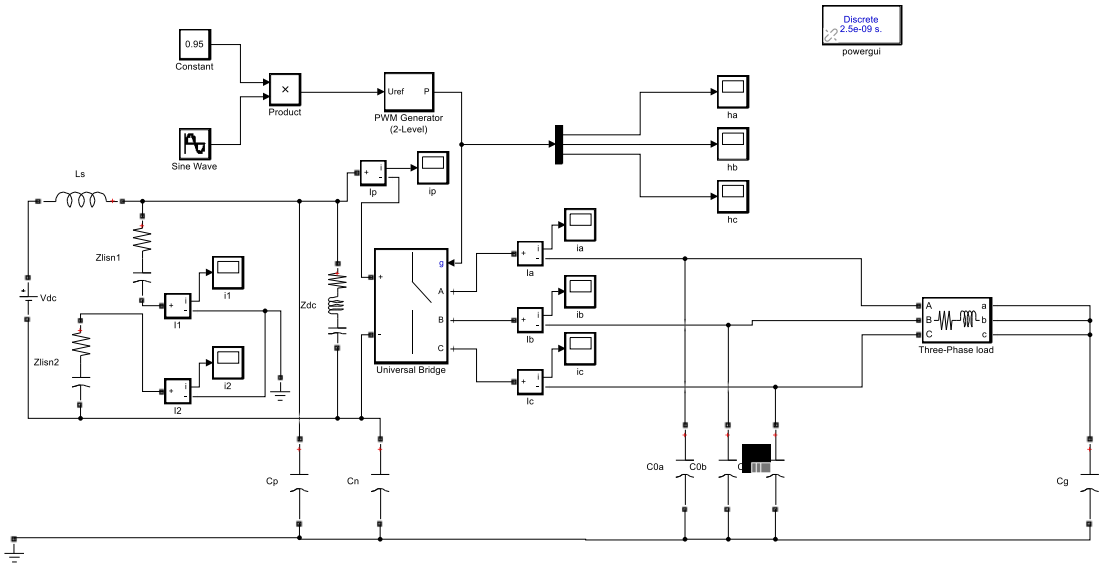

Fig. 6. Simulink model of a three-phase inverter including the main parasitic capacitances, the high frequency model of the link capacitor, and the LISN.

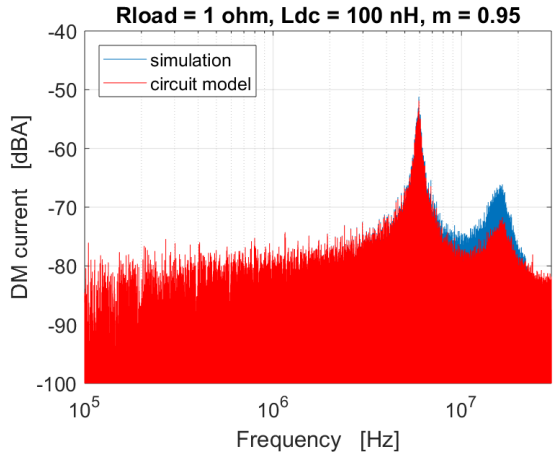

Fig. 7. Amplitude spectrum of the differential mode current in Fig. 6. Comparison between simulations (blue curve) and analytical results (3).

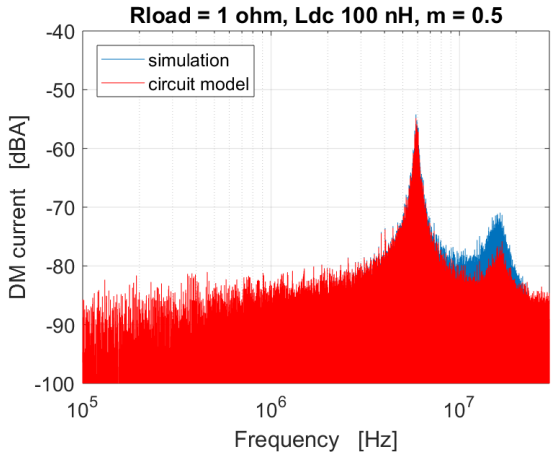

Fig. 9. Frequency behavior of the differential mode current for a different value (i.e., 0.5) of the amplitude-modulation ratio *m* with respect to Fig. 7.

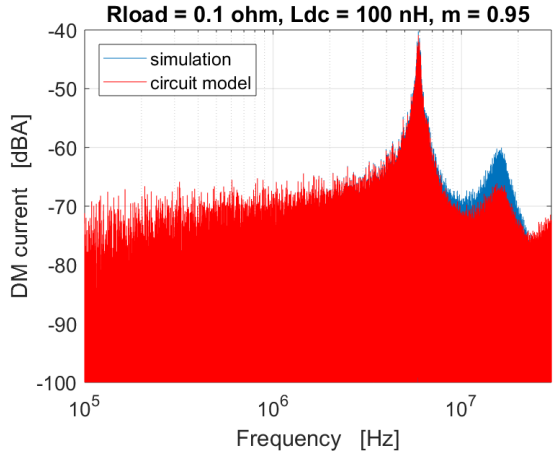

Fig. 8. Frequency behavior of the differential mode current with a lower value of the resistance in the three-phase load with respect to Fig. 7.

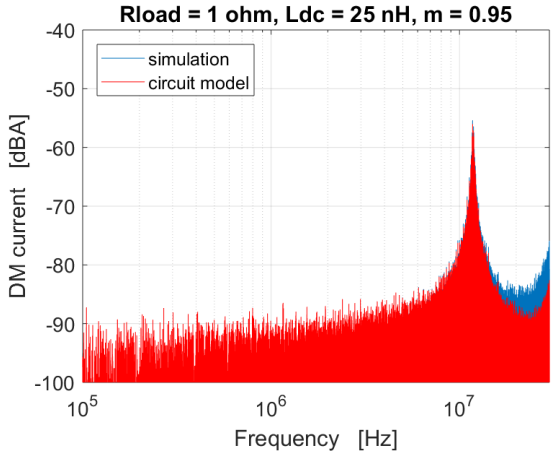

Fig. 10. Frequency behavior of the differential mode current for a lower value of the inductance L_{dc} in the high-frequency model of the link capacitor.

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