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REVIEW

Standards for the Characterization of Endurance in Resistive Switching Devices

Mario Lanza,* Rainer Waser, Daniele Ielmini, J. Joshua Yang, Ludovic Goux, Jordi Suñe, Anthony Joseph Kenyon, Adnan Mehonic, Sabina Spiga, Vikas Rana, Stefan Wiefels, Stephan Menzel, Ilia Valov, Marco A. Villena, Enrique Miranda, Xu Jing, Francesca Campabadal, Mireia B. Gonzalez, Fernando Aguirre, Felix Palumbo, Kaichen Zhu, Juan Bautista Roldan, Francesco Maria Puglisi, Luca Larcher, Tuo-Hung Hou, Themis Prodromakis, Yuchao Yang, Peng Huang, Tianqing Wan, Yang Chai, Kin Leong Pey, Nagarajan Raghavan, Salvador Dueñas, Tao Wang, Qiangfei Xia, and Sebastian Pazos

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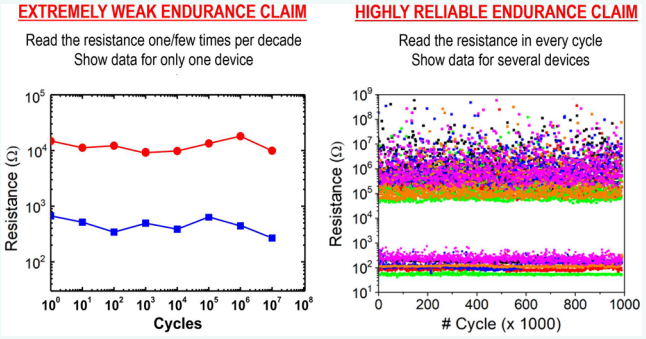
ABSTRACT: Resistive switching (RS) devices are emerging electronic components that could have applications in multiple types of integrated circuits, including electronic memories, true random number generators, radiofrequency switches, neuromorphic vision sensors, and artificial neural networks. The main factor hindering the massive employment of RS devices in commercial circuits is related to variability and reliability issues, which are usually evaluated through switching endurance tests. However, we note that most studies that claimed high endurances >10^6 cycles were based on resistance *versus* cycle plots that contain very few data points (in many cases even <20), and which are collected in only one device. We recommend not to use such a characterization method because it is highly inaccurate and unreliable (*i.e.*, it cannot reliably demonstrate that the device effectively switches in every cycle and it ignores cycle-to-cycle and device-to-device variability). This has created a blurry vision of the real performance of RS devices and in many cases has exaggerated their potential. This article proposes and describes a method for the correct characterization of switching endurance in RS devices; this method aims to construct endurance plots showing one data point per cycle and resistive state and combine data from multiple devices. Adopting this recommended method should result in more reliable literature in the field of RS technologies, which should accelerate their integration in commercial products.



KEYWORDS: *resistive switching, memristor, memory, variability, reliability, characterization, metal-oxide, endurance*

Resistive switching (RS) devices are materials systems in which two or more metallic electrodes are connected to an insulating or semiconducting material, whose electrical resistance can be adjusted to specific values (*i.e.*, states) by applying electrical stresses.[1] Most RS devices reported to date have exhibited two resistance states, often referred to as high-resistance state (HRS) and a low-resistance state (LRS), although RS devices with up to 100 states (often referenced with numbers from 1 to *n*) have been also reported.[2] Depending on the number of resistance states and their stability, RS devices may be used for different applications. For example, RS devices exhibiting one nonvolatile state and one volatile state can be used as selectors to minimize sneak path currents in crossbar array circuits[3] and are being considered for the hardware implementation of electronic neurons in deep neural networks (DNNs)[4] and spiking neural networks (SNNs).[5,6] RS devices exhibiting two nonvolatile states have been employed to construct radiofrequency switches,[7,8] logic gates,[9−11] stochastic computing systems,[12,13] and nonvolatile memories (NVM).[14−16] RS

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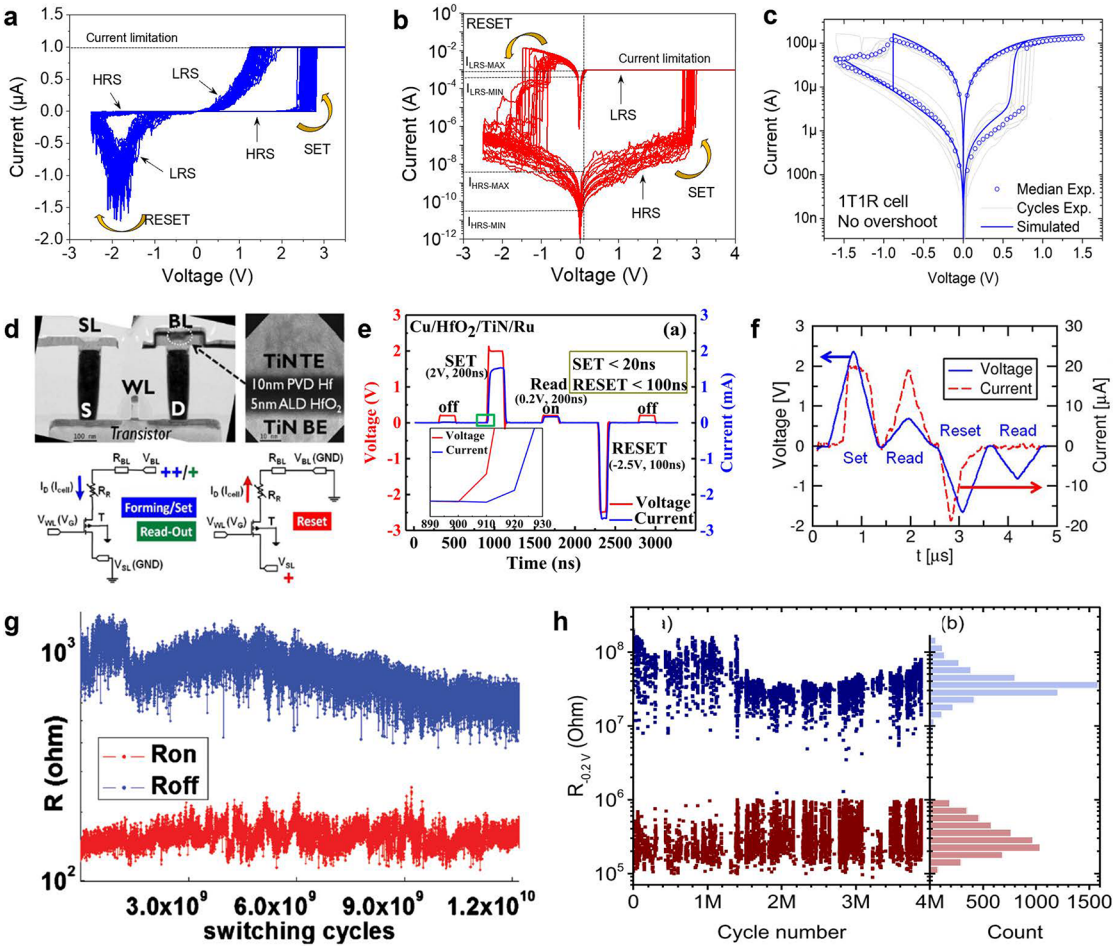

Figure 1. Characterization of the resistive switching phenomenon. (a, b) Current-limited *I*−*V* plots demonstrating the presence of nonvolatile bipolar RS in Au/h-BN/Au devices, using linear and logarithmic current scales, respectively. Each plot shows several lines measured in the same device, displaying the cycle-to-cycle variability of the currents. In panel (b) the overshoot can be seen, as the reset current is higher than the current limitation; this indicates that the current limitation tool from the SPA did not act immediately. Reprinted with permission from ref 36. Copyright 2020 Nature. (c) *I*−*V* curves collected in a memristor connected to a transistor. The current limitation takes place immediately and there is no overshoot. Reprinted with permission from ref 118. Copyright 2021 MDPI. (d) Cross-sectional TEM image of a 1T1R cell and equivalent electrical circuit used for forming, set and reset polarization. Reprinted with permission from ref 27. Copyright 2012 IEEE. (e) *I*−*t* plot demonstrating the presence of nonvolatile bipolar RS in Cu/HfO_2/TiN/Ru devices when applying rectangular PVS. Reprinted with permission from ref 33. Copyright 2017 IEEE. (f) *I*−*t* plot demonstrating nonvolatile bipolar RS in Ti/HfOx/TiN device when applying triangular PVS. Reprinted with permission from ref 34. Copyright 2015 IEEE. (g, h) R_{HRS} and R_{LRS} *vs* cycle plots displaying the write endurance of RS devices with different compositions. (g) Reprinted with permission from ref 91. Copyright 2010 AIP Publishing. (h) Reprinted with permission from ref 147. Copyright 2014 AIP Publishing.

devices exhibiting multiple nonvolatile and stable states are being considered for the hardware implementation of electronic synapses in DNNs, as they allow implementing computing algorithms (*e.g.*, backpropagation) by updating and maintaining multiple conductance states in each training iteration (often referred to as epoch).[17,18]

Despite multiple device structures exhibiting RS have been reported (*i.e.*, planar junctions, memtransistors),[19,20] so far the only one being considered by the semiconductor industry is the crossbar array of vertical metal/insulator/metal (MIM) nanocells.[21−23] The use of crossbar arrays of RS devices for the aforementioned applications is interesting because: (i) this circuital architecture is reasonably easy to fabricate (it requires few lithography steps, less than, for example, a transistor), which makes it also relatively cheap;[1] (ii) it offers a very high integration density (~100 Gbit/cm^2),[24] which can be further enhanced by using three-dimensional (3D) configurations;[25] (iii) their electrical properties can be tuned (by using different metallic and insulating materials) to fit the technological requirements of different applications;[21] and (iv) the yield, variability, reliability, and stability reported are the best among all RS device architectures.[14−16,26] It is worth noting that many industrial crossbar arrays employ one transistor in series with each RS device.[27−32] At the same time, this configuration (often referred as one-transistor/one-resistor, or 1T1R structure) provides a superior control when programming the conductance of each RS device, and it reduces the integration density and increases the complexity of the fabrication process.

The two typical figures-of-merit confirming the presence of RS in bistable devices are (i) current *vs* voltage (*I*−*V*) plots created during the application of ramped voltage stresses (RVS) and (ii) current *vs* time (*I*−*t*) plots created during the application of pulsed voltage stresses (PVS). When applying RVS, the presence of RS can be confirmed by the detection of a current increase (HRS-to-LRS transition, *i.e.*, set) and a

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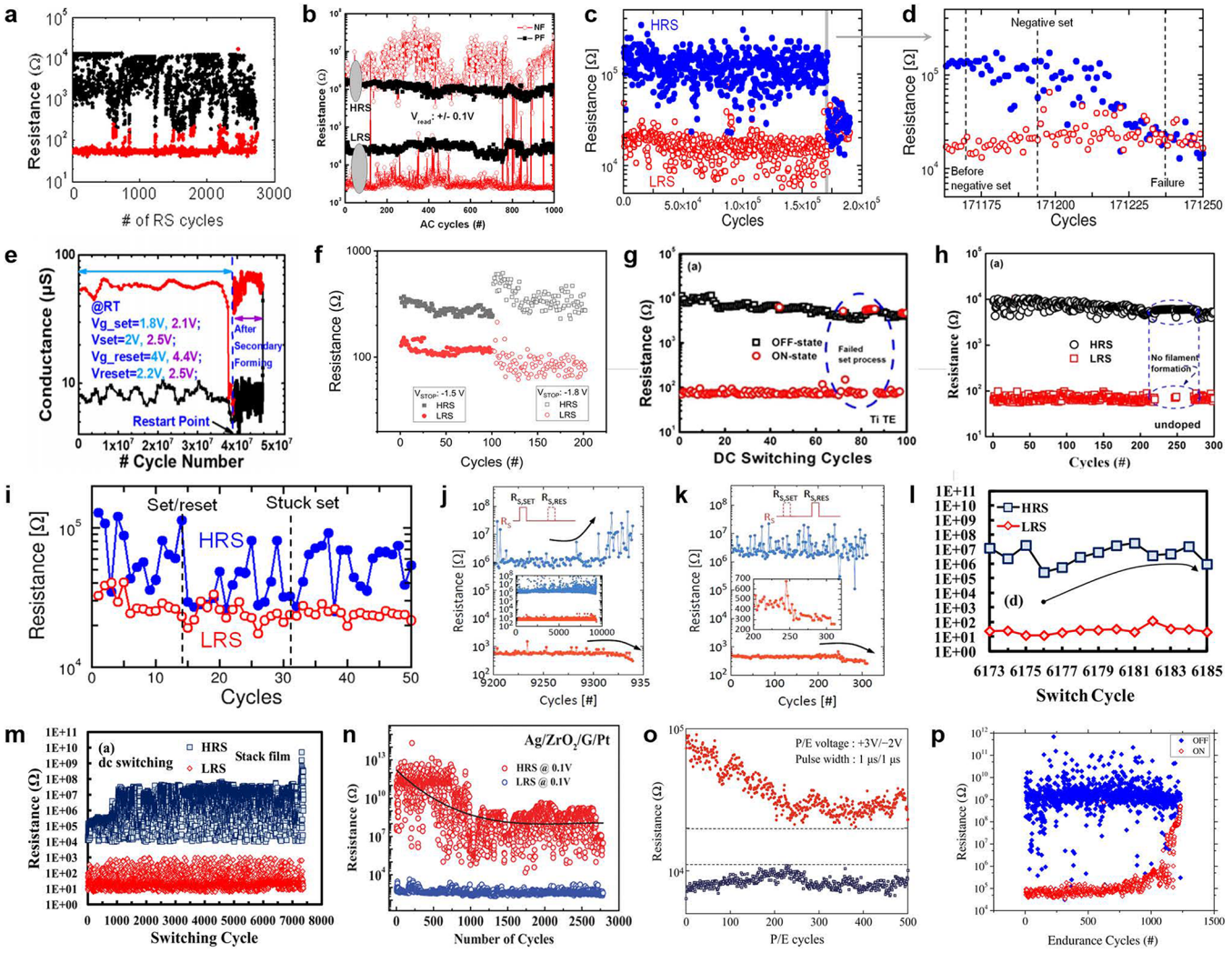

Figure 2. Examples of endurance plots showing undesired and unexpected fluctuations on the values of R_{HRS} and R_{LRS} as the RS device is switched for several cycles. (a) Clear stochastic fluctuations. Reprinted with permission from ref 39. Copyright 2011 AIP Publishing. (b) Similar stochastic fluctuations. Reprinted with permission from ref 40. Copyright 2012 Springer. (c) A progressive decrease of the value of R_{HRS} until the device gets stuck in the LRS. (d) Magnified image of (c) at the gray vertical line. Reprinted with permission from ref 34. Copyright 2015 IEEE. (e) A sudden decrease of the resistance in R_{HRS}, and the device becomes stuck in the LRS. Reprinted with permission from ref 49. Copyright 2019 IEEE. (f) How the values of RHRS and R_{LRS} change with the magnitude of the stress applied, which changes the value of R_{HRS}/R_{LRS} and the variability. Reprinted with permission from ref 51. Copyright 2020 MDPI. (g–i) Examples of endurance plots in which the device does not switch for some cycles. (g) Reprinted with permission from ref 52. Copyright 2017 Nature. (h) Reprinted with permission from ref 53. Copyright 2016 ACS. (i) Reprinted with permission from ref 34. Copyright 2015 IEEE. (j–o) Endurance plots of some devices that experience resistance and variability shift as the stress proceeds. (j, k) Reprinted with permission from ref 54. Copyright 2016 Nature. (l, m) Reprinted with permission from ref 55. Copyright 2016 AIP Publishing. (n) Reprinted with permission from ref 56. Copyright 2016 Wiley-VCH. (o) Reprinted with permission from ref 57. Copyright 2015 Springer. (p) Failure of a device because it becomes stuck in R_{HRS}. Reprinted with permission from ref 58. Copyright 2017 AIP Publishing.

current decrease (LRS-to-HRS transition, *i.e.*, reset) in the *I*−*V* plot (see Figure 1a); this produces that, for a given read voltage (typically ∼0.1 V), the currents read in the forward and backward sweeps are different (*i.e.*, there is a gap between them), and the resistances (R_{HRS} and R_{LRS}) can be calculated. This plot is also often given as the logarithm of the absolute value of the current (see Figure 1b), which allows visualizing the R_{LRS}/R_{HRS} ratio much more clearly. It is worth noting the RVS aimed to collect hysteretic *I*−*V* curves are normally current limited, either using the semiconductor parameter analyzer (Figure 1b) or using a series transistor (Figures 1c,d) or resistor. Collecting *I*−*V* sweeps can be very slow, especially when registering small currents <1 nA, and in some cases measuring one single RS cycle can take tens of seconds and up to 1 min. When applying PVS, pulses with relatively high voltages (typically >±2 V) are used to induce the state transitions, and read pulses with small voltages (typically ∼0.1 V) are intercalated to read the current; then, the values of R_{HRS} and R_{LRS} are calculated dividing the read voltage by the average current detected during the read pulses. Most researchers employ PVS with a rectangular shape (Figure 1e),[33] although triangular PVS have also been employed (Figure 1f);[34] this could be considered another type of PVS. The *I*−*t* plots obtained during PVS may allow quantifying the set and reset times (t_{SET} and t_{RESET}), which could be used to calculate the set and reset energies (E_{SET} and E_{RESET}). Moreover, all RS technologies work under PVS; for these reasons, and because (in general) it is much faster, the application of PVS is the

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most recommended method to study RS devices. Confirming the presence of RS in multistate devices is also carried out through the same figures-of-merit ($I-V$ and $I-t$ plots). Still, in such cases determining the state resistances and the switching voltages, energies and times reliably are often more complex due to the smaller differences between the states (*i.e.*, the value of R_{LRS}/R_{HRS} in a bistable RS device is normally much higher than the value of R_{n+1}/R_n in a multistate device, where $n + 1$ is the state adjacent to n that is more conductive than n).[35]

One of the most important properties of RS devices for any application is the write cycling endurance. In the field of RS, this is defined as the maximum number of programming cycles that a device can undergo before its electrical characteristics start to deviate outside the allowed ranges (often called the operation window),[26] even if that happens only temporarily during one cycle. In bistable RS devices, one operating cycle is defined as one set transition plus one reset transition;[1] in multistate RS-based devices, the definition of cycling endurance is not so well established, although some authors defined it as the number of transitions from the most to the least resistive states stopping at all intermediate states (*i.e.*, potentiation) and back to the most resistive state (*i.e.*, depression).[2] The required electrical characteristics of RS devices and their allowed ranges for multiple electronic technologies are described in detail in ref 21. For example, the typical operation windows for RS devices used as NVM are $R_{HRS}/R_{LRS} > 10$, V_{SET} and $V_{RESET} < 1$ V, E_{SET} and $E_{RESET} < 10$ pJ, t_{SET} and $t_{RESET} < 10$ ns, t_{HRS} and $t_{LRS} > 10$ years, where R, V, E, and t denote resistance, voltage, energy, and time, respectively, and t_{HRS} and t_{LRS} are the duration of the resistances states if no electrical stress is applied, often referred as retention times. In RS devices for other applications, additional figures-of-merit may also be important, such as LRS resistance and HRS capacitance in radiofrequency switches (which should be <50 Ω and <2 fF, respectively),[7] switching slope in selectors and electronic neurons (which should be <1 mV/decade),[36] and linearity in multistate electronic synapses for ANNs (which is evaluated through the linearity factor, c, in the equation $G = G_{MIN} + G_0[1 - e^{-cN}]$, which ideally should be 0). In this expression G is the conductance of a given state, G_{MIN} is the minimum conductance, G_0 is a constant value describing the conductance window, and N is the number of pulses of equal voltage applied.[37,38]

After a number of operating cycles, the electrical characteristics of RS devices may start to deviate until failure, either because the devices become stuck at one specific resistance state or because their electrical characteristics stop matching the technological requirements or their allowed tolerances. Therefore, characterizing and quantifying the endurance of RS devices is critical to assess their reliability and potential for integration in commercial electronic systems. As measuring all the parameters of RS devices (*e.g.*, R_{HRS}, R_{LRS}, V_{SET}, V_{RESET}, E_{SET}, E_{RESET}, t_{SET}, t_{RESET}, t_{HRS}, t_{LRS}, linearity, capacitance, *etc.*,) for a large number of cycles is not feasible, the indicator selected in most cases to quantify the cycling endurance is the resistance, and plots showing the values of R_{HRS} and R_{LRS} *vs* cycle number (often referred as endurance plot) have been presented (see Figure 1g,h). Unfortunately, the endurance plots reported in many research articles have been constructed using methods that are highly questionable; this has created a blurry vision of the real endurance (and reliability) of RS devices. In this review, we aim at clarifying which are the most convenient methods to quantify the endurance of RS devices and to summarize which endurance claims have been supported by enough data and which require further demonstrations.

FAILURE MECHANISMS

In RS devices, the set and reset transitions are induced by applying electrical stresses to the metallic electrodes, which produce the modification of the atomic structure of the insulator or semiconductor between them.[1] While the magnitude of the stress-induced structural changes can be roughly adjusted by tuning the voltage, duration, and separation of the PVS, accurate control of the number of atoms moved in each cycle and their position in the device has never been achieved and it is considered to be impossible.[12,13] Therefore, the conductance in LRS (after set) and in HRS (after reset) can be very different after each RS cycle (Figure 2a,b),[39,40] and the switching voltages, times, and energies may also be slightly different in each cycle,[33] which is why it is often said that the RS is a stochastic phenomenon.[12,13] In fact, the cycle-to-cycle variations of R_{HRS}, R_{LRS}, V_{SET}, V_{RESET}, E_{SET}, E_{RESET}, t_{SET}, and t_{RESET} are so unpredictable that they have been employed as an entropy source in true random number generators (TRNG) and physical unclonable functions (PUF) for data encryption.[41−43]

Most MIM-like RS devices fail during cycling because of the degradation of their microstructure, often associated with the irreversible penetration of metallic atoms from the electrodes and/or the formation of atomic vacancies in the insulator (*e.g.*, O vacancies in HfO_2);[44,45] this results in a permanent LRS (see Figure 2c,d).[34] Thermal effects related to the high currents flowing in LRS can also contribute to accelerate the degradation of the insulator, as they promote atomic diffusion.[46−48] In this article, we are not examining all the physical, chemical, and thermal phenomena producing incorrect/undesired ionic motion in RS devices resulting in endurance failure, for two reasons: (i) RS devices have been fabricated using many different materials and discussing all of them in detail would be very space consuming; and (ii) multiple articles have claimed switching mechanisms and movement of ions without any solid evidence, just drawing speculative schematics based on imagination, and that are not supported by any nanochemical measurement or atomistic simulation, which are the recommended characterization methods. There is a huge amount of misleading and erroneous literature in this field, and we do not want to promote it. Even in the case of oxygen vacancies in transition-metal oxides, which has been studied in hundreds of articles, the community still did not agree on where the oxygen atoms go (some articles claim that they form a reservoir at the interface, and some others claim that they interact with the electrode forming a metal oxide). For more information related to the endurance failure mechanisms of each specific RS device, please explore the literature about a specific materials combination.

The degradation of the microstructure of an insulator is a process that might take place suddenly or progressively depending on the materials employed and their thicknesses. For example, ref 34 shows that in Ti/HfO_x/TiN devices, the values of R_{HRS}, R_{LRS}, and R_{HRS}/R_{LRS} experienced a progressive drift until the two states became indistinguishable (see Figure 2c,d). On the contrary, ref 49 shows that TiN/HfO_x/TEL/TiN devices reached the LRS abruptly (see Figure 2e); TEL stands for thermal enhanced layer, but the authors of this article did not share its composition. In addition, the same

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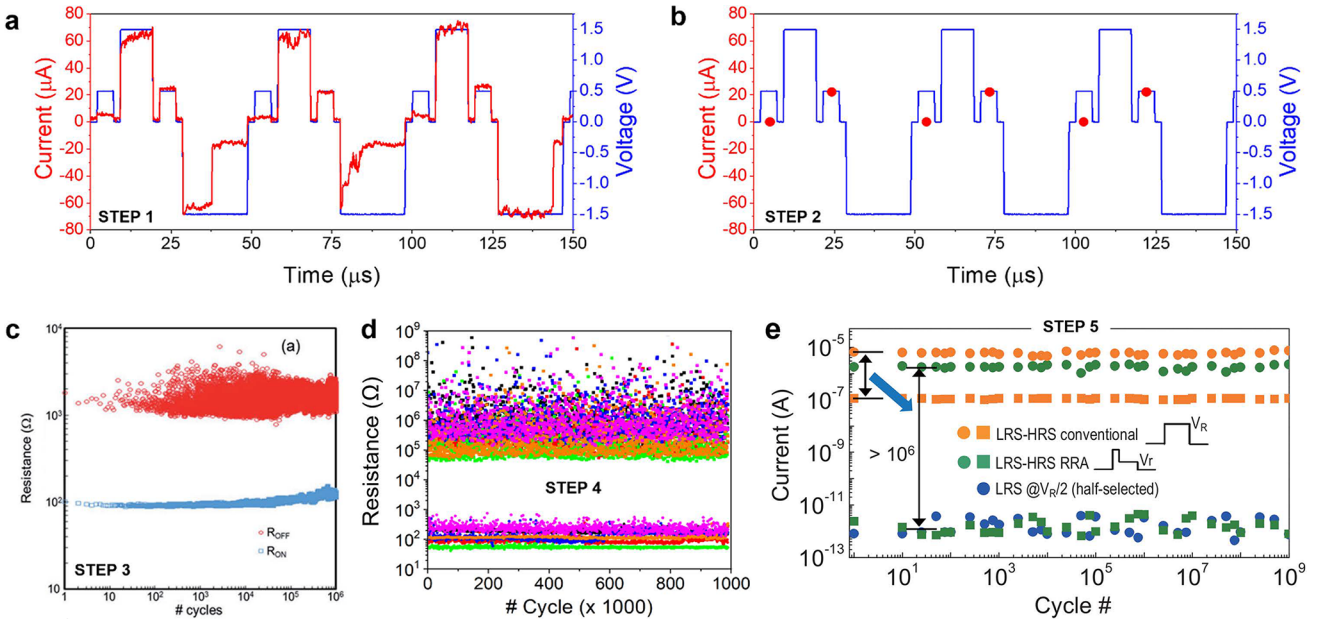

Figure 3. Recommended process to characterize the endurance of RS devices. (a) PVS displaying the currents through a MIM-like RS device when a sequence of read, write, read, and erase pulses is applied. (b) PVS with the same sequence as (a) but measuring current only during the read pulses. The read time is schematically indicated with a red ball. (c) Endurance of a Pt/Ta_2O_5/Ta device, showing the resistance in each cycle. Reprinted with permission from ref 176. Copyright 2017 Wiley-VCH. (d) Illustration of endurance plot for 10^6 cycles for five devices. (e) Endurance plot showing a few data points per decade, aiming to characterize high endurances >10^6 cycles. This test would be acceptable when only applied after steps 1−4 have been conducted. It is highly recommended to provide >50 points per decade for 10 devices. Reprinted with permission from ref 90. Copyright 2015 IEEE.

device may exhibit progressive endurance degradation when applying some specific electrical stresses and sudden endurance degradation for others (*e.g.*, larger voltage, current, duration).[50] The values of R_{HRS}, R_{LRS}, and R_{HRS}/R_{LRS} and their dispersions also depend on the stresses applied (see Figure 2f).[51] Moreover, sometimes the resistance of a RS device can get unpredictably stuck at one state for some time (*i.e.*, it stops switching even if read, write, and erase pulses are applied) and recover the normal functioning suddenly.[52] For example, if in one set event too many ions in the MIM cell have been displaced, the voltage applied to induce the reset might not be high enough. In such cases, triggering the reset may require several stresses in order to get those impurities to drift back, which means that the device is stuck in the LRS for some cycles (see Figure 2g,h),[52,53] and conversely, if in one cycle the reset event displaces too many ions, in the following cycle the voltage applied to induce the set may not be high enough; increasing again the conductance of the device may require the application of multiple stresses, leading to the device being stuck in the HRS for some cycles (see Figure 2g−i).[34,52,53] In addition, R_{HRS}, R_{LRS}, and their dispersions may suddenly or progressively change (see Figure 2j−o),[54−57] resulting in an alteration of the energy consumption per state transition. In the worst case, these unexpected changes can result in R_{HRS}/R_{LRS} being too low (*i.e.*, <10) for some cycles, or even permanently (see Figure 2o).[57]

It is also worth noting that RS devices may stick in an irreversible HRS (Figure 2p) because the metallic wires of the crossbar array melt due to the high currents driven in the LRS,[58] which promotes electromigration.[59] This has been often observed in RS studies coming from academia (where the stability of the materials is poorer and the contamination is higher than in the industry), especially when studying devices with wires narrower than 100 nm.

In multistate RS-based electronic synapses, endurance failure can be understood as a change in the number of resistance states per potentiation and depression cycle beyond an acceptable range. This can also be understood as a prohibitive change in the number of electrical stresses that one needs to apply to increase/decrease the resistance of the devices between the required value.

ENDURANCE CHARACTERIZATION METHOD

For all the above reasons, characterizing the cycling endurance of RS devices requires measuring their electrical properties in every cycle; otherwise, one has a very high probability that the switching is ineffective for some cycles, which leads to an overestimation of the endurance lifetime. Measuring R_{HRS} and R_{LRS} in every cycle is especially important when studying RS devices made of advanced materials (*e.g.*, 2D materials, MXenes, perovskites) and nanostructures (*e.g.*, nanowires, nanotubes, memtransistors), as their switching mechanisms and their reliability have not been demonstrated by different groups, and therefore, they are still controversial and not widely accepted. Unfortunately, many studies in the field of RS do not show robust enough evidence of high endurance, as they did not measure the resistance in every cycle; several studies even claimed endurances >10^6 cycles showing a plot with even <20 data points per state (in total),[60−86] which are insufficient to confirm the device reliability. Registering the current in few cycles also raises a doubt whether the applied electrical stress is the optimal biasing condition for practical applications. Moreover, most studies only display the endurance plot of one single device, ignoring how the dispersion of R_{HRS} and R_{LRS} varies from one device to another. These insufficient characterization results make it hard to evaluate the potential of the RS devices.

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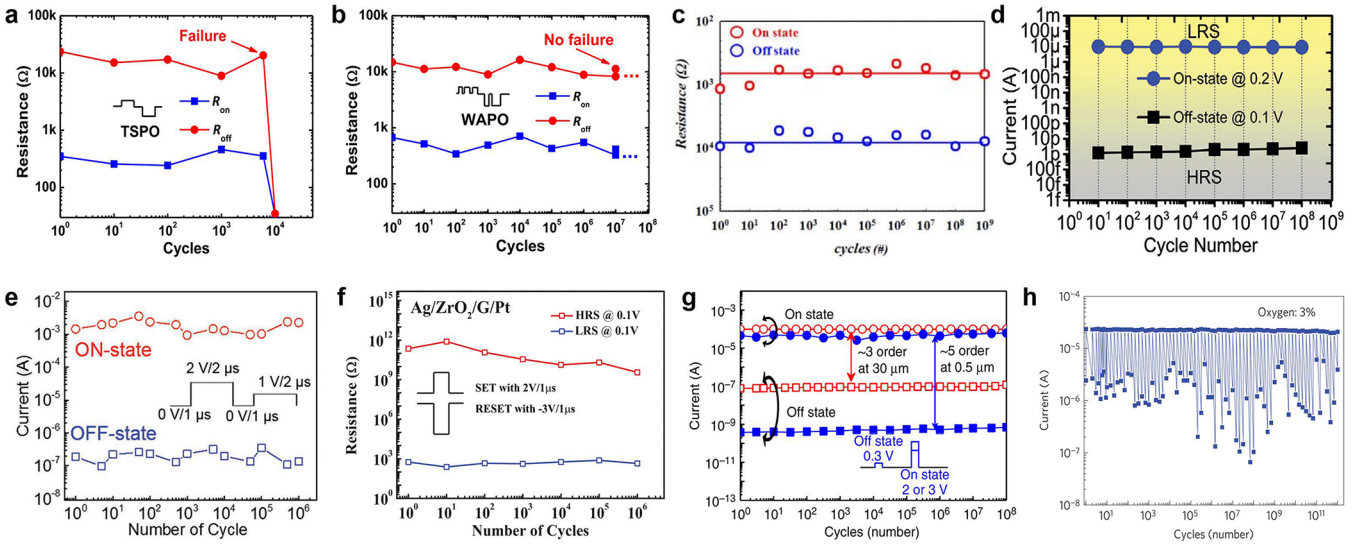

Figure 4. Examples of plots that do not provide enough data to reliably support their endurance claims. In these studies, R_{HRS} and R_{LRS} have not been measured in every cycle, so it cannot be confirmed that the devices actually switched so many times, and hence the cycle-to-cycle variability by be underestimated. (a, b) Reprinted with permission from ref 177. Copyright 2015 API Publishing. (c) Reprinted with permission from ref 68. Copyright 2014 IEEE. (d) Reprinted with permission from ref 100. Copyright 2021 Wiley-VCH. (e) Reprinted with permission from ref 101. Copyright 2018 Wiley-VCH. (f) Reprinted with permission from ref 56. Copyright 2016 Wiley-VCH. (g) Reprinted with permission from ref 62. Copyright 2013 Nature. (h) Reprinted with permission from ref 123. Copyright 2011 Nature.

The correct method to characterize the endurance of RS devices requires five steps, which need to be carried out sequentially. The first step consists of applying a sequence of read, write, read, and erase PVS during few (*i.e.*, <10) cycles and measuring the current simultaneously with a high temporal resolution (*e.g.*, 100 data points per voltage pulse). The typical resulting plot (Figure 3a) can be used to confirm the presence of RS by (i) observing the set and reset transitions and (ii) comparing the average values of R_{HRS} and R_{LRS} during the read pulses. However, the number of data points that standard measuring equipment can register in one sequence of PVS (*i.e.*, one run) is limited. For example, the Keysight B1500A and the Keithley 4200—two semiconductor parameter analyzers (SPA) widely used to study RS devices—cannot register more than 5000 data points per run. Using a temporal resolution of 100 data points per cycle, that means ∼50 cycles. If one wants to measure more data points, then one needs to first store all the data recorded and then run the PVS sequence again. While this operation can be automated with the software of the SPA, it produces an inherent delay of ∼30 s between each run that impedes the analysis of long endurances of millions of cycles. Sophisticated measuring setups may employ a software (*e.g.*, Labview, Matlab) to control the instrumentation and to read the data buffer of the SPA while it is measuring, so that the stress does not need to be interrupted.[87] In any case, plotting such a huge amount of data points may be very time-consuming and unfeasible for standard spreadsheet software (*e.g.*, Excel, Origin). Ref 88 presents a commercial integrated circuit for the characterization of crossbar arrays of RS devices; this circuit can overcome the limitations of the SPA in terms of data collection, and a recent study presented a high-speed amplifier capable to measure 10^5 $I-V$ sweeps per second.[89]

To avoid these problems, one can apply the PVS sequence and only register one current data point in each read pulse, as shown in Figure 3b (step 2). While this produces a loss of valuable information (*i.e.*, writing/erase currents, t_{SET}, t_{RESET}, E_{SET}, E_{RESET}), it allows measurement of the values of R_{HRS} and R_{LRS} during a few thousands of cycles in each PVS. By repeating this measurement (*e.g.*, using the loop tool in most commercial SPAs), it is relatively easy and fast to construct an endurance plot displaying the values of R_{HRS} and R_{LRS} for a few millions of cycles (see Figure 3c). Beyond 10^6-10^7 cycles, the methodology described in steps 2−3 to measure endurance could be very time-consuming. For example, if RS is measured using read, write, read, and erase PVS with a duration and interval of 1 μs (*i.e.*, time per RS cycle ∼8 μs), the total time needed to measure endurances of 10^{12} cycles would be ∼92 days. Despite the fact that measuring R_{HRS} and R_{LRS} for $>10^{10}$ cycles is possible and strongly recommended,[84] an alternative and acceptable measurement protocol would be as follows. First, repeat the measurement of endurance up to 10^6-10^7 cycles for multiple devices to confirm that the pulse voltages, duration, and interval produce acceptable switching and that the values of R_{HRS}, R_{LRS}, and R_{HRS}/R_{LRS} fit the technological requirements for each cycle and for each device (step 4). This is very important because variability is one of the most important problems of RS technologies.[26] One good way to do it is by presenting the resistance *vs* cycle plot for multiple devices overlapped (see Figure 3d). The more devices and cycles that one measures, the better, as it will allow a deeper understanding of not only the materials system employed but also the effect of the electrical stresses applied. Second, apply an additional endurance measurement on the same devices, keeping only few read pulses (randomly selected) per decade to speed-up the measurement, however extending the number of cycles far above 10^6-10^7 cycles, so that an endurance plot with enough statistical validity can be constructed (see Figure 3e, *i.e.*, step 5).

This method is similar to quality controls in which only a certain number of events and/or products of the total population are analyzed; therefore, again, the more cycles that one measures, the better. This method has been employed by companies to characterize the endurance of metal/TMO/

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Table 1. Endurance Reported for 2D Materials-Based RS Devices[a]

ref	structure	device structure and device sizes	endurance claim and data points	test method
119	G/$MoS_{2-x}O_x$/G	vertical MIM 25 μm × 25 μm	over 2 × 10^7 72 data points	pulse voltage stress
100	Pt/hBN/Ag	vertical MIM 250 nm × 250 nm	10^8 8 data points	pulse voltage stress
158	Au/MoS_2/Au	planar FET channel length (2 μm)	15 15 data points	$I-V$ sweeps
20	Au/MoS_2/Au	planar FET channel length (1−5 μm)	475 475 data points	$I-V$ sweeps
159	Au/Li_xMoS_2/Au	planar FET channel length (∼5 μm)	1000 1000 data points	pulse voltage stress
160	Au/MoS_2/Au	vertical MIM 2 μm × 2 μm	150 150 data points	$I-V$ sweeps
161	Ag/GaSe/Ag	planar FET channel length (∼30 μm)	5000 indistinguishable	$I-V$ sweeps
162	Au/Ti/MoS_2/Ti/Au	planar FET channel length (∼2 μm)	6 6 data points	pulse voltage stress
163	Au/α-In_2Se_3/Au	planar FET channel length (∼1 μm)	40 40 data points	$I-V$ sweeps
164	Cu/MoS_2/Au	vertical MIM 2 μm × 2 μm	21 21 data points	$I-V$ sweeps
165	Au/h-BN/Au	vertical MIM 1 μm × 1 μm	50 50 data points	$I-V$ sweeps
36	Ag/h-BN/Au	vertical MIM 150 nm × 150 nm	80,000 80,000 data points	pulse voltage stress

[a]High endurances (>1 × 10^6 cycles) have been only supported using plots that display few data points, and when the values of R_{HRS} and R_{LRS} are measured in each cycle, the maximum endurance recorded has been 80,000 cycles. Researchers in the field of RS should always use the correct characterization method (*i.e.*, report R_{HRS} and R_{LRS} in every cycle) instead of trying to oversell the endurance of their devices using an inaccurate method (*i.e.*, measure one/few data points per decade). The letters "*G*" and "h-BN" stand for graphene and hexagonal boron nitride, respectively.

metal RS devices that showed highly reliable switching behavior when applying steps 1−4, and values >10^9 cycles have been achieved (see Figure 3e).[3,90] Engineering the shape of the PVS to minimize reading times and maximize performance has also been reported.[3] In any case, measuring the value of R_{HRS} and R_{LRS} for >10^{10} cycles is possible (see Figure 1g)[91] and is the preferred way to do it.

DISCUSSION AND PROSPECTS

We have noticed that a considerable number of publications in the field of RS claimed very high endurances >10^7 cycles based on a plot that contains few (*i.e.*, < 100) data points for only one device (see Figure 4), that is, ignoring steps 1−4. Such a simplified method is less reliable than the one described in the previous section because it cannot confirm that the device has actually switched in every cycle. As mentioned, the value of V_{SET}, V_{RESET}, t_{SET}, and t_{RESET} can notoriously change in every cycle, and it could be possible that the application of the same pulse voltage or pulse duration could not induce the state transition or could damage the device. Furthermore, the endurance plots in Figure 4 ignore some of the most important challenges of RS technologies, which are cycle-to-cycle and device-to-device variability.[26]

In many cases endurance plots like those in Figure 4 have been created by applying a PVS without reading the current and interrupting the stress to read the resistance by applying either a PVS or an RVS. This process is different than the one described in step 5 of Figure 3 (see previous section), as it requires interrupting the stress and introduces a relaxation time (of the order of seconds).[92] This relaxation time may affect the state and its properties (*e.g.*, V_{SET}, V_{RESET}),[93] which means that the switching conditions might no longer be appropriate. It is therefore very important that same values of delays are applied between write pulses over the whole endurance test. The use of a RVS to read the current is even worse because the authors would be claiming high endurances without having confirmed that the device can switch when applying a PVS. This is important because an RVS will always reach V_{SET} and V_{RESET} and the device may switch; however, when applying a fast PVS, the voltage or duration may not be sufficiently high to always guarantee the switching, or else may be too high and could damage the device. Moreover, most RS studies employ RVS with a current limitation to prevent the degradation of the device, while this function is not available when applying the PVS with commercial SPA. Current limitation during PVS could also be achieved using a resistor or transistor in series with the RS cell; however, it should not be forgotten that conventional SPA systems do not provide sufficiently fast current limitation (during RVS) to prevent device damage during the set events, plus add additional parasitic capacitance effects; all of this has an impact in the endurance.[94−96] The overshot current caused by the parasitic capacitances leads to an excessive leakage current across the RS device after the forming and set process. In most cases it accelerates the device degradation. Overall, the total integrated stress during a RVS normally exceeds that of a PVS by orders of magnitude; therefore, the two types of measurements are not comparable. Disclosing details about the measuring protocol is very important.

In addition, MIM-like RS devices with different compositions (*i.e.*, materials, thicknesses) are likely to have different optimal biasing conditions. As their right balance is crucial for

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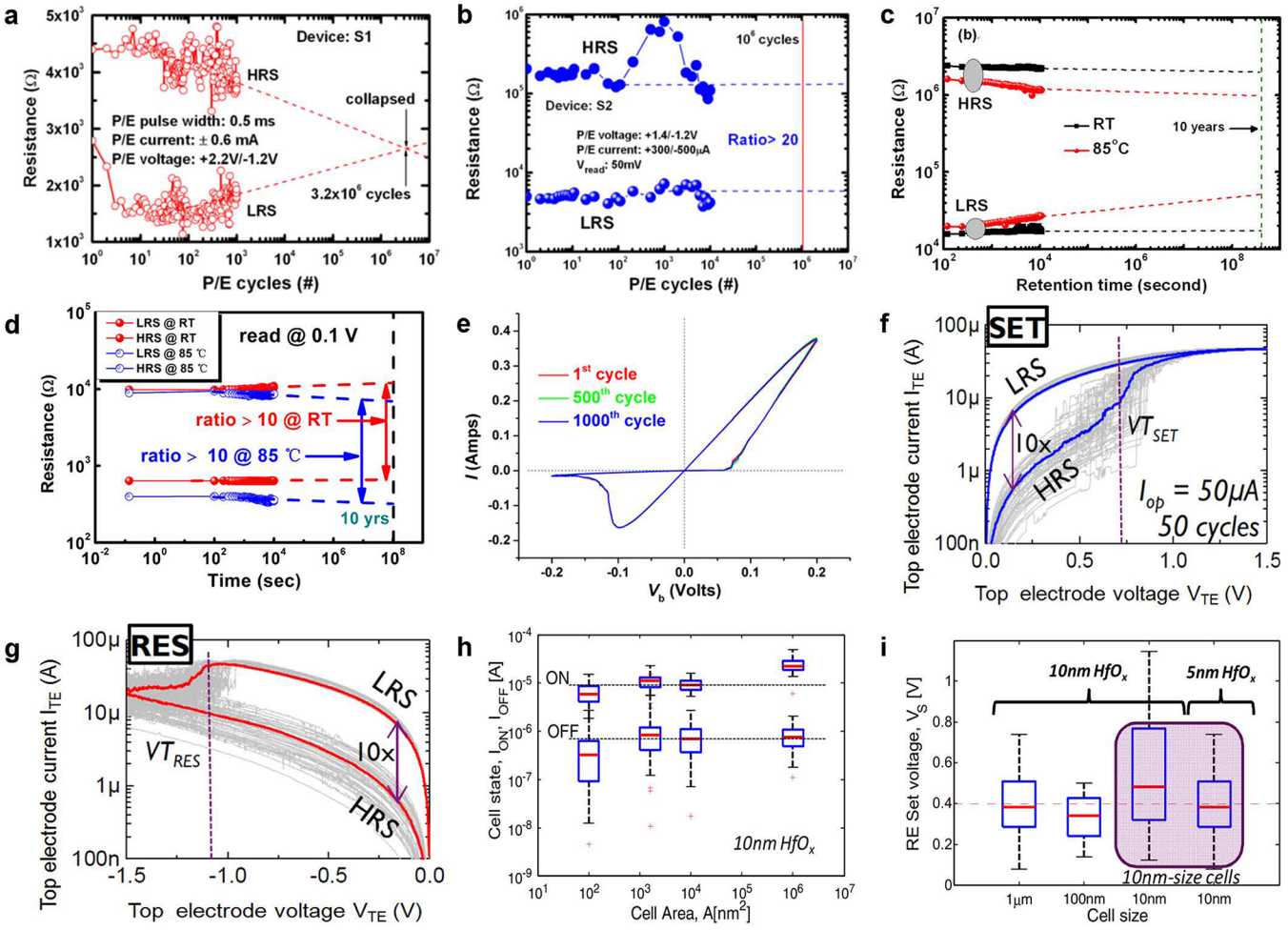

Figure 5. Additional considerations related to the estimation of endurance of RS devices. (a, b) Resistance *vs* cycle plot presenting a claim of endurance based on the drawing of dashed lines. This method is unreliable. The method used in Figure 3 is recommended. Reprinted with permission from ref 112. Copyright 2012 Springer. (c, d) Current *vs* time plot measured at a constant voltage to characterize the retention time of the RS device in HRS and LRS. The retention claim of 10 years is unreliable because it is based on extrapolation over several orders of magnitude. The correct method to measure the retention time of RS devices is explained in ref 49. (c) Reprinted with permission from ref 40. Copyright 2012 Springer. (d) Reprinted with permission from ref 113. Copyright 2013 Springer. (e) Current *vs* voltage plots for the 1st, 500th, and 1000th cycles of a MoS_2-based RS device. This method presenting the data is problematic, as it cannot confirm that the devices switched during all the 1000 cycles and ignores cycle-to-cycle variability. Reprinted with permission from ref 114. Copyright 2016 ACS Publishing. (f, g) Current *vs* voltage plots measured during 50 cycles in some state-of-the-art MIM-like RS devices fabricated in industrial facilities. These plots indicate the real variability of RS devices, and such a type of characterization is recommended. (f, g) Reprinted with permission from ref 115. Copyright 2014 IEEE. (h, i) Dispersion of the state currents and switching voltages in state-of-the-art MIM-like RS devices fabricated in an industrial facility. Reprinted with permission from ref 22. Copyright 2011 IEEE.

a high endurance,[97] the comparison between different devices becomes challenging. The popular strategy of using a fixed set of switching parameters for different stacks might lead to a false endurance quantification. If the write scheme is optimized for one specific stack, a potentially better stack could show inferior endurance due to suboptimal biasing. We think that this strategy is only valid if the biasing conditions are strictly specified by the application. In other cases, we recommend optimizing the switching parameters by adaptive programming for each tested stack (or even for each device) and comparing the optimized endurance. A respective algorithm has been demonstrated.[98]

In order to emphasize how important the measuring protocol is, Table 1 summarizes the highest cycling endurances ever reported for RS devices made (totally or partially) of 2D materials and indicates the structure and size of the device, the method used to characterize the endurance, and the number of points shown in each plot. As it can be observed, all endurance claims $>10^5$ cycles have been made presenting plots that contain <100 data points, while when measuring R_{HRS} and R_{LRS} in each cycle, the maximum endurance achieved is 80,000 cycles. The fact that the endurance registered strongly depends on the characterization method indicates their important effect on the device reliability. High endurances have been only achieved when measuring few cycles, which means that this method ignores failure mechanisms. Overall, making endurance claims based on plots showing few (*i.e.*, < 100) data points is risky and can be unreliable, especially if the authors are using advanced nanomaterials (*e.g.*, 2D materials, MXene or perovskites) in which the endurance has never been tested in each cycle before.

As explained in the previous section, in the context of RS devices measuring R_{HRS} and R_{LRS} for the first 10^6–10^7 cycles, they only take a few minutes or hours, so we do not see any

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Table 2. Highest Switching Endurances of RS Devices Ever Reported and the Number of Data Points Presented to Support Such Claims[a]

ref	structure	endurance claimed	data points presented	reliability of the claim
136	ITO(or Au)/$Ru(L)_3(PF_6)_2$/ITO	10^{12}	indistinguishable	high
91	Ta/TaO_x/Pt	$>10^{10}$	indistinguishable	high
147	Au/Ni/PR/Pt/Co/$BiFeO_3$/$Ca_{0.96}Ce_{0.04}MnO_3$/ $YAlO_3$	4×10^6	indistinguishable	high
98	Pt/Ta/ZrO_2/Pt	$> 10^6$	indistinguishable	high
97	TiN/TiO_x/HfO_x/TiN	$>10^6$	indistinguishable	high
174	Ag/10%Sb-GeS_2/W	$>10^5$	indistinguishable	high
179	Pt/Ta/TaO_x:Zr/Pt	2.9×10^{10}	indistinguishable	medium
131	Pt/TaO_x/Pt	$>10^9$	indistinguishable	medium
178	Ag/a-Si/poly-Si	$>10^8$	indistinguishable	medium
166	Pd/Ag/HfO_x/Ag/Pd	$> 10^8$	indistinguishable	medium
151	Ta/TaO_x/Pt	10^6	indistinguishable	medium
146	Au/BFO/BFTO/Pt	$>2 \times 10^5$	indistinguishable	medium
127	Au/Co-doped $BaTiO_3$ (BTCO)/Pt	10^5	indistinguishable	medium
141	Pt/BST/SRO/STO	10^4	indistinguishable	medium
143	Al/PEDOT:PSS/PMMA/ITO	10^5	indistinguishable	medium
150	TiN/HfO_x/TiN	10^{10}	~60	medium
167	Ta/TaO_x/TiO_2/Ti	10^{15}	~21	low
123	Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt	10^{12}	~75	low
120	Pt/TaO_x/Ta_2O_5/Pt	$>10^{12}$	~50	low
120	W/AlO/TaO_x/Doped ZrO_x/Ru	$> 10^{11}$	23	low
155	TE/SLT/BE (1S)	10^{11}	~60	low
168	Pt/AlO_δ/Ta_2O_{5-x}/TaO_y/Pt	10^{11}	~33	low
145	Ta/HfO_2/Pt	1.2×10^{11}	~34	low
60	Ag/$Ag_{33}Ge_{20}Se_{47}$/Ag	$>10^{10}$	4	low
128	TiN/Hf/HfO_2/TiN	10^{10}	~31	low
	TiN/Ti/HfO_2/TiN	10^{10}	~31	low
	TiN/Ta/HfO_2/TiN	10^6	25	low
140	TiN/Hf/HfO_2/TiN	10^{10}	~31	low
67	Ti/HfO_2(1)/O_2-HfO_2(9)/TiN	10^{10}	11	low
149	Pt/AlO_δ/Ta_2O_{5-x}/TaO_y/Pt	10^{10}	~32	low
68	TiN/Gd:SiO_2/ITO	10^9	10	low
61	Cu/HfO_2/Pt (1T1R)	$>10^8$	13	low
62	TiN/As-Ge-Te-Si-N/TiN (or Ni)	10^8	25	low
77	TiN/TiON/HfO_x/Pt	$>10^8$	22	low
135	TiN/Ti/HfO_2/TiN	10^8	~80	low
126	Pt/Au/MgO/Co_3O_4/Pt/Au	10^8	~74	low
69	Al/PFCF-rGO/ITO	10^8	9	low
70	Al/GO-PVK/ITO	10^8	9	low
71	Al/TPAPAM-GO/ITO	10^8	9	low
139	Al/BCP:GO/ITO	10^8	25	low
72	Ti/AlN/Pt	10^8	9	low
148	TiN/AsTeGeSiN/TiN/Pt	10^8	25	low
169	Pt/TaO_x/Ta	10^8	~55	low
32	TiN/Ti/HfO_x/TiN (1T1R)	10^8	~130	low
33	Cu/HfO_2/TiN/Ru	10^8	8	low
134	ITO/HfO_x/ITO	10^7	~150	low
117	Pt/SiO_2:Pt/Ta	3×10^7	~80	low
119	G/$MoS_{2-x}O_x$/G	$>2 \times 10^7$	~70	low
144	TiN/RTO WO_x/W/TiN	$>10^7$	~100	low
170	Cu/Cu-Te/GdO_x/W	$>10^7$	~44	low
73	TiN/a-C:H/Pt	10^7	9	low
74	ITO/AlN/ITO	10^8	9	low
152	TaN/ZrO_2/HfO_2/TiN	10^7	~70	low
154	Pt/Zn:SiO_x/TiN	10^7	~70	low
75	Cu/nanohole-graphene/HfO_2/Pt/Cu/HfO_2/Pt	10^7	11	low
22	TiN/Hf/HfO_2/TiN	10^7	~30	low
76	Cu/Cu-doped SiO_2/W	10^7	6	low
63	Graphene/PMMA:P3BT/Al/PET	10^7	15	low
125	Pt/TiO_2/TiN/Pt	2×10^6	24	low
64	Pt/Nb-doped $SrTiO_3$/Pt	$>10^6$	7	low

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Table 2. continued

ref	structure	endurance claimed	data points presented	reliability of the claim
65	PtSi-coated AFM tips/HZO/LSMO/LAO	$>10^6$	13	low
66	Ag/GeSe/Si_3N_4/W	$>10^6$	11	low
111	TiN/Hf/TaO/HfAlO/AlO/TiN	10^6	~22	low
129	TiN/Ti/HfO_x/TiN	10^6	~80	low
130	Au/Pt/$Bi_{1-\delta}FeO_3$/ $SrRuO_3$/$SrTiO_3$	10^6	~55	low
132	Ru/Ta_2O_5/TiO_2/Ru	10^6	~50	low
133	TiN/WO_x/W	10^6	~70	low
137	noble metal/NiO/noble metal	10^6	~60	low
142	TiN/Ti/HfO_x/TiN	10^6	~150	low
78	Pt/ZrO_x/HfO_x/TiN	10^6	7	low
121	Pt/Al/PCMO/Pt	10^6	~37	low
153	Pt/ZnO/Pt	10^6	7	low
171	Pt/Ni: SiO_2/TiN	10^6	~54	low
172	Al/TiN/Cu/TiW/Al_2O_3/W	10^6	25	low
173	Pt/HfO_x/ZrN_x	10^6	~64	low
122	Cu/$TiTe_x$/Cu-GST/$TiTe_x$/SiO_2/W	2×10^5	24	low
138	Al/PMMA/MLG/PMMA/ITO/PET	1.5×10^5	~150	low
79	Pt/ZrO_x/HfO_x/TiN	$>10^5$	6	low
157	Pt or Au/NP SiOx/Pt	10^5	25	low
175	Al/Cu/$Ge_{0.4}Se_{0.6}$/W	$>10^5$	~48	low
80	IrO_x/Al_2O_3/Ge NW_S/SiO_2/Si MOS structure	$>10^5$	12	low
81	Ni/HfO_x/n^+ Si	$>10^5$	9	low
82	Ni/GeO_x/HfON/TaN	10^5	6	low
83	Pt/$SrTiO_x$/Si	10^5	5	low
84	Al/PMMA/GO/PMMA/ITO	10^5	7	low
85	Al/TiO_x/Al	10^5	11	low
86	Cu/pV3D3/Al	10^5	9	low
124	TiN/HfO_x/AlO_x/Pt	10^5	~37	low
156	Pt/a-CO_x/SiO_2/W	5×10^4	~40	low

[a]Many studies in the field of RS claimed endurances $>10^5$ cycles based on plots that contain fewer than 50 data points, which are collected from one single device. Such claims need to be supported by much more abundant data, if possible, and collected on multiple devices. The rows with medium reliability are those for which, while showing abundant data, it looks like multiple cycles were not measured or the points were just skipped when plotted (which was not specified in the article). In this table the structure of the devices is given in most cases by the chemical name of materials and compounds, although others like PMMA are related to the acronym. For a detailed description of the structure of each device, please refer to the indicated reference.

convincing reason for not including such data in every RS publication. It is worth noting that the recommended method to characterize the endurance (Figure 3) requires reading the current during the pulsed voltage stress. The most common way to do this experiment is to (i) use an additional module of the SPA (*e.g.*, Keysight B1500A and Keithley 4200) that can apply a PVS and record current simultaneously and (ii) connect the RS device in series with a resistor, apply the PVS with the SPA, and measure the voltage of the resistor using a mixed-signal oscilloscope (although the resolution of the oscilloscope is much worse than that of the SPA,[99] especially when trying to measure R_{HRS}). Some authors, when asked to provide the values of R_{HRS} and R_{LRS} in every cycle during revisions in journals, argue that they do not have such setups. In such cases, collaborating with other scientists or simply making no claim of endurance would be better than claiming a value without enough supported statistical data. Some papers showed a plot like the one in Figure 3a to demonstrate correct switching (which confirms that they have the required hardware), but they select not to measure R_{HRS} and R_{LRS} in every cycle.[58,100−103] This practice should be avoided, as measuring 10^6 cycles applying PVS with a duration of 1 μs would take only a few minutes or hours; if the device does not switch in 1 μs, it is not useful for most RS technologies.

Regarding the number of devices to measure, it is obvious that the more the better (as for any other electronic device) and establishing a specific number to consider an article reliable would be subjective and controversial. As for any other product, controlling the quality of 100% of items fabricated for the entire required lifetime is not feasible. For this reason, quality controls in which only a small percentage of devices are tested are often applied. These processes bring an associated inherent trade-off: development time *vs* accuracy; and in most cases, companies do not reveal details about them. Nevertheless, it is known that the standard qualification procedure for memory endurance in the industry requires statistical results from a sufficiently large memory array (>kilobit size).[104,105] This characterizes endurance under the influences of cycle-to-cycle evolution and device-to-device variation. Therefore, a low bit error rate after cycling guarantees robust endurance. However, the array-level analysis with many devices is typically not available in the early development stage and in the academic research. Furthermore, the process control on the device variation is not optimized for most studies. In any case, we note that publications in top journals exploring other electronic devices (*e.g.*, FETs) often present data (*i.e.*, mobility, subthreshold swing) for >50 devices;[106−109] however, in the field of RS, the number of devices analyzed is (in general) strikingly lower, and most publications present data for one or

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few (*i.e.*, < 5) devices, especially in terms of endurance. Combined with the aforementioned low number of data points presented in many cases, the claim of high endurance is particularly unreliable. We think that presenting endurance data for at least 10 devices would be more reliable and at the same time feasible. This number is in line with the statistical reproducibility statements of some relevant journals.[110] A useful validation metric would be to plot the distributions of resistance states obtained for steps 1−4 and compare them with the distributions obtained for step 5, which would allow detecting any onset of degradation mechanisms.[111] Some companies also use verified-endurance tests, using algorithms like increasing-step-pulse-programming.[101]

Finally, we would like to point out some much less reliable claims of high endurances presented in some articles, consisting of measuring few cycles and drawing extended dashed lines (see Figure 5a,b).[112] Similar unwarranted extrapolations have also been done for HRS and LRS retention times (Figure 5 c,d).[40,113] Presenting a few current *vs* voltage ($I-V$) curves corresponding to a handful of selected cycles (see Figures 5e) also leads to underestimations of cycle-to-cycle variability.[114] With this method, the devices show a low variability of switching voltages and state currents, when the device currents could be experiencing larger variations from one cycle to another. The best variability in the switching voltages and state resistances demonstrated by visualizing multiple cycles in state-of-the art RS devices fabricated at industrial facilities is always much larger (see Figures 5f,g).[115]

Another important aspect when analyzing the endurance of RS devices is the lateral size. One should always keep in mind that achieving a very high endurance (>10^8 cycles) in RS devices with a large lateral size (>25 μm^2) does not mean that smaller (~100 nm^2) RS devices with similar composition will exhibit a similar endurance.[115] First, narrower metallic wires could easily melt if the currents in LRS are too high; and second the concentration of native defects (necessary to promote RS)[1,26,44] may be much lower in smaller devices, and if it reaches a critical value, the devices may not switch. Note that the switching voltages and state currents strongly depend on the device size, as shown in Figure 5h,i.[22] It may happen for large cells that when the filament degrades and gets stuck into a high-resistive state during the endurance test, another filament is created and takes over the cycling. This phenomenon might occur several times, and its probability to happen is much higher for large than for scaled RS devices.

Some of the most prominent researchers in the field of RS usually present values of R_{HRS} and R_{LRS} in every cycle when making endurance claims.[90,116,117] This is also the method used by the industry before trying to commercialize RS devices for different technologies, independently if they show that in papers or not (sometimes articles from companies do not disclose enough information due to confidentiality issues). Therefore, it would be much better if the entire community working on RS devices always support endurance claims by measuring R_{HRS} and R_{LRS} in every cycle (see Figure 1e,f and Figure 3c,d). To provide the readers with a practical summary of the endurances of RS devices, in Table 2 we have summarize all the studies that we found in the literature claiming an endurance >10^5 cycles and indicate the number of data points presented.[172−174]

CONCLUSION

The cycling endurance of RS devices has been mainly characterized using two different methods. The first one consists of stressing the devices and measuring the values of R_{HRS} and R_{LRS} after every set/reset transition; this method is highly reliable and should always be employed, at least for the first 10^6−10^7 cycles. The second one consists of stressing the devices without measuring R_{HRS} and R_{LRS} and stopping the stress after some cycles to read the values of R_{HRS} and R_{LRS}; this method is not recommended because it cannot confirm the switching of the device in every cycle, it introduces delays affecting the RS properties, it underestimates cycle-to-cycle variability of switching voltages and state currents, and it also overestimates the endurance lifetime. Table 2 presents a summary of the highest endurances ever claimed for RS devices and the number of data points presented in those studies. In our opinion, authors of studies in the field of RS reporting endurance plots should always describe in detail their measuring protocol, specifically indicating if they read R_{HRS} and R_{LRS} in each cycle and how many data points they are displaying. Clear communication of these critical experimental details will help readers to understand the real cycling endurance of the RS devices developed in each study and should accelerate the commercialization of RS technologies.

AUTHOR INFORMATION

Corresponding Author

Mario Lanza − *Physical Science and Engineering Division, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia;* orcid.org/0000-0003-4756-8632; Email: mario.lanza@kaust.edu.sa

Authors

Rainer Waser − *Peter-Grünberg-Institut (PGI-7), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany; Peter-Grünberg-Institut (PGI-10), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany; Institut für Werkstoffe der Elektrotechnik 2 (IWE2), RWTH Aachen University, Aachen 52074, Germany*

Daniele Ielmini − *Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano and IU.NET, Milano 20133, Italy*

J. Joshua Yang − *Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, California 90089, United States*

Ludovic Goux − *Imec, 3001 Leuven, Belgium*

Jordi Suñe − *Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Barcelona 08193, Spain*

Anthony Joseph Kenyon − *Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, United Kingdom*

Adnan Mehonic − *Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, United Kingdom*

Sabina Spiga − *CNR-IMM, Unit of Agrate Brianza, Agrate Brianza (MB) 20864, Italy;* orcid.org/0000-0001-7293-7503

Vikas Rana − *Peter-Grünberg-Institut (PGI-10), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany*

Stefan Wiefels − *Peter-Grünberg-Institut (PGI-7), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany*

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Stephan Menzel − *Peter-Grünberg-Institut (PGI-7), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany;* orcid.org/0000-0002-4258-2673
Ilia Valov − *Peter-Grünberg-Institut (PGI-7), Forschungszentrum Jülich GmbH, 52425 Jülich, Germany;* orcid.org/0000-0002-0728-7214
Marco A. Villena − *Applied Materials Inc., Reggio Emilia 74L 42122, Italy*
Enrique Miranda − *Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Barcelona 08193, Spain*
Xu Jing − *School of Materials Science and Engineering, Jiangsu Key Laboratory of Advanced Metallic Materials, Southeast University, Nanjing 211189, China*
Francesca Campabadal − *Institut de Microelectrònica de Barcelona-Centre Nacional de Microelectrònica, Consejo Superior de Investigaciones Científicas, Bellaterra 08193, Spain*
Mireia B. Gonzalez − *Institut de Microelectrònica de Barcelona-Centre Nacional de Microelectrònica, Consejo Superior de Investigaciones Científicas, Bellaterra 08193, Spain*
Fernando Aguirre − *Unidad de Investigación y Desarrollo de las Ingenierías-CONICET, Facultad Regional Buenos Aires, Universidad Tecnológica Nacional (UIDI-CONICET/FRBA-UTN), Medrano 951(C1179AAQ), Argentina*
Felix Palumbo − *Unidad de Investigación y Desarrollo de las Ingenierías-CONICET, Facultad Regional Buenos Aires, Universidad Tecnológica Nacional (UIDI-CONICET/FRBA-UTN), Medrano 951(C1179AAQ), Argentina*
Kaichen Zhu − *Physical Science and Engineering Division, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia*
Juan Bautista Roldan − *Departamento de Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, Granada 18071, Spain*
Francesco Maria Puglisi − *Dipartimento di Ingegneria "Enzo Ferrari", Università di Modena e Reggio Emilia, Modena 41125, Italy*
Luca Larcher − *Applied Materials Inc., Reggio Emilia 74L 42122, Italy*
Tuo-Hung Hou − *Department of Electronics Engineering and Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan;* orcid.org/0000-0002-9686-7076
Themis Prodromakis − *Centre for Electronics Frontiers, University of Southampton, Southampton SO171BJ, United Kingdom*
Yuchao Yang − *Key Laboratory of Microelectronic Devices and Circuits (MOE), Department of Micro/nanoelectronics, Peking University, Beijing 100871, China;* orcid.org/0000-0003-4674-4059
Peng Huang − *Key Laboratory of Microelectronic Devices and Circuits (MOE), Department of Micro/nanoelectronics, Peking University, Beijing 100871, China;* orcid.org/0000-0003-3280-0099
Tianqing Wan − *Department of Applied Physics, The Hong Kong Polytechnic University, Kowloon, Hong Kong*
Yang Chai − *Department of Applied Physics, The Hong Kong Polytechnic University, Kowloon, Hong Kong*
Kin Leong Pey − *Engineering Product Development, Singapore University of Technology and Design (SUTD), 487372, Singapore;* orcid.org/0000-0002-0066-091X
Nagarajan Raghavan − *Engineering Product Development, Singapore University of Technology and Design (SUTD), 487372, Singapore;* orcid.org/0000-0001-6735-3108
Salvador Dueñas − *Department of Electronics, University of Valladolid, Valladolid E-47011, Spain*
Tao Wang − *Institute of Functional Nano and Soft Materials (FUNSOM), Collaborative Innovation Center of Suzhou Nano Science and Technology, Soochow University, Suzhou 215123, China*
Qiangfei Xia − *Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003-9292, United States*
Sebastian Pazos − *Physical Science and Engineering Division, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsnano.1c06980

Notes

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VOCABULARY

Resistive switching device, electronic device that can alter their electrical resistance when an electrical stress is applied. They normally have a metal/insulator/metal structure (*i.e.*, two electrodes), although some three-electrode configurations (with a third electrode adjacent to the insulator) have been proposed. The changes in the electrical resistance are normally nonvolatile, although a small portion of devices also exhibit volatile resistive switching; **memristor**, short for "memory" and "resistor", this is the fourth fundamental electronic component (together with the resistor, capacitor and inductor), and it relates electric charge and magnetic flux. The word memristor has been often employed as a synonym of resistive switching device, although one portion of the community working in this field thinks that is not correct; **nonvolatile memory (NVM)**, a type of computer memory that can store information even after power is removed. This type of memory is used to store information for long periods >10 years. The most employed NVM is the NAND Flash. Emerging NVMs are phase-change memories, resistive random-access memories, and magnetic random-access memories, among others; **switching endurance**, for devices exhibiting two stable states, endurance is defined as the maximum number of programming cycles that a device can undergo before its electrical characteristics start to deviate outside the allowed ranges, even if that happens only temporarily during one cycle. For multistate devices, there is no consensus on what endurance is, although several authors defined it as the number of transitions from the most to the least resistive states stopping at all intermediate states and back to the most resistive state; **crossbar array**, circuit containing two groups of metallic bars separated by one insulator. First, one group of parallel metallic bars is deposited on an insulating substrate, then an insulator is deposited on the bars, and finally the second group of bars (parallel to each other but perpendicular to the first group) is deposited on top. This configuration leads to multiple metal/insulator/metal cells at

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the intersections between the bars, which serve as a resistive switching device

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