# Switching Dynamics of Ag-Based Filamentary Volatile Resistive Switching Devices—Part I: Experimental Characterization

Erika Covi<sup>®</sup>, *Senior Member, IEEE*, Wei Wang, *Member, IEEE*, Yu-Hsuan Lin, Matteo Farronato, *Graduate Student Member, IEEE*, Elia Ambrosi<sup>®</sup>, and Daniele Ielmini<sup>®</sup>, *Fellow, IEEE* 

Abstract—Volatile resistive switching random access memory (RRAM) devices are drawing attention in both storage and computing applications due to their high ON-/OFF-ratio, fast switching speed, low leakage, and scalability. However, these devices are relatively new and the physical switching mechanisms are still under investigation. A thorough understanding and modeling of the physical dynamics underlying filament formation and self-dissolution are of utmost importance in view of future integration of volatile devices in neuromorphic systems and in memory arrays. To assess the physical mechanisms and develop appropriate models, though, the electrical properties of the device have to be characterized. In this article, we present an extensive study of Ag/SiOx-based volatile RRAM devices. Important parameters, such as switching time, switching voltage, and retention time are investigated as a function of the stimulation conditions. A physical explanation is provided and the applicability of the device in neuromorphic systems is discussed.

Index Terms— Electrical characterization, oxide-based resistive switching random access memory (RRAM), volatile RRAM devices.

# I. INTRODUCTION

THE fast increase of applications and devices which need to adapt and interact with the environment calls for a radical change of present computing paradigms [1], [2]. This

Manuscript received February 12, 2021; revised April 19, 2021; accepted April 21, 2021. Date of publication July 26, 2021; date of current version August 23, 2021. This work was supported in part by the Semiconductor Research Corporation under Grant 2018-IN-2814, in part by the European Union's Horizon 2020 Research and Innovation Program under Grant 824164, in part by the Ministero dell'Istruzione dell'Università e della Ricerca under Grant 2016/R164TYLBZP. The device fabrication was performed in PoliFAB, the micro- and nanofabrication facility of Politecnico di Milano. The review of this article was arranged by Editor P. Narayanan. (*Corresponding author: Daniele lelmini.*)

Erika Covi, Wei Wang, Matteo Farronato, Elia Ambrosi, and Daniele lelmini are with the Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano, 20133 Milan, Italy, and also with IU.NET, 20133 Milan, Italy (e-mail: daniele.ielmini@polimi.it).

Yu-Hsuan Lin is with the Department of Electronics Engineering, Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3076029.

Digital Object Identifier 10.1109/TED.2021.3076029

evolution of the computing scenario requires new technologies which can complement current CMOS one [3]. In this context, a key role is played by emerging memory technologies, which can find several applications as both storage and computing elements. In particular, volatile oxide-based resistive switching random access memory (RRAM) devices, also known as conductive bridge RAM (CBRAM) [4]-[6], electrochemical metallization memory (ECM) [5]-[7], programmable metallization memory (PMC) [5], [6], [8], diffusive memristor [9], and atomic switch [6], [10], have recently attracted a large interest as selectors in memory arrays and as fundamental short-term elements in neuromorphic systems. Indeed, thanks to their high ON-/OFF-ratio and steep switching slope, these devices are ideal in emerging memory arrays as an access element preventing sneak paths during normal read/write operation of the memory array [11]-[13]. However, the reported switching off times span various orders of magnitudes, from microseconds or nanoseconds [14]–[16], to several milliseconds [9], [17], [18], the latter being more compatible with biological timescales. Therefore, from a neuromorphic perspective, volatile devices are very attractive because they display tunable retention times in the range of biological timescales, i.e., hundreds of milliseconds, thus offering a valid and compact alternative to CMOS technology in the design of novel hardware which needs to operate in real time [19], [20].

Volatile RRAM devices find application in short-term memory synapses [9], [18], [19], [21], [22], where they keep trace of recent neural activity, to firing neuron, as shown by Wang *et al.* [23], who presented a fully memristive unsupervised neural network. Another interesting application of volatile devices was reported in [24] and [25], where the volatile elements are used as a reservoir in a computing system for temporal information processing and time-series prediction, as well as to solve a second-order nonlinear dynamic task.

The switching mechanism of volatile RRAM devices is based on the field-driven formation of a metallic filament (typically Ag or Cu, which are not interchangeable, since they feature different behaviors such as different compliance current ranges for volatile and non-volatile regimes [17], [26]) in the oxide and its diffusion-driven spontaneous dissolution in

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/



Fig. 1. Structure of the fabricated 1T-1R volatile device and scheme of the experimental setup.

absence of an applied field [27]–[29]. The interesting features of volatile devices demand a thorough study of their electrical properties to understand the physical mechanisms underlying the switching process and the stimulation parameters that determine the device behavior. However, such a comprehensive investigation is still missing.

In this work, we provide an extensive study of the electrical behavior of Ag/SiO<sub>x</sub>-based volatile RRAM devices. We investigate the dependence of switching time and retention time on voltage amplitude, pulse time width, and current compliance. We show that the read voltage can be also used as a tuning parameter for the retention time. The results presented in this work serve as a basis for the understanding and modeling of the physical mechanisms that are presented in the companion article [30], as well as a step toward the development of neuromorphic systems and learning algorithms with multitimescale dynamics. A preliminary report is presented in IEEE International Electron Device Meeting (IEDM 2019) [31]. Here, we extend our investigation considering a variable oxide thickness and we provide an extensive report of the device electrical behavior highlighting the differences and similarities among samples with different oxide thickness. At first, we consider the quasi-static behavior and we provide an insight into the possible phenomena occurring inside the oxide (Section III). Then, we focus on the pulsed regime, where we provide a complete overview of the parameters affecting the switching on time, the threshold voltage, and the retention time (Section VI). Finally, a Section is added in order to discuss how the features of the proposed volatile RRAM device can be exploited in neuromorphic applications (Section V).

#### II. MATERIALS AND METHODS

## A. Device Fabrication

We fabricated RRAM devices with  $Ag/SiO_x/C$ stack, as shown in Fig. 1. Each device has a onetransistor/one-resistor (1T-1R) structure, where the transistor serves as a selector for the RRAM device, as well as allowing the control of the compliance current  $I_C$ , namely the maximum current during the set transition [32]. The drain of the transistor is connected to the RRAM device via a W plug. The RRAM has a top electrode (TE) made of a Ag



Fig. 2. (a) Forming voltage  $V_F$  (blue circles) and threshold voltage  $V_T$  (red squares) as a function of the oxide thickness  $t_{ox}$ . Data are colored filled symbols, medians are symbols with white filling. Whereas  $V_F$  shows dependence on  $t_{ox}$ ,  $V_T$  is independent. (b) Schematic representation of the device in its pristine state and (c) after forming operation. Forming induces a modification of the oxide lattice, hence, the independence of  $V_T$  on  $t_{ox}$ .

layer and a switching layer made of SiO<sub>x</sub>, both deposited by e-beam evaporation without breaking the vacuum [33]. The oxide layer was deposited from a silicon monoxide source at room temperature and with a deposition rate of 0.02 nm/s, therefore, we expect x in SiO<sub>x</sub> to be close to one. The bottom electrode (BE) of the RRAM device consists of a graphitic C pillar with a base of 70 nm × 70 nm. The graphitic C BE has already been shown to be a good electrode material for both volatile and non-volatile devices thanks to its stability and inert behavior [17], [26], [32]. The TE thickness is 50 nm, whereas the SiO<sub>x</sub> thickness is 5 nm, except in Fig. 2(a), where the oxide thickness varies from 2 to 20 nm.

# B. Electrical Characterization

Forming and dc characterizations were carried out using an HP 4156C semiconductor device parameter analyzer. The pulsed characterization was carried out using a TTI TGA12104 arbitrary waveform generator providing the voltage waveform to be applied to the TE. To measure the device current, a LeCroy Waverunner 640Zi oscilloscope was connected at the BE side, and the voltage drop across a 50- $\Omega$  series resistance was probed. The experimental setup is sketched in Fig. 1.

In the following, unless otherwise noted, the following conditions apply: device oxide thickness  $t_{ox} = 5$  nm, read voltage  $V_{Read} = 100$  mV, current compliance  $I_C = 10 \ \mu$ A, and maximum set voltage pulse  $V_{p,max} = 5$  V. Since the device-to-device variability is comparable to the cycle-to-cycle one, the results shown in the following sections refer to one representative case tested for up to 100 cycles. Note that the voltages refer to the voltage applied to the TE of the device, therefore, the voltage drop across the transistor is included in the given value.

#### III. DC CHARACTERIZATION

# A. Thickness Dependent Forming and Threshold Voltage

The device is initially in its pristine state, therefore, a forming operation is required to form the Ag filament for the



Fig. 3. (a) and (d) Positive and negative experimental FV curve at different current compliance: (a) 10  $\mu$ A and (d) 100 nA. Conceptual representation of (b) and (e) initial filament size after switch on and (c) and (f) spontaneous filament retraction leading to switch off.

first time. The forming voltage ( $V_F$ ) increases with the oxide thickness, as demonstrated in Fig. 2(a), where  $V_F$  is plotted as a function of oxide thickness  $t_{ox}$ . Interestingly, the threshold voltage  $V_T$  does not show any dependence on the oxide thickness, similar to Cu-based devices [34]. A plausible explanation is that whereas in the pristine state the oxide film is uniform [Fig. 2(b)], after forming, the Ag ions generate a preferential path in the oxide [Fig. 2(c)] altering its original atomic configuration. Therefore, the field required to induce the ion migration does not depend on the oxide thickness anymore.

# B. Bidirectional Switching

After forming, the device is ready to be operated in its normal working regime. Fig. 3(a) and (b) show the I-Vcharacteristic of the device at different current compliance ( $I_C$ ) of  $I_C = 10 \ \mu$ A and  $I_C = 100 \ n$ A, respectively. The modulation of  $I_C$  during positive sweeps is done through controlling the transistor gate voltage, whereas during negative sweeps  $I_C$  is set by the instrument. The device shows bidirectional switching, which can be ascribed to a residual Ag stub remaining on the BE after forming operation. During a voltage sweep, the device is initially in its high resistive state (HRS). When the applied voltage is above  $V_T$ , the formation of the conductive filament induces the transition to the low resistive state (LRS). The filament, however, is not stable and tends to self-dissolve when the applied voltage is below a critical voltage referred to as hold voltage  $V_H$ .

The ON-current in LRS can be as high as  $10^{-5}$  A and the OFF-current in HRS can be as low as  $10^{-13}$  A, resulting in an ON-/OFF-ratio of  $10^7$ . This promising feature enables the



Fig. 4. Measured retention time as a function of oxide thickness. Blue circles are the experimental data and white squares with blue border indicate the median value. Error bars indicate the standard deviation.

device application as a selector for a large memory array in crossbar structure.

# *C.* Effects of the Compliance Current in the Device Characteristic

From Fig. 3, the switching off can be partitioned into two stages: 1) abrupt current drop after the applied voltage decreases below the hold voltage, followed by 2) gradual decrease after the abrupt drop at  $V < V_H$  [Fig. 3(a)]. This can be explained by the filament dissolution process due to the diameter decrease at the initial stage and subsequent filament stub retraction after the break. The filament shape evolution in Fig. 3(b), (c), (e), and (f) is simulated assuming surface tension induced surface atom diffusion as reported in our previous work [29]. When the compliance current is smaller than a critical value, for instance,  $I_C = 100$  nA as shown in Fig. 3(d), the first stage of the abrupt current drop is missing, resulting in a smaller hold voltage. However, the current level of the gradually decreasing phase is higher than that in the higher compliance current situation [Fig. 3(a)].

A possible physical explanation is illustrated in Fig. 3, where a mere graphical representation of what may occur during the filament rupture, depending on the filament size, is sketched. Since the size of the Ag filament depends on  $I_C$  [31], [35], higher  $I_C$  determines the formation of a thicker filament [Fig. 3(b)]. In the case of the high compliance current, upon removal of any voltage applied to the device, the filament starts retracting into two stubs, one from TE and the other from BE [Fig. 3(c)]. In the case of  $I_C = 100$  nA, the filament has a smaller diameter [Fig. 3(e)]. Therefore, when the spontaneous dissolution occurs, due to the ovulation effect of the surface tension-driven filament shape evolution, as also directly observed in similar oxide-Ag structures [9], [36], some Ag clusters would be formed in the oxide layer [Fig. 3(f)]. In this new configuration, the conductance is comparable to the ultrathin filament. The final relaxation of the device and conductance decrease is due to the Ostwald ripening effect of the Ag cluster to the electrode [9], [37]. As a result, the apparent holding voltage becomes lower, thus decreasing the volatility of the device.

#### **IV. AC CHARACTERIZATION**

For practical use of this device, apart from the switching parameters, the understanding of the switching dynamics is



Fig. 5. Time resolved technique to estimate switching time  $t_{set}$ : applied rectangular voltage pulse  $V_{\rho}$  (blue) and relative current trace (red).



Fig. 6. Distribution of  $t_{set}$  for increasing  $V_{\rho}$ .

also essential. Indeed, both switching and spontaneous relaxation dynamics need to be characterized in view of device use in temporal-related applications.

At first, the retention time of all the samples was tested by applying to all semitriangular pulses of 100  $\mu$ s time width and reading their retention time. Fig. 4 shows the recorded retention times (circles) and median value (squares) for all the oxide thicknesses. The results demonstrate that there is neither a significant difference in the distribution of the retention times nor a dependence of the retention time on the oxide thickness. Therefore, in the following, the sample with 5 nm oxide thickness is chosen as a representative case.

#### A. Switching Time as a Function of the Pulse Amplitude

Initially, the set dynamics were analyzed. In this respect, our investigation complements the previous studies on Agand Cu-based non-volatile devices [38]–[42]. Fig. 5 shows the rectangular programming pulses (voltage amplitude  $V_P$ ) applied to the devices and the current flowing across the device during stimulation. We define  $t_{set}$  as the time between the beginning of the programming pulse and the device switching on.

Fig. 6 shows the distribution of  $t_{set}$  when stimulated by pulses with increasing  $V_p$ . Log-normal distribution of the switching on time is observed, evidencing the field-induced ionic transport barrier lowering effect. In fact, assuming a normal distribution of the energy barrier for the ionic transport will result in a log-normal distribution of the ionic transport velocity and switching speed according to the general Arrhenius law [43]. Due to the field-driven origin of filament growth,  $t_{set}$  is very sensitive to  $V_p$ . Indeed, an increase of 20% in  $V_p$  results in a decrease in  $t_{set}$  by one order of magnitude, thus further confirming an exponential-like relationship between switching time and programming voltage. Moreover, other processes concur in the set time, namely the nucleation of Ag nanoparticles, the Ag ion migration inside the host material, and the oxidation–reduction reaction at the Ag-SiO<sub>x</sub> interface [39], [40].

# B. Impact of the Ramp Rate on Threshold Voltage

We also investigated the device switching-on process with half triangular pulses, to provide more information about the switching dynamics of the device. In particular, the dependence of switching voltage  $V_T$  on the ramp rate, defined as  $V_m/t_p$ , where  $V_m$  is the maximum value and  $t_p$  is the width of the half-triangular pulse, can be obtained. Fig. 7(a) shows the time-resolved technique to monitor the switching voltage and the retention time of the volatile device. The device is characterized by the application of 6 V pulses at different  $t_p$  and its state after the pulse is monitored by a small read voltage. In Fig. 7(b),  $V_T$  is plotted as a function of pulse ramp rate. The threshold voltage is higher than the DC threshold voltage. Indeed, from Fig. 7(b), an increase by five orders of magnitude in the ramp rate causes an increase of less than a factor of two in  $V_T$ . Fig. 7(c) shows the distributions of  $V_T$  obtained with increasing ramp rates. The distributions are quite steep, confirming that there is a tradeoff between the pulse time width and the minimum voltage needed to induce the device switching process [30].

# C. Current Compliance Modulated Retention Time

The filament size controls the retention time [35] and can be determined by the maximum current flow through the device [31]. Therefore, we studied the retention time  $(t_R)$ as a function of the device current compliance, which was changed by varying the gate voltage of the transistor in our 1T-1R structure. Fig. 8(a) shows the  $t_R$  distribution. Data indicate a log-normal distribution of  $t_R$  with relatively large deviation. Note the strong impact of the compliance current, where an increase by a factor 7 in  $I_C$  results in an increase by 100 in retention time. This is confirmed by Fig. 8(b), showing the measured retention time  $t_R$  as a function of  $I_C$ : within a relatively large statistical spread, the retention time significantly increases as  $I_C$  increases from 9  $\mu$ A to 65  $\mu$ A.

The filament formation is a stochastic process, therefore, the filament size and microscopical configuration can slightly vary even while keeping the same  $I_C$ . Macroscopically, this stochasticity can be associated with a fluctuation of the average value of retention current  $I_{ret}$ , defined according to the Ohm's law as the product of the reading voltage and the device conductance. The value of  $I_{ret}$  is an important indicator of the expected  $t_R$ . Fig. 8(c) shows the median  $t_R$  as a function of  $I_{ret}$ , where each data-point is calculated in a neighborhood of  $\Delta I_{ret} = 3 \ \mu A$ . The data refer to different sample thicknesses. It can be noted that there is a strong correlation between  $t_R$  and  $I_{ret}$  and this correlation is independent of the oxide thickness. We can therefore, conclude that the section of the filament, i.e., its initial diameter, is dominant in determining  $t_R$ . More



Fig. 7. (a) Time resolved technique to estimate the threshold voltage  $V_T$ . The blue trace is the applied pulse, whereas the red trace is the sensed current. (b) Dependence of  $V_T$  on the ramp rate defined as maximum pulse voltage divided by pulse width. (c) Distribution of  $V_T$  with different pulsewidths.



Fig. 8. (a) Distribution of  $t_R$  for different  $I_C$ . (b) Dependence of  $t_R$  on  $I_C$ : the current compliance determines the filament size, hence, the median  $t_R$ . To obtain different current compliance, the gate voltage of the transistor was varied between 1 and 1.5 V, with 50 mV step. (c) Dependence of  $t_R$  on  $I_{ret}$  for different oxide thicknesses. Each data-point is the median retention time of the data lying in a  $I_{ret}$  neighborhood of  $\Delta I_{ret} = 3 \mu A$ .

specifically, longer  $t_R$  are associated with higher  $I_{ret}$ , which in turn are related to larger filament diameter.

## D. Reading Voltage Modulated Retention Time

After the device switches to the ON-state, the voltage needed to prevent filament dissolution, i.e., the hold voltage, is lower than  $V_T$  as already shown in Fig. 3. Therefore, we can predict that a read voltage ( $V_{\text{Read}}$ ) lower but close to the hold voltage can be used not only to monitor the state of the filament, but also to modulate  $t_R$ , as shown in Fig. 9(a). Here, we demonstrate that  $V_{\text{Read}}$  amplitude indeed has an effect on  $t_R$  because it contrasts the diffusion phenomenon which is responsible for filament dissolution. The applied  $V_{\text{Read}}$  does not prevent the device from switching off, provided that  $V_{\text{Read}} < V_{H,\text{DC}}$ , as shown in the distributions in Fig. 9(b). Retention time exceeding the monitoring time limit is also observed when the read voltage approaches the hold voltage ( $V_{\text{Read}} \approx V_{H,\text{DC}}$ ).

#### V. DISCUSSION

Recently, volatile devices have attracted increasing interest for a variety of applications which range from selectors in memory arrays to volatile elements in neuromorphic computing systems. The target performance of the devices, though, is closely dependent on the application. Indeed, in memory applications, volatile devices have to feature high nonlinearity, high ON-/OFF-ratio, fast switching but also short retention time. In neuromorphic applications, where the retention of the device is proposed to mimic short-term memory effects, requirements on retention time are the opposite, and times in the order of tens of microseconds up to milliseconds or even seconds are desired. The proposed volatile device shows performance that is suitable for the latter application. Indeed, Fig. 8 demonstrates that the device has retention times in line with the requirements for neuromorphic applications.

The possibility of tuning the retention time with electrical parameters, e.g., current compliance, enhances the flexibility of the system, which can be used at different timescales without the need for redesign part of the CMOS circuits. Furthermore, the cycle-to-cycle variability of the retention time is an additional advantage in learning systems, which can be exploited to change the learning rate of the network. As an example, in classical spike-timing-dependent-plasticity (STDP), the timing between two spikes determines the magnitude and direction of the weight update [9]. If the proposed devices are used to store the eligibility trace of the neural activity, the weight update occurs with a probability p that depends on the retention time of the volatile device. As a result, the learning and forgetting processes are slowed down, with consequent beneficial effects on the network memory capacity. In this context, it is of utmost importance to consider when and how the device should be read. The retention time is a hidden variable of the system, which does not need continuous monitoring. On the contrary, as evidenced in Fig. 9(a), the read condition might influence the retention





Fig. 9. (a) Demonstration of the controllability of  $t_R$  with reading voltage  $V_{\text{Read.}}$  (b) Distribution of  $t_R$  with different  $V_{\text{Read.}}$ 

time. Therefore, in neuromorphic systems, the best practice is to read the device only when strictly necessary, using pulses ideally  $\leq 100 \text{ mV}$  and for a minimum read time to minimize possible read disturbs.

The intrinsic stochastic behavior of the volatile RRAM can be exploited to generate noise in neural networks [44], which has been proven beneficial for the performance of the network itself, as well as a mechanism already present in and used by the human brain [45], [46]. In these networks, the possibility to tune the stochasticity of the device, to a certain extent, increases the device attractiveness, since the dynamics can be changed through the selection of proper electrical stimuli without the need for designing extra control circuits. In our case, as an example, the switching probability of the device can be tuned by changing either the time width of the programming pulse or its amplitude. The existence of stochasticity is observed in many device parameters, for instance, the switching time, threshold voltage, and retention time. We can therefore, associate the y-axis of Figs. 6 and 7(c)to the switching probability for our device given a combination of  $t_p$  and  $V_p$ .

# **VI. CONCLUSION**

In this work, we presented an Ag-based volatile RRAM device. The device was characterized under different stimulation conditions and the electrical parameters which can be used to tune the device behavior have been identified and quantified. This characterization is essential to understand the physical switching dynamics underlying device behavior and provide some guidelines to include volatile devices in more complex systems for either memory or neuromorphic applications.

#### REFERENCES

- W. Maass, "Networks of spiking neurons: The third generation of neural network models," *Neural Netw.*, vol. 10, no. 9, pp. 1659–1671, 1997, doi: 10.1016/S0893-6080(97)00011-7.
- [2] A. R. Young, M. E. Dean, J. S. Plank, and G. S. Rose, "A review of spiking neuromorphic hardware communication systems," *IEEE Access*, vol. 7, pp. 135606–135620, 2019, doi: 10.1109/ACCESS.2019.2941772.
- [3] M. Payvand, M. V. Nair, L. K. Müller, and G. Indiveri, "A neuromorphic systems approach to in-memory computing with non-ideal memristive devices: From mitigation to exploitation," *Faraday Discuss.*, vol. 213, pp. 487–510, 2019, doi: 10.1039/C8FD00114F.
- [4] M. Kund *et al.*, "Conductive bridging RAM (CBRAM): An emerging non-volatile memory technology scalable to sub 20nm," in *IEDM Tech. Dig.*, Dec. 2005, pp. 754–757, doi: 10.1109/IEDM.2005.1609463.
- [5] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, nos. 25–26, pp. 2632–2663, Jul. 2009, doi: 10.1002/ adma.200900375.
- [6] I. Valov and M. N. Kozicki, "Cation-based resistance change memory," J. Phys. D, Appl. Phys., vol. 46, no. 7, Feb. 2013, Art. no. 074005, doi: 10.1088/0022-3727/46/7/074005.
- [7] M. Lübben and I. Valov, "Active electrode redox reactions and device behavior in ECM type resistive switching memories," *Adv. Electron. Mater.*, vol. 5, no. 9, Sep. 2019, Art. no. 1800933, doi: 10.1002/aelm. 201800933.
- [8] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Self-accelerated thermal dissolution model for reset programming in unipolar resistiveswitching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 193–200, Feb. 2009, doi: 10.1109/TED.2008.2010584.
- [9] Z. Wang et al., "Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing," *Nature Mater.*, vol. 16, no. 1, pp. 101–108, Jan. 2017, doi: 10.1038/nmat4756.
- [10] M. Aono and T. Hasegawa, "The atomic switch," *Proc. IEEE*, vol. 98, no. 12, pp. 2228–2236, Dec. 2010, doi: 10.1109/JPROC.2010.2061830.
- [11] S. Hyun Jo, T. Kumar, S. Narayanan, W. D. Lu, and H. Nazarian, "3D-stackable crossbar resistive memory based on field assisted superlinear threshold (FAST) selector," in *IEDM Tech. Dig.*, Dec. 2014, pp. 6.7.1–6.7.4, doi: 10.1109/IEDM.2014.7046999.
- [12] R. Midya *et al.*, "Anatomy of Ag/Hafnia-based selectors with 10<sup>10</sup> nonlinearity," *Adv. Mater.*, vol. 29, no. 12, Mar. 2017, Art. no. 1604457, doi: 10.1002/adma.201604457.
- [13] M. Wang *et al.*, "Enhancing the matrix addressing of flexible sensory arrays by a highly nonlinear threshold switch," *Adv. Mater.*, vol. 30, no. 33, Aug. 2018, Art. no. 1802516, doi: 10.1002/adma.201802516.
- [14] S. H. Jo, T. Kumar, S. Narayanan, and H. Nazarian, "Cross-point resistive RAM based on field-assisted superlinear threshold selector," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3477–3481, Nov. 2015, doi: 10.1109/TED.2015.2426717.
- [15] H. Yang *et al.*, "Threshold switching selector and 1S1R integration development for 3D cross-point STT-MRAM," in *IEDM Tech. Dig.*, Dec. 2017, p. 38, doi: 10.1109/IEDM.2017.8268513.
- [16] P. Bousoulas *et al.*, "Investigating the origins of ultra-short relaxation times of silver filaments in forming-free SiO<sub>2</sub>-based conductive bridge memristors," *Nanotechnology*, vol. 31, no. 45, Aug. 2020, Art. no. 454002, doi: 10.1088/1361-6528/aba3a1.
- [17] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "Resistive switching device technology based on silicon oxide for improved on-off ratio—Part II: Select devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 122–128, Jan. 2018, doi: 10.1109/TED.2017.2776085.
- [18] W. Wang, A. Bricalli, M. Laudato, E. Ambrosi, E. Covi, and D. Ielmini, "Physics-based modeling of volatile resistive switching memory (RRAM) for crosspoint selector and neuromorphic computing," in *IEDM Tech. Dig.*, Dec. 2018, p. 40, doi: 10.1109/IEDM.2018.8614556.
- [19] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, "Short-term plasticity and long-term potentiation mimicked in single inorganic synapses," *Nature Mater.*, vol. 10, no. 8, pp. 591–595, Aug. 2011, doi: 10.1038/nmat3054.
- [20] G. Indiveri and S.-C. Liu, "Memory and information processing in neuromorphic systems," *Proc. IEEE*, vol. 103, no. 8, pp. 1379–1397, Aug. 2015, doi: 10.1109/JPROC.2015.2444094.
- [21] X. Zhang *et al.*, "Emulating short-term and long-term plasticity of biosynapse based on Cu/a-Si/Pt memristor," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1208–1211, Sep. 2017, doi: 10.1109/LED.2017. 2722463.

- [22] W. Wang et al., "Volatile resistive switching memory based on Ag ion drift/diffusion—Part II: Compact modeling," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3802–3808, Sep. 2019, doi: 10.1109/ TED.2019.2928888.
- [23] Z. Wang *et al.*, "Fully memristive neural networks for pattern classification with unsupervised learning," *Nature Electron.*, vol. 1, no. 2, pp. 137–145, Feb. 2018, doi: 10.1038/s41928-018-0023-2.
- [24] C. Du, F. Cai, M. A. Zidan, W. Ma, S. H. Lee, and W. D. Lu, "Reservoir computing using dynamic memristors for temporal information processing," *Nature Commun.*, vol. 8, no. 1, p. 2204, Dec. 2017, doi: 10.1038/s41467-017-02337-y.
- [25] J. Moon *et al.*, "Temporal data classification and forecasting using a memristor-based reservoir computing system," *Nature Electron.*, vol. 2, no. 10, pp. 480–487, Oct. 2019, doi: 10.1038/s41928-019-0313-3.
- [26] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "SiO<sub>x</sub>-based resistive switching memory (RRAM) for crossbar storage/select elements with high on/off ratio," in *IEDM Tech. Dig.*, Dec. 2016, pp. 4.3.1–4.3.4, doi: 10.1109/IEDM.2016.7838344.
- [27] J. van den Hurk, E. Linn, H. Zhang, R. Waser, and I. Valov, "Volatile resistance states in electrochemical metallization cells enabling nondestructive readout of complementary resistive switches," *Nanotechnology*, vol. 25, no. 42, Sep. 2014, Art. no. 425202, doi: 10.1088/0957-4484/25/42/425202.
- [28] W. Chen, H. J. Barnaby, and M. N. Kozicki, "Volatile and nonvolatile switching in Cu-SiO<sub>2</sub> Programmable metallization cells," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 580–583, May 2016, doi: 10.1109/LED.2016.2540361.
- [29] W. Wang *et al.*, "Surface diffusion-limited lifetime of silver and copper nanofilaments in resistive switching devices," *Nature Commun.*, vol. 10, no. 1, p. 81, Jan. 2019, doi: 10.1038/s41467-018-07979-0.
- [30] W. Wang et al., "Switching dynamics of Ag-based filamentary volatile resistive switching devices—Part II: Mechanism and modeling," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4342–4349, Sep. 2021.
- [31] W. Wang, E. Covi, Y.-H. Lin, E. Ambrosi, and D. Ielmini, "Modeling of switching speed and retention time in volatile resistive switching memory by ionic drift and diffusion," in *IEDM Tech. Dig.*, Dec. 2019, p. 32, doi: 10.1109/IEDM19573.2019.8993625.
- [32] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "Resistive switching device technology based on silicon oxide for improved on-off ratio—Part I: Memory devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 115–121, Jan. 2018, doi: 10.1109/ TED.2017.2777986.
- [33] J. Song, J. Woo, A. Prakash, D. Lee, and H. Hwang, "Threshold selector with high selectivity and steep slope for cross-point memory array," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 681–683, Jul. 2015, doi: 10.1109/LED.2015.2430332.

- [34] C. Schindler, G. Staikov, and R. Waser, "Electrode kinetics of Cu–SiO<sub>2</sub>based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories," *Appl. Phys. Lett.*, vol. 94, no. 7, Feb. 2009, Art. no. 072109, doi: 10.1063/1.3077310.
- [35] W. Wang *et al.*, "Volatile resistive switching memory based on ag ion drift/diffusion—Part I: Numerical modeling," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3795–3801, Sep. 2019, doi: 10.1109/ TED.2019.2928890.
- [36] C.-P. Hsiung *et al.*, "Formation and instability of silver nanofilament in Ag-based programmable metallization cells," ACS Nano, vol. 4, no. 9, pp. 5414–5420, Sep. 2010, doi: 10.1021/nn1010667.
- [37] A. Simo, J. Polte, N. Pfänder, U. Vainio, F. Emmerling, and K. Rademann, "Formation mechanism of silver nanoparticles stabilized in glassy matrices," *J. Amer. Chem. Soc.*, vol. 134, no. 45, pp. 18824–18833, Nov. 2012, doi: 10.1021/ja309034n.
- [38] J. R. Jameson *et al.*, "One-dimensional model of the programming kinetics of conductive-bridge memory cells," *Appl. Phys. Lett.*, vol. 99, no. 6, Aug. 2011, Art. no. 063506, doi: 10.1063/1.3623485.
- [39] S. Menzel, S. Tappertzhofen, R. Waser, and I. Valov, "Switching kinetics of electrochemical metallization memory cells," *Phys. Chem. Chem. Phys.*, vol. 15, no. 18, pp. 6945–6952, 2013, doi: 10.1039/C3CP50738F.
- [40] S. Menzel, U. Böttger, M. Wimmer, and M. Salinga, "Physics of the switching kinetics in resistive memories," *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6306–6325, Oct. 2015, doi: 10.1002/adfm.201500825.
- [41] W. Chen, S. Tappertzhofen, H. J. Barnaby, and M. N. Kozicki, "Sio<sub>2</sub> based conductive bridging random access memory," *J. Electroceram.*, vol. 39, nos. 1–4, pp. 109–131, 2017, doi: 10.1007/s10832-017-.0070-5.
- [42] A. Nayak, T. Tsuruoka, K. Terabe, T. Hasegawa, and M. Aono, "Switching kinetics of a Cu<sub>2</sub>S-based gap-type atomic switch," *Nanotechnol*ogy, vol. 22, no. 23, Apr. 2011, Art. no. 235201, doi: 10.1088/0957-4484/22/23/235201.
- [43] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, no. 5, Sep. 2007, Art. no. 054517, doi: 10.1063/ 1.2773688.
- [44] P. Wijesinghe, A. Ankit, A. Sengupta, and K. Roy, "An all-memristor deep spiking neural computing system: A step toward realizing the lowpower stochastic brain," *IEEE Trans. Emerg. Topics Comput. Intell.*, vol. 2, no. 5, pp. 345–358, Oct. 2018, doi: 10.1109/TETCI.2018. 2829924.
- [45] G. Basalyga and E. Salinas, "When response variability increases neural network robustness to synaptic noise," *Neural Comput.*, vol. 18, no. 6, pp. 1349–1379, Jun. 2006, doi: 10.1162/neco.2006.18.6.1349.
- [46] W. Maass, "Noise as a resource for computation and learning in networks of spiking neurons," *Proc. IEEE*, vol. 102, no. 5, pp. 860–880, May 2014, doi: 10.1109/JPROC.2014.2310593.