



Design issues and performance analysis of CCM boost converters with RHP zero mitigation via inductor current sensing

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Abstract

The right-half plane (RHP) zero in the control to output voltage transfer function of a boost converter operating in the continuous conduction mode limits the loop bandwidth. By injecting a scaled version of the inductor current into the loop, it is possible to shift the zero from the right-half plane to the left-half plane, which leads to increased stability of the control loop. This solution generates a static voltage error at the output of the converter (tracking error), which may be unacceptable in practical applications. A few strategies to mitigate or correct this tracking error have been suggested. However, they have never been fully assessed. This paper thoroughly investigates the impact of the RHP zero mitigation technique on the dynamic performance of a boost converter, and identifies the complex trade-off between the system stability, transient response, and tracking error correction capability. Based on these findings, design guidelines are provided to help maximize system performance. A representative case study is considered to highlight the performance benefits and simulation results are presented to validate the analysis.

Keywords Boost converter · Right-half-plane zero · Transient response · Dynamic performance · Tracking error

1 Introduction

Handheld devices with large LED displays require one or more high-efficiency step-up DC–DC converters occupying small footprints and being able to handle large instant line and load variations without impairing image quality. Step-up converters working in the continuous conduction mode (CCM) suffer from the presence of a right half plane (RHP) zero, which constrains the closed-loop bandwidth of the converter, which affects the speed of the transient response. This zero, which is inherently present in the control-to-output transfer function, usually limits the maximum bandwidth to a fraction of the frequency of the RHP zero. A typical solution is to force the converter to operate in the discontinuous conduction mode (DCM). In this mode of operation, the RHP zero is shifted to a much higher frequency, which increases the phase margin for a given bandwidth [1]. Unfortunately, this advantage comes at the price of a large inductor current ripple, which results in higher device

stress, lower efficiency, and potential magnetic core saturation. Numerous papers have been devoted to the RHP zero problem [2–16]. In [3–8], the unwanted zero is either moved to a higher frequency or eliminated by modifying the power stage topology. These solutions, despite providing excellent dynamic behavior, require an extra power MOS switch or an extra inductance, which makes them unsuitable for integrated low-power converters where minimum circuit footprint is required. Ripple-based control, such as that proposed in [9, 10], guarantees an inherently stable loop and can provide fast line and load transient responses. In [11], the duty cycle of a converter is kept fixed during a transition to compensate for the effect of the RHP zero. However, the major drawback of these techniques is that the switching frequency of the converter is not fixed. Instead, it depends on the circuit operating conditions. The authors of [12–15] introduced techniques to solve the RHP zero problem by acting on the loop compensator. However, either the area of the compensator is largely increased or the power efficiency of the converter is decreased since they require sophisticated computational algorithms or analog-to-digital converters with a high sampling rate.

Among the various methods to mitigate issues related to the RHP zero, an interesting approach has been recently

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presented by Paduvali et al. [16]. The method exploits the left-hand plane (LHP) zero present in the transfer function from the control to the inductor current flowing in the high-side power MOS. The authors demonstrate that by summing a voltage proportional to the scaled inductor current and the output voltage, as shown in Fig. 1, the RHP zero of the system is moved either to an infinite frequency (perfect cancellation) or to the LHP. By setting the value of the transimpedance R_T applied to the inductor current, it is possible to change the frequency of the zero in the control-to-output transfer function, which leads to increased stability of the control loop. The advantage of this compensation method is that it adds little additional hardware on the power stage while requiring no modifications to the standard (voltage-mode) compensation network. On the downside, the technique proposed in [16] results in a static voltage error at the output of the converter (tracking error). A few strategies have been suggested to mitigate or correct this tracking error. However, they have never been fully assessed. In this paper, the impact of the RHP zero shifting technique on the dynamic performance of a boost converter is thoroughly investigated, identifying the complex trade-off between system stability, transient response and tracking error correction capability. The aim of the paper is to provide design guidelines that help maximize system performance. In order to highlight the performance benefits, a step-up converter powering a large LED screen of a portable device has been considered as a representative case-study.

The input voltage V_{in} of the converter from a standard Li-ion cells typically ranges from 2 to 4.5 V. The output voltage V_{out} is 5 V, and the load current I_{load} ranges from 0 to $I_{load,max} = 800$ mA. In such applications, where the footprint is one of the main constraints, the converter is usually fully integrated except for the second-order LC filter. To minimize the footprints of the external inductor and capacitor, a relatively large switching frequency is typically chosen. In this

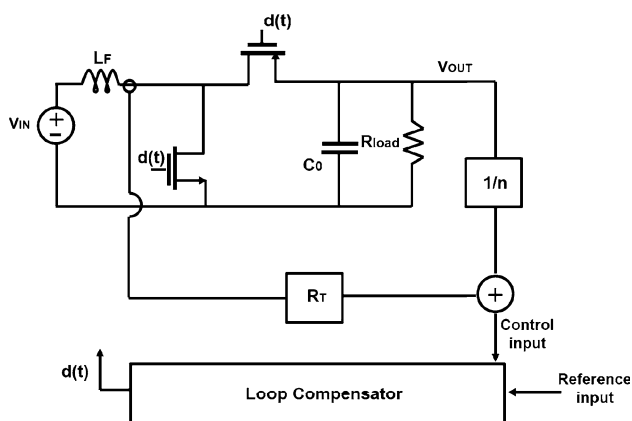


Fig. 1 Simplified schematic block of a boost converter with inductor-information-based RHP elimination

study, a switching frequency f_{sw} of 1.5 MHz, an inductance L of 2.2 mH, and a capacitance C of 44 μ F are assumed.

This paper is organized as follows. Section 2 is devoted to an explanation of the RHP zero mitigation technique. In Sect. 3, the bandwidth and phase margin variations across the input voltage and the load current ranges of a practical case study are analyzed. In addition, a comparison is made of three different design criteria. Section 4 discusses the tracking error and provides guidelines for designing a simple tracking error correction network. Section 5 analyses the impact of RHP zero mitigation and tracking error correction techniques on the transient performance of a converter. Section 6 presents simulation results that validate the presented analysis. Finally, conclusions are drawn in Sect. 7.

2 RHP zero mitigation

To obtain a stable boost converter, a proportional-integral-derivative (PID) compensator is typically implemented. It provides a DC pole, two zeroes, and two high-frequency poles. The zeroes are used to compensate for the poles of the output filter. Meanwhile, the two high-frequency poles are used to cancel the zero introduced by the capacitance ESR and to reduce the ripple at the switching frequency. These poles are not accounted for in the following analysis since their impact on stability and transient response is negligible. Under this assumption, the loop gain transfer function of the boost converter with a type-III compensator is written as follows:

$$G_L(s) = G_0 \frac{(1 + s\tau_{z1}) \times (1 + s\tau_{zh}) \times (1 + s\tau_{z,rhp})}{s(\alpha s^2 + \beta s + 1)}, \quad (1)$$

where:

τ_{z1} and τ_{zh} are the time constants of the low-frequency and high-frequency zero of the compensation network.

$\tau_{z,rhp}$ is the time constant of the RHP zero.

The term $s(\alpha s^2 + \beta s + 1)$ accounts for the poles of the LC filter.

Neglecting the capacitance ESR, the RHP frequency becomes:

$$\omega_{z,rhp} = \frac{R_{load} \times D'^2}{L} = \frac{V_{in}^2}{LV_{out}I_{load}}, \quad (2)$$

where $R_{load} = V_{out}/I_{load}$ is the load impedance, and $D' = 1 - D = V_{in}/V_{out}$. In battery-powered applications, the input voltage V_{in} , as well as the load current I_{load} , vary across a relatively wide range. As a result, the RHP zero frequency, which is a function of those two parameters,

is variable along with the ranges of V_{in} and I_{load} . The loop stability has to be guaranteed under the limiting condition when the RHP zero is at its minimum frequency. This occurs for the minimum values of R_{load} and D' , or, in other terms, for the minimum V_{in} and the maximum I_{load} . Employing the RHP zero mitigation technique proposed in [16], whose diagram is schematically represented in Fig. 1, the expression of the zero frequency in (2) becomes:

$$\omega_{z,rhp} = \frac{D'}{R_{load}D' - nR_T C}, \quad (3)$$

where n is the attenuation factor with which the boost output voltage is applied to the compensator input. The negative term at the denominator of (3) is directly proportional to the transimpedance R_T , and is responsible for the shifting of the RHP zero. This shift is exploited to widen the loop bandwidth with respect to the previous case. In particular, when the condition $R_T > \frac{L}{nCR_{load}D'}$ is met, $\omega_{z,rhp}$ becomes negative, which means the zero is brought to the LHP. However, in practice, stability has to be assured over all the possible working conditions. Since $nR_T C$ is fixed, while $\frac{L}{R_{load}D'}$ depends on the input to output voltage ratio and the load current, R_T should be chosen large enough to move the zero to the LHP even in the worst possible case. As a result, the frequency of the resulting LHP zero is dependent on D' . The natural frequency of the complex poles $\omega_0 = \frac{D'}{\sqrt{LC}}$ is also proportional to D' . Thus, it can be concluded that, following this approach, the LHP zero tracks the complex pole pair at least to the first order, and the control system can be reduced from a type-III PID to a simple type-II proportional-integral (PI) controller.

3 Stability analysis

In this section, the performance of the RHP zero-mitigation technique is assessed in a practical case, where stability has to be guaranteed across the entire range of input voltages and load currents. Considering this specific case study, the minimum frequency of the RHP zero from (2) is at $f_{z,rhp} = \omega_{z,rhp}/(2\pi) = 72.3$ kHz. To guarantee a sufficient loop phase margin with a type-III compensator, the bandwidth is limited to about $f_{z,rhp}/5$, i.e. 14 kHz, which is significantly lower than the switching frequency. Using the RHP mitigation technique in [16], some degrees of freedom exist in the positioning of the singularities. Thus, three different strategies are studied and their performances are compared.

A. R_T is chosen to cancel the RHP zero, i.e. to shift it to an infinite frequency.

- B. R_T is chosen to move the RHP zero to the LHP at an angular frequency equal to $1/\tau_{zh}$, and the controller is reduced to a type-II PI.
- C. R_T is chosen to move the RHP zero to the LHP at an angular frequency equal to $1/\tau_{zl}$, and the controller is reduced to a type-II PI.

For a fair comparison, the zeroes are placed at the same frequencies, $f_{zl} = 5$ kHz and $f_{zh} = 25$ kHz, in the three cases, (A), (B) and (C). By eliminating the RHP zero, the loop bandwidth is no longer restrained. However, it cannot exceed about one tenth of the switching frequency f_{sw} to ensure the validity of the linear continuous-time model. Thus, in the three cases, the bandwidth is kept below about 150 kHz, under all working conditions.

3.1 Stability in case (A)

To remove the RHP zero or in other words to move it to infinity, it is imposed that the denominator in (3) is null. Assuming a voltage attenuation factor of $n = 5$, the required transimpedance value is $R_T = 4$ m Ω . In this case, the loop gain can be re-written as:

$$G_L(s) = G_0 \frac{(1 + s\tau_{zl}) \times (1 + s\tau_{zh}) \times \left(1 - s \frac{\frac{L}{D'R_{load}} - nR_T C}{D'}\right)}{s \times \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)}, \quad (4)$$

where $Q = \frac{D'\sqrt{CR_{load}}}{\sqrt{L}}$ is the filter quality factor, and the gain $G_0 = -\frac{G_{C0}V_{out}}{nD'}$ is given by the product of the gain of the control-to-output transfer function and the compensator gain G_{C0} . The widest loop bandwidth is achieved when the complex poles in (4) are at their maximum frequencies, i.e. when V_{in} is at its maximum and the load current is zero. To have a maximum bandwidth of 150 kHz under this condition, the required compensator gain of $G_{C0} = 111$ dB is obtained from (4). Figure 2 shows the variation of the loop-gain magnitude and the phase margin for three different input voltages V_{in} and a fixed load current of $I_{load} = 0.8$ A. To better verify the data, each of the diagrams is computed using both a MATLAB continuous-time model (continuous line) and a AC periodic simulation in SIMPLIS (dotted line). The large bandwidth variation is mainly given by a shift of the complex pole pair frequency ω_0 . However, the inaccurate cancellation of the RHP zero is responsible for the larger phase margin. At low load currents, when the term $\frac{L}{D'R_{load}}$ in (3) is negligible with respect to $nR_T C$, the minimum LHP zero frequency is achieved, whose expression is:

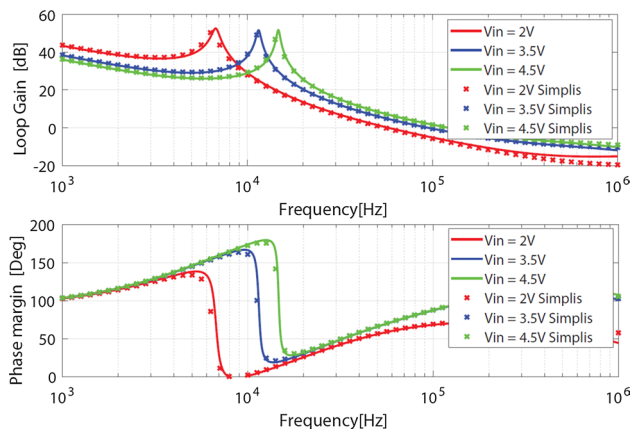


Fig. 2 Loop gain and phase margin of a boost converter in case (A) across three input voltage values and at a load current of $I = 0.8$ A

$$\omega_{z,rhp,min} = \frac{D'_{min}}{nR_T C} = -\frac{V_{in,min}}{V_{out} nR_T C}. \tag{5}$$

Using the parameters in this case study, the minimum LHP zero frequency from (5) is 163 kHz, which is very close to the maximum crossover frequency of 150 kHz. As a result, the slope of the loop gain magnitude near the crossover goes above -20 dB/dec. This effect increases the sensitivity of the loop gain crossover frequency with respect to the process, voltage and temperature (PVT) variations.

3.2 Stability in case (B)

The second design approach is to select R_T so that the RHP zero is shifted to the LHP and used in place of the high frequency zero ω_{zh} of the compensator. Applying this condition to the worst case of the minimum V_{in} and the maximum I_{load} , the required transimpedance is given by:

$$R_T = \frac{\left(\frac{L}{D'_{min} R_{load,min}} + \frac{D'_{min}}{\omega_{zh}}\right)}{nC} = \frac{\left(\frac{L I_{load,max}}{V_{in,min}} + \frac{V_{in,min}}{\omega_{zh} V_{out}}\right)}{nC}. \tag{6}$$

Taking into account the parameters of this case study, the required transimpedance from (6) is $R_T = 15$ m Ω . The overall loop gain can be written as:

$$G_L(s) = G_0 \frac{(1 + s\tau_{z1}) \times \left(1 - s \frac{\frac{L}{D'R_{load}} - nR_T C}{D'}\right)}{s \times \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)}, \tag{7}$$

In the previous case, the largest loop bandwidth should not exceed 150 kHz. Thus, a compensator gain G_{C0} of 118 dB is needed in this case. Figure 3 shows the loop gain

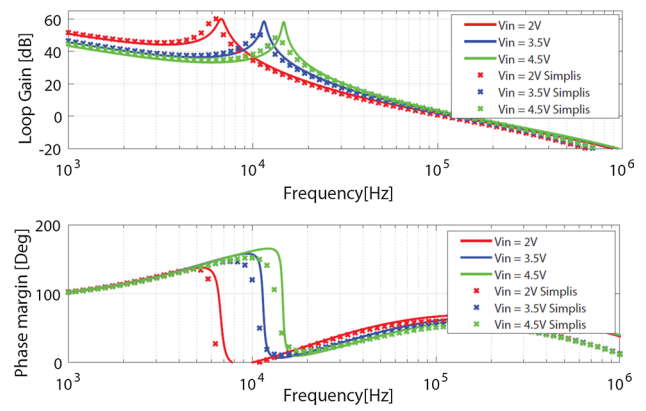


Fig. 3 Loop gain and phase margin of a boost converter in case (B) across three input voltage values and at a load current of $I = 0.8$ A

magnitude and phase margin at different V_{in} values. In the previous case, the data are obtained using both a continuous-time model (continuous line) and a periodic small-signal model (dotted line). The magnitude plot shows the expected shift of the complex pole pair with the input to output ratio. Unlike the previous case, this effect does not seem to significantly influence the crossover frequency and the phase margin. This behavior can be explained by recalling that the LHP zero and the complex poles have the same dependency on D' to the first order. Due to this singularity tracking, the converter bandwidth and phase margin remain relatively stable over the entire working range.

3.3 Stability in case (C)

In this case, the RHP zero is moved to the LHP and used in place of the low frequency zero ω_{z1} of the compensation network. In the worst-case condition of the minimum V_{in} and the maximum I_{load} , the required transimpedance has the same expression in (6) but with ω_{z1} instead of ω_{zh} . Solving the equation a value of $R_T = 60$ m Ω is obtained for the case study. The loop gain is:

$$G_L(s) = G_0 \frac{(1 + s\tau_{zh}) \times \left(1 - s \frac{\frac{L}{D'R_{load}} - nR_T C}{D'}\right)}{s \times \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)}, \tag{8}$$

Thus, the value of the compensator gain G_{C0} to obtain the maximum bandwidth turns out to be $G_{C0} = 120$ dB. Figure 4 shows the loop gain magnitude and phase margin for the three values of V_{in} . The diagrams are computed with the same technique as the previous two cases. The lower sensitivity to V_{in} with respect to case (B) follows from the larger value of $nR_T C$ which makes it dominant in the denominator in (3). This allows for a better frequency tracking of the zero

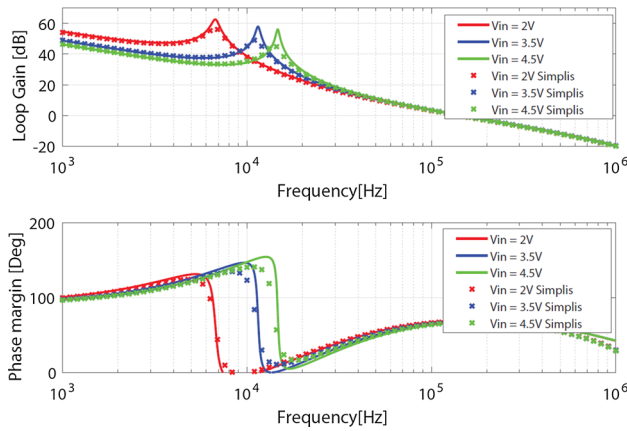


Fig. 4 Loop gain and phase margin of a boost converter in case (C) across three input voltage values and at a load current of $I = 0.8$ A

and the complex poles. Comparing the three design cases, it can be concluded that by increasing the R_T value, the loop gain crossover frequency, and the phase margin become less dependent on the operating conditions (input voltage and load current). In particular, choosing a value of R_T as in case (A) or lower is not recommended since this leads to a large variation in terms of the bandwidth and phase margin at different operating conditions, which impairs the robustness of the converter. Case (B) and case (C) are better choices since they have been proven to be less susceptible to RHP variation.

4 Tracking error correction

Adopting the above-discussed RHP zero mitigation technique, the reference voltage of the compensator is not directly compared with the voltage of the filter capacitor. Instead, it is compared with the sum of the output voltage and the scaled inductor current. Thus, at the steady-state, the following equation holds:

$$V_{\text{ref}} = \frac{V_{\text{out}}}{n} + R_T I_{\text{ind}}, \quad (9)$$

where I_{ind} is the average inductor current. This means that the output voltage is affected by the static error $V_{\text{tr}} = nR_T I_{\text{ind}}$. The first parameter affecting V_{tr} is the average inductor current, which depends on the output load current $I_{\text{ind}} = \frac{I_{\text{load}}}{\eta D'}$, where η is the transfer efficiency. The maximum error is obtained at the maximum load current and the minimum input voltage. Considering a transfer efficiency η of 100%, the maximum average inductor current I_{ind} in this case, the study is equal to 2 A. The second parameter influencing the tracking error is the transimpedance R_T , whose value depends on the chosen design strategy. Case (A) entails the

lowest R_T , which leads to minimum error. On the other hand, case (C) results in the largest offset. The maximum tracking error calculated for the three design strategies (A), (B), and (C) are 40 mV (0.8% of V_{out}), 150 mV (3%), 600 mV (12%), respectively.

In applications where the static error is unacceptable, an error correction strategy must be employed. To understand whether the tracking error can be eliminated without impairing the RHP zero mitigation technique, we can analyze the transfer function from the duty-cycle to the compensator input $T_{\text{dc}}(s)$ of the system in Fig. 1:

$$T_{\text{dc}}(s) = \frac{V_{\text{out}} \left(1 - s \frac{L}{D'^2 R_{\text{load}}}\right)}{nD' \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)} + \frac{2R_T V_{\text{out}} \left(1 + \frac{sRC}{2}\right)}{D'^2 R_{\text{load}} \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right)}, \quad (10)$$

where the first term of the sum is the control to the output transfer function, $T_{\text{do}}(s)$, divided by n . Meanwhile, the second one is the control to inductance current transfer function, $T_{\text{di}}(s)$, multiplied by R_T . After manipulating (10), T_{dc} can be written as:

$$T_{\text{dc}}(s) = \frac{V_{\text{out}}}{nD'} \left(\underbrace{1}_{T_{\text{do,DC}}} + \underbrace{\frac{2nR_T I_{\text{load}}}{V_{\text{in}}}}_{T_{\text{di,DC}}} + \underbrace{\frac{-sL}{D'^2 R_{\text{load}}}}_{T_{\text{do,AC}}} + \underbrace{\frac{sR_T C}{D'}}_{T_{\text{di,AC}}} \right) \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right). \quad (11)$$

As long as the term $\frac{2nR_T I_{\text{load}}}{V_{\text{in}}}$ in (11) is $\ll 1$, it can be concluded that only the AC value of the $T_{\text{di}}(s)$ transfer function affects the RHP zero mitigation. Thus, the tracking error can be removed in principle by eliminating the DC value of the scaled inductor current before injecting it into the output node. As suggested in [16], this task can be accomplished by applying a high-pass filter to the scaled inductor current (see Fig. 5). The pole of the high-pass filter at an angular frequency of ω_{lp} has to be low enough to preserve the AC content of the control to the inductance transfer function. Starting from (11), neglecting the term $\frac{2nR_T I_{\text{load}}}{V_{\text{in}}}$ and replacing R_T with $\frac{sR_T/\omega_{\text{lp}}}{(1+s/\omega_{\text{lp}})}$, in (11) the following is obtained:

$$T_{\text{dc}}(s) = \frac{\frac{V_{\text{out}}}{nD'} \left(1 + s \left(\frac{1}{\omega_{\text{lp}}} - \frac{L}{R_{\text{load}} D'^2}\right) + s^2 \left(\frac{nR_T C - \frac{L}{R_{\text{load}} D'}}{\omega_{\text{lp}} D'}\right)\right)}{\left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1\right) \left(1 + \frac{s}{\omega_{\text{lp}}}\right)}. \quad (12)$$

If ω_{lp} is chosen so that $\omega_{\text{lp}} \ll \frac{R_{\text{load}} D'^2}{L}$ and $\omega_{\text{lp}} \ll \frac{D'}{nR_T C - \frac{L}{R_{\text{load}} D'}}$, Eq. (12) can be approximated with (11). This means that the

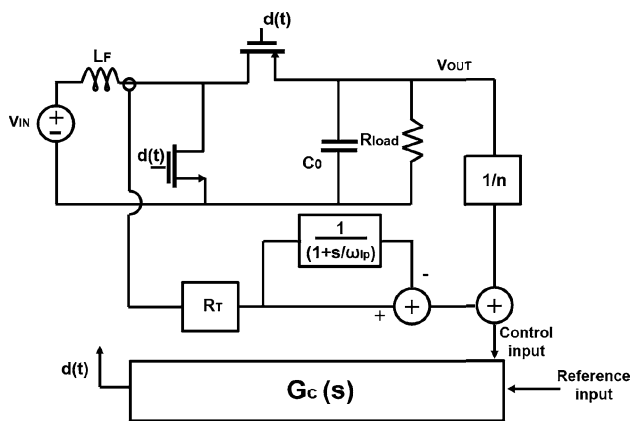


Fig. 5 Simplified schematic block of the proposed boost converter with tracking error correction

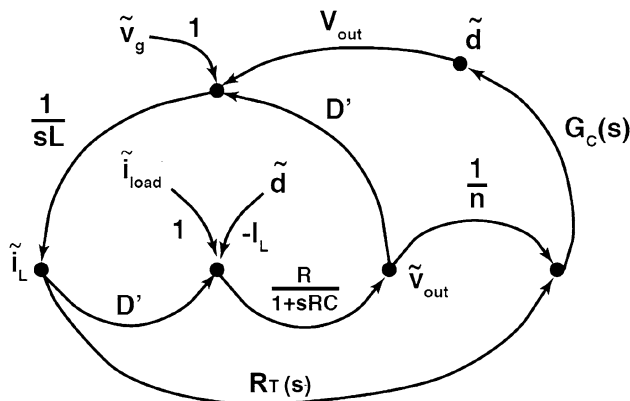


Fig. 6 Flowgraph of the proposed boost converter

addition of the high pass filter in Fig. 5, does not affect the system stability as long as the frequency of the pole ω_{lp} is chosen properly.

5 Transient response

5.1 Load transient response

The load transient response is determined by the closed-loop output impedance, $Z_{out}(s)$. This can be computed from the flowgraph of the circuit shown in Fig. 5. The flowgraph is shown in Fig. 6, where \tilde{v}_g represent a variation of the input voltage, \tilde{i}_{load} represent a variation of the load current, $G_C(s)$ is the compensator transfer function, and $R_T(s) = \frac{sR_T/\omega_{lp}}{(1+s/\omega_{lp})}$ is the high-pass filtered transimpedance

R_T . Solving the flowgraph under the hypothesis of $\tilde{v}_g = 0$ yields:

$$Z_{out}(s) = \frac{\frac{sL}{D'^2 \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right)}}{1 - G_L(s)} - \frac{\frac{V_{out} R_T(s) G_C(s)}{D'^2 \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right)}}{1 - G_L(s)} = Z_{out_1}(s) + Z_{out_2}(s), \tag{13}$$

where the loop gain $G_L(s)$ must be replaced with the loop gain from (4) or (7) depending on the type of design adopted. For comparison, the output impedance of a boost converter with no RHP zero mitigation can be calculated as:

$$Z_{out_{no-mit}}(s) = \frac{\frac{sL}{D'^2 \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right)}}{1 - G_{L_{no-mit}}(s)}. \tag{14}$$

Notice that the expression of $Z_{out_{no-mit}}$ is similar to that of the first term of Z_{out} , with the loop gain $G_L(s)$ being the only difference. To assess the impact of the RHP zero mitigation on the load transient response, the transient response obtained from (13) is compared with that obtained from (14). For the sake of simplicity, the peak output voltage variation ΔV_{out} caused by a step current variation ΔI_{load} is considered. Under simplifying assumptions, the peak output voltage variation is:

$$\Delta V_{out_{no-mit}} = - \frac{\Delta I_{load} n L \omega_{zh} \omega_{zl}}{D' G_{C0_{no-mit}} V_{out}}. \tag{15}$$

The magnitude of the compensator gain depends on the target zero dB crossing of the loop gain, which in turn depends on the minimum frequency of the RHP zero. Since the two zeroes of the compensation network are placed to eliminate the complex pole pair, the zero dB crossing frequency can be approximated as that of an integrator $\frac{V_{out} G_{C0_{no-mit}}}{s n D'}$. Considering the maximum bandwidth to be a fraction of the RHP zero frequency $\omega_c = \frac{\omega_{z,rhp}}{\alpha}$, the voltage variation in (15) can be rewritten as:

$$\Delta V_{out_{no-mit}} = - \frac{\Delta I_{load} L \omega_{zh} \omega_{zl} \alpha}{D' \omega_{rhp}}. \tag{16}$$

The voltage variation in (16) must be compared with the corresponding term generated by (13). The output impedance in (13) includes two terms, the first is similar to the closed-loop impedance of a standard boost converter, and the second is generated by the RHP zero mitigation technique. The first term leads to ΔV_{out1} which has the same expression reported in (15). The only difference is the DC value of the compensator gain (G_{C0} instead of $G_{C0_{no-mit}}$). Considering a large loop gain, the second term

of (13) becomes $Z_{out_2}(s) = \frac{snR_T}{\omega_p D' \left(1 + \frac{s}{\omega_p}\right)}$. The peak voltage generated by a load current step variation ΔI_{load} is:

$$\Delta V_{out_2} = -\frac{\Delta I_{load} n R_T}{D'} \quad (17)$$

This contribution depends on the input to output ratio, has a magnitude proportional to the transimpedance value R_T and does not depend on the system bandwidth. Combining (15), (16), and (17) yields:

$$\frac{\Delta V_{out}}{\Delta V_{out_{no-mit}}} = \frac{\Delta V_{out_1} + \Delta V_{out_2}}{\Delta V_{out_{no-mit}}} = \left(\frac{G_{C0_{no-mit}}}{G_{C0}} + \frac{n R_T D' \omega_{rhp}}{L \omega_{z1} \omega_{zh} \alpha} \right) \quad (18)$$

When the ratio expressed in (18) is less than 1, the load transient performance of a boost converter with RHP zero mitigation is better than that of a standard boost converter limited by a RHP zero. For this to occur, the transimpedance R_T must fulfill the following inequality:

$$R_T < \left(1 - \frac{G_{C0_{no-mit}}}{G_{C0}}\right) \frac{L \omega_{zh} \omega_{z1} \alpha}{n D' \omega_{rhp}} \quad (19)$$

Notice that the compensator gain is proportional to the system bandwidth. Thus, the following inequality holds true $G_{C0} \gg G_{C0_{no-mit}}$ since the RHP zero mitigation provides an increase in the bandwidth. Accordingly, the term inside the parenthesis is $\simeq 1$. Combining (19) with the equation describing the RHP zero in (2) yields:

$$R_T < \frac{L^2 \omega_{zh} \omega_{z1} \alpha I_{load,max}}{n V_{in} D'^2_{min}} \quad (20)$$

Solving this inequality under the worst case, i.e. with $V_{in} = V_{in,max}$ and $\alpha = 5$, yields $R_T < 30 \text{ m}\Omega$. In contrast to the conclusions drawn in Sect. (3), the load transient performance improves when R_T decreases. In particular, case (A) provides a significant improvement in the load transient performance. Meanwhile, case (C) has a load transient behavior far worse than that of a boost converter limited by RHP zero.

5.2 Line transient response

The line transfer function is obtained starting with the flowgraph in Fig. 6 considering no-load current variation, i.e. $\tilde{i} = 0$.

$$T_{line}(s) = \frac{1}{D' \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right)} - \frac{I_{load} R_T(s) G_C(s)}{D'^3 \left(\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1 \right)} = T_{line_1}(s) + T_{line_2}(s) \quad (21)$$

where the loop gain is the one computed in the previous section. In the load transient case, (21) includes two contributions. The first contribution is the standard line transfer function of a boost converter, and the second contribution is generated by the RHP zero mitigation technique. For comparison, the line transfer function of a standard boost converter is:

$$T_{line_{no-mit}}(s) = \frac{1}{1 - G_{L_{no-mit}}(s)} \quad (22)$$

The load transient case (22) is similar to $T_{line_1}(s)$ except for the loop gain. To assess the line transient performance, the peak output voltage variation obtained from (21) is compared with the one given by (22). The peak variation of the output voltage for a step variation of the input voltage ΔV_{in} in the case of a standard boost converter without zero mitigation is:

$$\Delta V_{out_{no-mit}} = -\frac{\Delta V_{in} n \omega_{zh} \omega_{z1}}{V_{out} G_{C0_{no-mit}} \Delta \omega} \left[-\left(\frac{\omega_{z1}}{\omega_{zh}} \right)^{\frac{\omega_{zh}}{\Delta \omega}} + \left(\frac{\omega_{z1}}{\omega_{zh}} \right)^{\frac{\omega_{z1}}{\Delta \omega}} \right] \quad (23)$$

where $\Delta \omega = \omega_{zh} - \omega_{z1}$. The value of the compensator gain is related to the zero dB crossing of the loop gain which is related to the frequency of the RHP zero. By estimating the compensator gain $G_{C0_{no-mit}}$ as that of an integrator $\frac{G_{C0_{no-mit}} V_{out}}{\omega_{rhp}}$ and assuming the crossover frequency to be $\omega_c = \frac{\omega_{rhp}}{\alpha}$, (23) can be rewritten as:

$$\Delta V_{out_{no-mit}} = -\frac{\alpha \Delta V_{in} \omega_{zh} \omega_{z1}}{D' \omega_{rhp} \Delta \omega} \left[-\left(\frac{\omega_{z1}}{\omega_{zh}} \right)^{\frac{\omega_{zh}}{\Delta \omega}} + \left(\frac{\omega_{z1}}{\omega_{zh}} \right)^{\frac{\omega_{z1}}{\Delta \omega}} \right] \quad (24)$$

This result should be compared with the peak voltage value derived from (21). As can be seen in Sect. 5.1, the first term in (21) leads to the contribution of ΔV_{out_1} , which has the same expression as that reported in (23) but for the DC value of the compensator gain ($G_{C0} \gg G_{C0_{no-mit}}$). Considering a large loop gain, the second term of (21) $T_{line_2}(s)$ can be approximated as $T_{line_2}(s) = -\frac{s I_{load} n R_T}{D' \omega_p V_{in} \left(1 + \frac{s}{\omega_p}\right)}$. This leads to a

peak output voltage variation, considering a step input voltage ΔV_{in} , and is equal to:

$$\Delta V_{out_2} = \frac{\Delta V_{in} n R_T I_{load}}{V_{in} D'} \quad (25)$$

This contribution is proportional to the steady-state load current I_{load} , and it does not depend on system bandwidth. Combining (23), (24), and (25) yields:

$$\frac{\Delta V_{out}}{\Delta V_{out_{no-mit}}} = \frac{\Delta V_{out_1} + \Delta V_{out_2}}{\Delta V_{out_{no-mit}}} = \frac{G_{C0_{no-mit}}}{G_{C0}} + \frac{nR_T \omega_{zrhp} \Delta \omega I_{load}}{V_{in} \omega_{z1} \omega_{zh} \alpha \left[-\left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{zh}}{\Delta \omega}} + \left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{z1}}{\Delta \omega}} \right]} \quad (26)$$

When the ratio in (26) is less than 1, the boost converter with RHP zero mitigation provides some advantage over the standard boost in terms of line transient response. For this to happen R_T must fulfill the following inequality:

$$R_T < \left(1 - \frac{G_{C0_{no-mit}}}{G_{C0}}\right) \times \frac{V_{in} \omega_{zh} \omega_{z1} \alpha}{n \omega_{rhp} \Delta \omega I_{load}} \left[-\left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{zh}}{\Delta \omega}} + \left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{z1}}{\Delta \omega}} \right] \quad (27)$$

As concluded in Sect. 5.1, the term in the first parenthesis is ≈ 1 . Combining (27) with (2) in the worst-case scenario of $V_{in, min}$ and $I_{load, max}$ the inequality (27) becomes:

$$R_T < \frac{L \omega_{zh} \omega_{z1} \alpha}{n \Delta \omega D'_{min}} \left[-\left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{zh}}{\Delta \omega}} + \left(\frac{\omega_{z1}}{\omega_{zh}}\right)^{\frac{\omega_{z1}}{\Delta \omega}} \right] \quad (28)$$

In agreement with the conclusions drawn in Sect. 5.1, the smaller the value of R_T the better the performance of a boost converter with RHP zero mitigation in terms of line transient response. Solving (27) with $\alpha = 5$, a transimpedance value $R_T < 115 \text{ m}\Omega$ is obtained. This value is larger than the transimpedance values calculated for all three of the case studies, which means that the RHP zero mitigation technique always improves the line transient performances when compared with a standard boost.

6 Simulation results

To validate the analysis, the dynamic performance of a boost converter with RHP zero mitigation has been simulated for the three design cases, (A), (B), and (C), using

Cadence-Virtuoso. The validation includes two steps. First, the line and the load transient responses for the boost converter in Fig. 5 with different design strategies are compared and commented upon. Then the line and load transient responses of a boost with design (B), which is the one with a better trade-off between dynamic performance and stability, are compared with those of a standard boost converter without RHP zero mitigation. All of the results shown in this section refer to a frequency of the compensation pole ω_{lp} that is equal to 1/4 of the zero in (3). This choice does not significantly affect the stability of the system, which remains close to the system estimated in Sect. 3. The main parameters used for the simulation of each case study are summarized in Table 1. The line transient response is simulated considering a fixed load current of 0.8 A and an input voltage variation of $V_{in} = 2 \text{ V} \rightarrow 2.5 \text{ V}$ for the three case

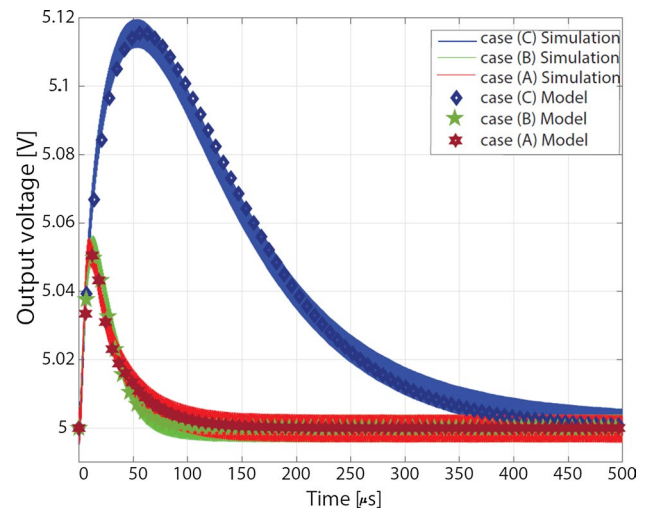


Fig. 7 Line transient comparison. Time response computed with a fixed load current of 0.8 A and an input voltage variation of $V_{in} = 2 \rightarrow 2.5 \text{ V}$. The continuous line is obtained from a Cadence-Virtuoso transient simulation, and the dashed line is the step response from Eq. (21)

Table 1 Main parameters for each case study

	Case-A	Case-B	Case-C	No-mitigation
L	2.2 μH	2.2 μH	2.2 μH	2.2 μH
C	44 μF	44 μF	44 μF	44 μF
n	5	5	5	5
f_{sw}	1.5 MHz	1.5 MHz	1.5 MHz	1.5 MHz
R_T	4m Ω	15 m Ω	60 m Ω	0
ω_{lp}	$2\pi 72 \text{ kHz}/4$	$2\pi 25 \text{ kHz}/4$	$2\pi 5 \text{ kHz}/4$	–
τ_{z1}	$1/2\pi 5 \text{ kHz}$	$1/2\pi 5 \text{ kHz}$	–	$1/2\pi 3 \text{ kHz}$
τ_{zh}	$1/2\pi 25 \text{ kHz}$	–	$1/2\pi 25 \text{ kHz}$	$1/2\pi 10 \text{ kHz}$
G_{C0}	111 dB	118 dB	120 dB	87 dB
$G_{C(s)}$	$G_{C0} \frac{(1+s\tau_{z1})(1+s\tau_{zh})}{s}$	$G_{C0} \frac{(1+s\tau_{z1})}{s}$	$G_{C0} \frac{(1+s\tau_{zh})}{s}$	$G_{C0} \frac{(1+s\tau_{z1})(1+s\tau_{zh})}{s}$
$G_L(s)$	Equation (4)	Equation (7)	Equation (8)	Equation (4)

studies, (A), (B), and (C). Figure 7 shows a comparison of the transient response obtained from Cadence-Virtuoso and the linear step response given by (21).

The comparison shows that design case (C) has a larger transient response with respect to that of the case (A) and case (B) designs, due to the higher R_T value. From Fig. 7, it is possible to see that the peak voltage variation for case (C) is about 120 mV, which is in close agreement with the value obtained from the first-order estimation in (25) for the same variation: 150 mV. The peak voltage variation in the figure is lower due to the effect of the mid-frequency poles inside the loop that have been neglected in the analysis. On the other hand, the line transient responses for cases (B) and (A) are very similar to each other and their peaks, which are about 50 mV, do not respect the estimation given in (25), which are equal to 30 mV and 8 mV, respectively.

This happens because the two contributions in (21) are similar in magnitude. A result can be obtained by summing the values provided by (25) and (23). By doing so, a voltage variation of 51 mV for case (B) and 40 mV for case (A) are obtained, which provides a better first-order estimation with the results in Fig. 7. The line transient waveform depends on which one of the two contributions in (21) is dominant. When the second one is dominant, as in case (C), the time transient shows an exponential recovery with a time constant of $1/\omega_{lp}$. When the first one is dominant, as in case (A), the time constant of the recovery transient is $1/\omega_{z1}$. Case (B) falls in between since the two terms in (21) have comparable magnitudes.

The load transient response has been simulated considering a load current step variation of $\Delta I_{load} = 0.1A \rightarrow 0.8A$

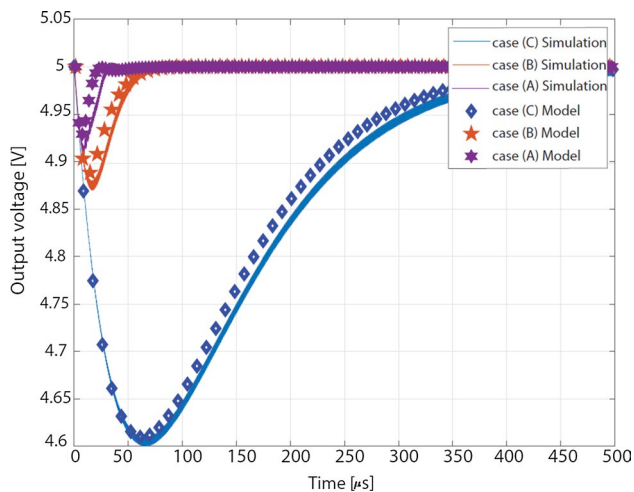


Fig. 8 Load transient comparison. Time response computed with a fixed input voltage of 2 V and a load current variation of $\Delta I_{load} = 0.1A \rightarrow 0.8A$. The continuous line is obtained from a Cadence-Virtuoso transient simulation, and the dashed line is the step response from Eq. (13)

with a fixed input voltage of $V_{in} = 2V$. Figure 8 shows a comparison between the transient response obtained from Cadence-Virtuoso and the linear step response given by (13). Similar to the line transient case, the peak voltage obtained in the case (C) design is dominated by the contribution of $Z_{out_2}(s)$ in (13), and its magnitude is much higher than the other design cases due to the large R_T value. The peak voltage variation from Fig. 8 is about 400 mV which is slightly lower than the estimation in (17) 525 mV due to the effect of the high-frequency poles neglected in the analysis. The peak voltage in (B) 120 mV is still dominated by the second contribution in (13), and its amplitude is well predicted by (17): 131 mV. Finally, case (A) (90 mV) presents a load transient response where the two contributions in (13) have similar impacts on the output voltage variation.

For this reason, a fair estimation of the peak voltage variation can be achieved by summing the values provided by (17) and (15), which yields 89 mV. Concerning the transient recovery time, case (C) and case (B) are mainly determined by the time constant $1/\omega_{lp}$, which is the load transient response in (13) dominated by the second term. Note that the value of the time constants $1/\omega_{lp}$ in case (C) and case (B) are different, and are proportional to R_T . Finally, the recovery transient in case (A) is dependent on both $1/\omega_{zh}$ and $1/\omega_{lp}$, since the two contributions in (13) are similar in magnitude.

To complete the validation, the load and line transient responses of the case (B) are compared with those of a boost converter where the crossover frequency of the control loop ω_c is limited to a fraction $\omega_{zrhp}/4$ of its RHP zero. However, this design leads to an unstable converter since $\omega_c < \omega_{zh}$. To reach a phase margin of about 40° , the frequency of the zeroes and the loop gain have been changed to: $\omega_{zh} = 2\pi 10$ kHz, $\omega_{z1} = 2\pi 3$ kHz, and $G_{C0} = 87$ dB. The transient responses of the two systems for a line voltage

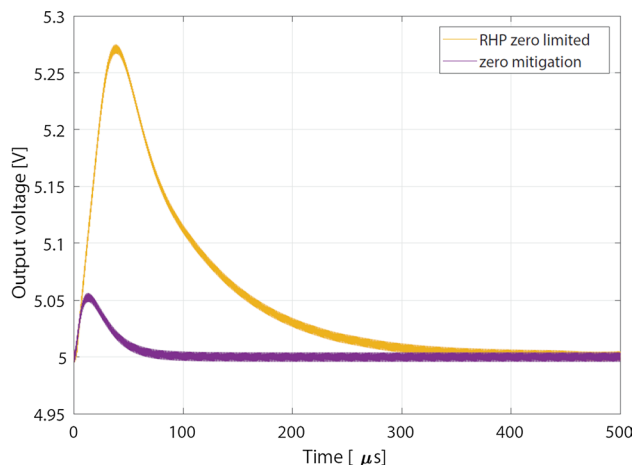


Fig. 9 Line transient comparison of a system with zero mitigation with respect to a system without it. The load current is 0.8A and the input voltage variation is $\Delta V_{in} = 2V \rightarrow 2.5V$

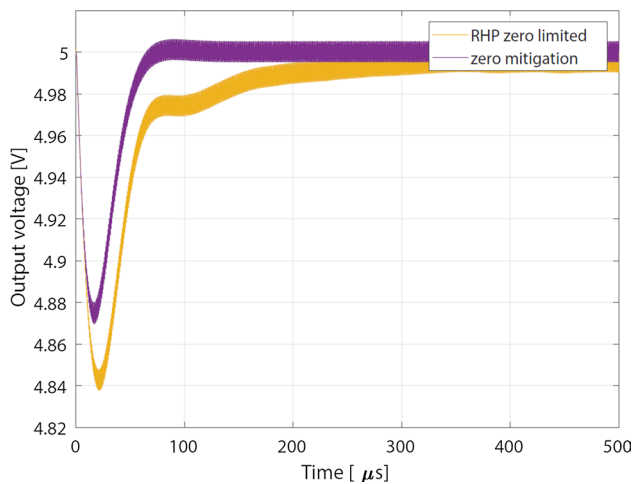


Fig. 10 Load transient comparison of a system with zero mitigation with respect to a system without it. The input voltage is 2 V and the load current variation is $\Delta I_{\text{load}} = 0.1A \rightarrow 0.8A$

variation of $\Delta V_{\text{in}} = 2V \rightarrow 2.5V$ and a fixed load current of $I_{\text{load}} = 0.8A$ are shown in Fig. 9. As expected from the analysis in Sect. (5), the RHP zero mitigation provides an improvement in the line transient response of the system provided that the maximum the achievable crossover frequency of the boost converter is limited by the presence of an RHP zero. Finally, a comparison of the load transient responses of the two systems is shown in Fig. 10. The simulation has been carried out with a fixed input voltage of 2 V and a load current variation of $\Delta I_{\text{load}} = 0.1A \rightarrow 0.8A$. The difference between the two transient responses is very small even if the loop crossover frequency of the boost with RHP zero mitigation is about a factor of 8 higher than that of the boost with no RHP zero mitigation. This result is in an agreement with the analysis in Sect. (5), which demonstrates that the advantages of the RHP zero mitigation technique in terms of load transient performance are limited.

7 Conclusion

This paper fully addresses the impact of the RHP zero mitigation technique on the dynamic performance of a boost converter. A first trade-off is identified between system stability and transient response, where the transimpedance R_T is applied to the inductor current to move the zero from the RHP to the LHP is the main trade-off parameter. The role

of the tracking error correction network is analyzed as well. The analysis shows a second trade-off between the static precision and the transient response of the output voltage. Based on these findings, design guidelines are provided to help maximize system performance. Different design strategies have been applied to a realistic case-study and compared with the same boost converter without zero mitigation, which demonstrates that that an optimal choice of R_T can greatly improve both the stability and the line transient response. On the other hand, the improvement in terms of load transient response is only marginal, even if the optimal design criteria are met. Circuit simulations performed with Cadence-Virtuoso are presented to validate the analysis. Work is ongoing on the identification of alternate tracking-error correction networks capable of breaking the trade-off between the static precision and transient response of the output voltage.

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References

1. Wei-Chung, W., Bass, R.M., Yeargan, J.R.: Eliminating the effects of the right-half plane zero in fixed frequency boost converters. In: 29th Annual IEEE Power Electronics Specialists Conference, vol. 1, 362–366 (1998).
2. Sable, D.M., Cho, B.H., Ridley, R.B.: Elimination of the positive zero in fixed frequency boost and flyback converters. In: Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition, 205–211 (1990).
3. Viswanathan, K., Oruganti, R., Srinivasan, D.: A novel tri-state boost converter with fast dynamics. *IEEE Trans. Power Electr.* **17**(5), 677–683 (2002)
4. Kapat, S., Patra, A., Banerjee, S.: A Current-controlled tristate boost converter with improved performance through RHP Zero-Elimination. *IEEE Trans. Power Electr.* **24**(3), 776–786 (2009)
5. Luo, Y., Su, Y., Huang, Y., Lee, Y., Chen, K., Hsu, W.: Time-multiplexing current balance interleaved current-mode boost DC-DC

- converter for alleviating the effects of right-half-plane zero. *IEEE Trans. Power Electr.* **27**(9), 4098–4112 (2012)
6. Calvente, J., Martinez-Salamero, L., Valderrama, H., Vidal-Idiarte, E.: Using magnetic coupling to eliminate right half-plane zeros in boost converters. *IEEE Power Electr. Lett.* **2**(2), 58–62 (2004)
 7. Liu, H., Zhang, D.: Two-phase interleaved inverse-coupled inductor boost without right half-plane zeros. *IEEE Trans. Power Electr.* **32**(3), 1844–1859 (2017)
 8. Poorali, B., Adib, E.: Right-half-plane zero elimination of boost converter using magnetic coupling with forward energy transfer. *IEEE Trans. Ind. Electr.* **66**(11), 8454–8462 (2019)
 9. Sun, J.: Characterization and performance comparison of ripple-based control for voltage regulator modules. *IEEE Trans. Power Electr.* **21**(2), 346–353 (2006)
 10. Redl, R., Sun, J.: Ripple-based control of switching regulators. An Overview. *IEEE Trans. Power Electr.* **24**(12), 2669–2680 (2009)
 11. Huang, H.H., Chen, C.L., Wu, D.R., Chen, K.H.: Solid-duty-control technique for alleviating the right-half-plane zero effect in continuous conduction mode boost converters. *IEEE Trans. Power Electr.* **27**(1), 354–361 (2012)
 12. Song, T., Chung, H.S.: Boundary control of boost converters using state-energy plane. *IEEE Trans. Power Electr.* **23**(2), 551–563 (2008)
 13. Yousefzadeh, V., Shirazi, M., Maksimovic, D.: Minimum phase response in digitally controlled boost and flyback converters. In: *APEC 07-Twenty-Second Annual IEEE Applied Power Electr. Conference and Exposition*, 865–870 (2007).
 14. Hariharan, K., Kapat, S.: Near optimal controller tuning in a current-mode DPWM boost converter in CCM and application to a dimmable LED array driving. *IEEE J. Emerg. Sel. Top. Power Electr.* **7**(2), 1031–1043 (2019)
 15. Hariharan, K., Kapat, S., Mukhopadhyay, S.: Constant off-time digital current-mode controlled boost converters with enhanced stability boundary. *IEEE Trans. Power Electr.* **34**(10), 270–281 (2019)
 16. Paduvalli, V.V., Taylor, R.J., Hunt, L.R., Balsara, P.T.: Mitigation of positive zero effect on nonminimum phase boost DC/DC converters in CCM. *IEEE Trans. Power Electr.* **65**(5), 4125–4134 (2018)



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