# Large Room-Temperature Electroresistance in Dual-Modulated Ferroelectric Tunnel Barriers

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Wave functions of free electrons of metals can propagate across insulating barriers eventually giving rise to a finite conductance across ultrathin barriers in metal–insulator–metal sandwiches. The "tunnel conductance" is primarily limited by the energy barrier height ($\phi$) of the metal–insulator interface and its width ($t$): $\approx e^{-t\sqrt{\varphi}}$. A ferroelectric layer (FE) is a particular case of insulating layer that allows, upon reversal of its polarization ($P$), the modulation of the barrier properties thus producing a significant change of its electrical resistance, named "tunnel electroresistance" (TER), of high technological interest. Although the concept of ferroelectric tunnel junction (FTJ) was proposed time ago by Esaki et al.,[1] it only drove a renewed attention in recent years due to the report of giant TER in epitaxial $La_{0.67}Sr_{0.33}MnO_3/BaTiO_3$/metal junctions, with values exceeding 75 000% at room-temperature.[2] In this seminal paper, $La_{0.67}Sr_{0.33}MnO_3$ was used as metallic bottom electrode. TER was also observed using $Pb[Zr_{0.2}Ti_{0.8}]O_3$ (PZT) as ferroelectric layer[3–7] and/or Nb:$SrTiO_3$ or $SrRuO_3$[8–10] as bottom metallic electrodes.

TER is basically understood as due to the change of the barrier height upon polarization reversal in presence of asymmetric electrodes. However, as reviewed by Tsymbal and Kohlstedt,[11,12] pure interface effects and strain (piezo) effects may also contribute to barrier modification. These considerations apply when the properties of the metal electrodes do not change appreciably upon charge accumulation/depletion as it occurs when they are sandwiching a FE tunnel barrier. This is not the case when electrodes are made of some strongly correlated metal oxides where metal–insulator transitions can be driven by tiny changes of the carrier concentration. $La_{1-x}A_xMnO_3$ (A = Sr, Ca) manganites are popular examples of this behavior that could be eventually used to engineer the barrier width.[7,13] However, although large values of TER have been obtained by incorporating non-optimally doped ($x$ = 0.5 and 0.2) manganite layers,[7,13] direct experimental evidences of a polarization-induced metal–insulator transition in these layers are lacking. A related case of modulation of the electrodes properties is that of FTJs employing degenerated semiconductors as electrodes, where both the Schottky barrier (SB) and the depletion layer formed at the interface with the FE are influenced by the FE polarization.[14] In particular, the modification of the depletion layer width ($W$) upon $P$ reversal can lead to a modulation of the effective barrier width,[10] thus impacting the measured TER.

Here we report on TER of Pt/$BaTiO_3$/$La_{0.7}Sr_{0.3}MnO_3$ (Pt/BTO/LSMO) tunnel junctions. It will be shown that record values of TER, up to $3 \times 10^4$%, can be observed at room-temperature for large-area junctions ($A$ = 4 to 900 μm$^2$), made using standard lithography techniques. Larger TER values in tunnel junctions involving simple ferroelectric barriers and metallic electrodes have been observed when performing measurements at low temperature or by using nanocontacts.[3,15] Beyond this, a radically new experimental observation is made. It is found that the capacitance of the junctions is bias-voltage and frequency dependent, both fully analogous to the response of metal/insulator/n-type semiconductor (M/I/n-SC) junctions, where these changes are due to the modification of the barrier thickness by bringing the devices to accumulation or depletion regions. Moreover it is found that the junction capacitance is modulated by the polarization. This implies that the properties of the n-doped region, namely, its width and/or permittivity, are polarization-sensitive. Therefore, and in contrast with the common wisdom, polarization does not only change the barrier height but also produces electronic reconstructions at interfaces that contribute to the observed large electroresistance. The simplest explanation of the observed effect is the polarization-dependent extension of a depletion layer existing in an n-doped region at the BTO/LSMO interface. While obtaining room-temperature TER values of about $10^4$% in micro-size devices paves the way to the use of FTJs for practical applications, the discovery that tunnel barrier height and width can both be modulated by polarization, signals new directions for further developments in the field of FTJs.

FTJs were fabricated on Pt(22 nm)/BTO(2–4 nm)/LSMO(30 nm)//$SrTiO_3$(001) heterostructures. In **Figure 1**a we show illustrative $I$–$V$ curves obtained on a junction (denoted B2) with BTO layer 4 nm thick and area A = 60 μm$^2$ using triangular $V(t)$ pulses after a dwell time of few seconds, after poling

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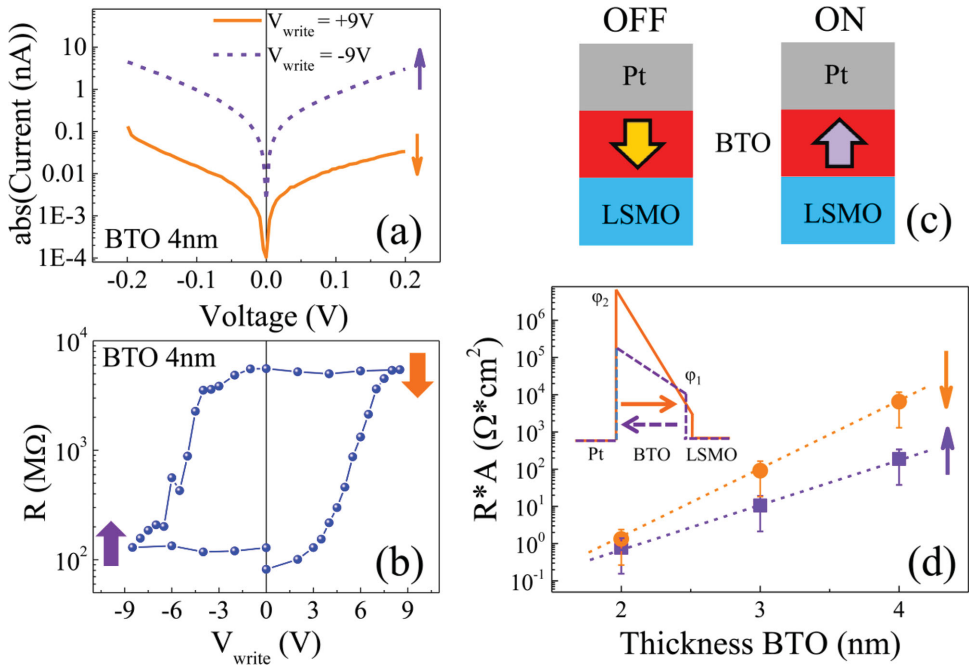


**Figure 1.** a) ON/OFF room-temperature *I–V* characteristics of a representative Pt/BTO(4 nm)/LSMO FTJ with A = 60 μm$^2$. b) Poling-dependent resistance of the same junction. The sketch in c) illustrates the relative orientation of the BTO polarization (arrow) at the ON/OFF states. d) Average measured junction resistance per area product $R \times A$ as a function of BTO barrier thickness. Bars indicate the data dispersion. In the inset: sketch of the barrier for ON/OFF states as deduced from the fits of the *I–V* curves for barriers nominally 4 nm thick. $\phi_1$ and $\phi_2$ are the barrier height at the BTO/LSMO and Pt/BTO interfaces, respectively.

the sample by applying a positive (continuous line) and negative (dashed line) voltage pulse $V_{write}$ about 0.5 s long (see Supporting Information, SI-3). The bottom electrode is grounded. The arrows in Figure 1a indicate the direction of the written polarization. One first notice in Figure 1a that for the up-state (polarization pointing away from the LSMO bottom electrode) the conductance is larger (ON state) than for the down-state, where the polarization points towards the LSMO electrode (OFF state), as indicated in the sketches of Figure 1c. Similar measurements and results are obtained for the BTO films of 2 and 3 nm. In Figure 1d we collect the resistance per area product (R × A) measured for the up- and down-states as a function of BTO film thickness. Note that R × A values displayed in Figure 1d are average values obtained considering all the measured junctions for each BTO thickness. Data for individual junctions are shown in Supporting Information, SI-3 and SI-4. Data in Figure 1d show an exponential dependence of the barrier resistance versus barrier thickness, as expected for tunnel transport, and distinctive values for up and down states illustrating the change of the energy barrier for tunneling upon P switching.

*I–V* curves of Figure 1a can be fitted with the Brinkman model for tunnel transport across trapezoidal potential barriers in the Wentzel–Kramers–Brillouin (WKB) approximation.[8,16,17] For this junction we obtain (see Supporting Information, SI-5): $\phi_{av(ON)} = 0.48$ eV, $\Delta\phi_{(ON)} = 0.38$ Ev, and $t_{(ON)} = 3.51$ nm for the ON state and $\phi_{av(OFF)} = 0.61$ eV, $\Delta\phi_{(OFF)} = 0.85$ eV, and $t_{(OFF)} = 3.71$ nm for the OFF state, where $\phi_{av(ON,OFF)} = (\phi_{1(ON,OFF)} + \phi_{2(ON,OFF)})/2$ and $\Delta\phi_{(ON,OFF)} = (\phi_{1(ON,OFF)} - \phi_{2(ON,OFF)})$ are the average height of the barrier ($\phi_1$ and $\phi_2$ being barrier height at the BTO/LSMO and Pt/BTO interfaces, respectively) and its asymmetry, respectively, and $t_{(ON,OFF)}$ is the thickness of the barrier. A sketch of the resulting shape of the barrier for ON/OFF states is shown in the inset of Figure 1d. Using these energy barrier data, a constant nominal barrier thickness of 4 nm, and a simple TER estimate (Equation (4) of ref. [8]), we obtain ≈3300%. This is in agreement with direct TER measurements reported below. Observation of ON state for P pointing away from the LSMO electrode in LSMO/ferroelectric(BTO or PZT)/metal junctions is in agreement with earlier observations.[2,5–7,13,18–21] We notice however, that a few reports exist that the OFF state is obtained when P points away from LSMO.[3,4,22,23]

In Figure 1b we show the polarization-dependent junction resistance. In this experiment, consecutive poling (writing pulses $V_{write}$) are applied and the junction resistance is subsequently determined by measuring *I–V* curves and extracting the resistance at 100 mV. Data in Figure 1b clearly show that the measured resistance follows a cycle that nicely mimics that of the ferroelectric polarization *P*(*V*) (see Supporting Information, SI-2), confirming that the ON/OFF resistance values are dictated by the polarization state of the FE barrier. From data in Figure 1b, TER ≈ 5 × 10$^3$% in good agreement with TER estimation obtained from the fitting of the *I–V* curves of the same junction (as described above).

The ON/OFF states for BTO films of 4 nm are very stable with a retention time that largely exceeds 3600 s while the thinnest films show a more modest retention (see Supporting Information, SI-3).

Results presented so far, while providing unparalleled values for TER in large BTO junctions (up to 3 × 10$^4$% for 4 nm thick

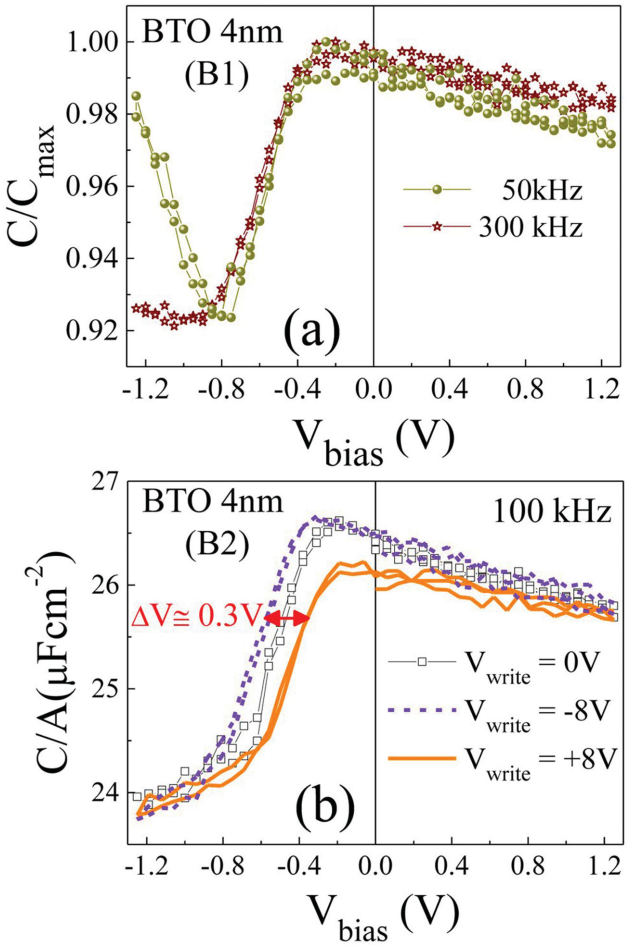


**Figure 2.** a) Capacitance versus $V_{bias}$ curves of a junction (B1) on the Pt/BTO(4 nm)/LSMO heterostructure, measured at different frequencies in a nonprepoled state. b) Capacitance versus $V_{bias}$ curves of another junction (B2) on the same heterostructure measured at 100 kHz in the nonprepoled state (open symbols) and in poled-up (dashed lines) and poled-down (solid lines) states.

BTO, see Supporting Information, SI-4), indicate that there is plenty of room for further improvement, especially if new concepts and material functionalities are exploited in the devices design. The standard picture used to interpret the results, based on the assumption of an asymmetric tunnel barrier whose height is modified by P, assumes that the FE barrier is a pure dielectric, rather than a semiconductor, and neglects the role of the Schottky barriers at M/FE interfaces and the concomitant formation of depletion layers, whose polarization dependence may induce variations of the barrier width. The change of effective barrier thickness extracted from the *I–V* curves in ON/OFF states, although subtle, already points in this direction. In the following we will show that the LSMO/BTO/Pt junctions display features indicating that the barrier width is polarization-modulated, thus impacting the measured TER.

In **Figure 2**a,b we show the capacitance $C$ versus $V_{bias}$ of two junctions (B1 and B2) with 4 nm thick BTO barrier. Figure 2a shows the bias-dependence of C of a nonprepoled junction measured at different frequencies. Data are normalized to the maximum $C$ at $V_{bias} \approx -0.2$ V. It is observed that $C$ is largely modified by $V_{bias}$. Indeed, for $V_{bias} < 0$, $C(V_{bias})$ displays a pronounced reduction at the so-called flat-band voltage $V_{FB} \approx -0.4$ V. At more negative $V_{bias}$ the capacitance develops either a plateau or recovers its initial larger value depending on the measuring frequency. These observations indicate that the LSMO/BTO/Pt heterostructure does not behave as an ideal M/I/M capacitor, where the capacitance ($C = \varepsilon_r A/t$ ; $A$, $t$, and $\varepsilon_r$ are the capacitor area, thickness, and relative permittivity, respectively) should be expected to be basically insensitive to frequency and independent of the bias voltage or, in case of a voltage dependent permittivity, the capacitance should follow the $\varepsilon_r(V_{bias})$ dependence. Instead, the observed response is characteristic of M/I/n-type semiconducting junctions.[24] The reduction of capacitance in the $C(V_{bias} < 0)$ curve is associated to the formation of a depletion layer of thickness $W_D$ at the I/n-type interface, whose capacitance is in series with that of the insulating layer, thus causing a reduction of the total capacitance. In other words: upon negative biasing of the metal in M/I/n-type structure, a charge depleted region is formed in the n-type semiconductor that widens the effective width of the dielectric layer, which is then given by $t + W_D$, and concomitantly reduces the capacitance. When $C(V_{bias})$ measurements are performed at even larger negative $V_{bias}$, strong inversion occurs in the semiconductor were minority carriers (holes in the present case) are accumulated at the insulator/semiconductor interface; in this situation, the effective width of the dielectric is given again by that of the insulator and thus the capacitance increases further recovering its initial value. Of course, if the minority carrier concentration cannot follow the frequency of the driving field for the measurement (the ac-field used in capacitance measurements) the capacitance recovery will not be observed. Therefore, when measurements are performed at relatively large frequency, a small $C$ should be observed at $V_{bias} < 0$, while recovering a larger $C$ is possible if a lower measuring frequency is used.[24]

This is just the behavior observed in Figure 2a, where a clear drop of capacitance is visible at $V_{bias} < 0$ when measurements are performed at high frequency but a recovery towards the initial large $C$ value is observed when reducing the frequency. This behavior is also in fully agreement with expectations for a M/I/n-type structure. Before ending, we stress that, in contrast with our experimental results, a M/I/p-SC capacitor would display a reduction of capacitance at $V_{bias} > 0$.

A similar reduction of $C(V_{bias})$ is observed in other junctions either having BTO barriers of 4 nm (i.e., B2, shown in Figure 2b) or in junctions with barriers of 3 nm (see Supporting Information, SI-6).

Consequently, the actual heterostructures should be viewed as metal(Pt)/insulator (BTO)/n-type/metal(LSMO). BTO is commonly an n-type semiconductor. Indeed, BTO can be easily doped by n-type carriers by suitable oxygen vacancies or atomic substitutions. We recall on passing that even the ferroelectric character of BTO has been found to be preserved up to substantially large electron doping levels.[25] Therefore most obviously, the n-type region can be originated at BTO. As LSMO is a hole-type metal, the simplest and most plausible structure compatible with the observed $C(V_{bias}$, frequency) data would be: metal(Pt)/insulator(BTO)/n-type-BTO/metal(LSMO).

The specifi c total capacitance of the M/BTO/M capacitor is C/A $\approx \varepsilon_0\varepsilon_r/d$ where $d$ is the thickness of the dielectric layer ($d = t_{BTO} + W_D$) and $\varepsilon_r$ its relative permittivity. At accumulation ($V_{bias} > 0$), $d = t_{BTO}$ as $W_D = 0$. If we use $\varepsilon_r \approx 60$[17] and $d = 4$ nm (the BTO thickness of this junction) one gets: $C/A \approx 13.3$ μF cm$^{-2}$ which is comparable to the measured value. As the actual value of the permittivity in this ultrathin BTO layer is unknown, one cannot further elaborate on the small difference between the calculated and measured $C$ value. At depletion, the capacitance is reduced by about $\Delta(C/A) \approx 2$ μF cm$^{-2}$, which leads to a depletion layer width $W_D \approx \Delta(C/A) \times d^2/\varepsilon_0\varepsilon_r \approx 0.6$ nm.

In Figure 2b we also include the $C(V_{bias})$ curves of a junction in the nonprepoled state (open symbols) and after poling with either a negative pulse ($V_{write} < 0$; dashed line) or with a positive pulse ($V_{write} > 0$; solid line). We observe that the capacitance in the depletion region ($V < V_{FB}$) depends on the polarization state of BTO. Assuming that the permittivity is not modifi ed by poling, this observation would indicate that the extension of $W_D$ varies with polarization and $C(V_{bias},P_{up}) > C_0(V_{bias}) > C(V_{bias},P_{down})$, where $C_0$ is the capacitance measured in the nonprepoled state. No polarization dependence of the capacitance is visible in the accumulation state: $C(V_{bias},P_{up}) \approx C(V_{bias},P_{down})$. This is fully expected as in the accumulation regime $C$ is almost insensitive to $V_{bias}$.

From data in Figure 2b, the observed change $\Delta C(P) = C(P_{up}) - C(P_{down})$ in the depletion region is $\approx 1$ μF cm$^{-2}$, indicating that the depletion width varies, upon $P$ switching, by about $\Delta W_D(P) \approx \Delta C(P) \times t_{BTO}^2/\varepsilon_0\varepsilon_r \approx 0.3$ nm. Inserting this variation in the simplest TER expression of ref. [8] and using $\phi_{av}$ and $\Delta\phi_{av}$ derived above, we conclude that the contribution of the barrier width variation on the observed TER is of about 25%.

The $V_{FB}$ in M/I/SC junctions is related to the built-in potential at the interface[24] and the shift of the $V_{FB}$ upon $P$ reversal is related to the corresponding change of the Schottky barrier $\Delta\Phi_{SB}(P)$. Using $\Delta P \approx C \times \Delta V_{FB}$,[26] where $C$ is the specific capacitance, we obtain: $\Delta P \approx 26$ μF cm$^{-2} \times 0.3$ V $= 7.8$ μC cm$^{-2}$, which is the right order of magnitude for ultrathin BTO films. On the other hand, $\Delta\Phi_{SB}(P)$ is given by[27] $\Delta V_{FB} \approx \Delta\Phi_{SB} = 2\sqrt{\frac{qP}{4\pi\varepsilon_0^2\varepsilon_{opt}\varepsilon_r}}$ where $\varepsilon_{opt}$ is the high-frequency dielectric constant ($\approx 5.4$[28]), $q$ the elementary charge, $\varepsilon_r \approx 60$, and $P$ is the switchable polarization. We obtain $P \approx 4$ μC cm$^{-2}$, which is again of the right order of magnitude. Finally, the observed different slope of $1/C^2$ versus $V_{bias}$ for $P_{up}$ and $P_{down}$, signaling a change of carrier density $\Delta n$ upon $P$ reversal, gives consistent estimates of $P$ (see Supporting Information, SI-6).

In brief, data in Figure 2 clearly show that the Pt/BTO/LSMO heterostructure can be viewed as a metal(Pt)/insulator(BTO)/n-type-BTO/metal(LSMO) whose depletion layer is modulated by the polarization of the ferroelectric layer. It thus follows that the switching of $P$ has the dual effect of varying the tunnel barrier height and its width. It may not be fortuitous that difference of barrier width extracted from $C(V_{bias},P)$ data upon $P$ reversal ($\Delta W_D(P) = 0.3$ nm) is fully consistent with the corresponding value extracted from the fits of $I$–$V$ data discussed above.

In **Figure 3**a,b we sketch the charge distribution at electron accumulation/depletion, respectively. It is clear from this sketch that the capacitance is reduced in the depletion region ($V_{bias} < 0$).

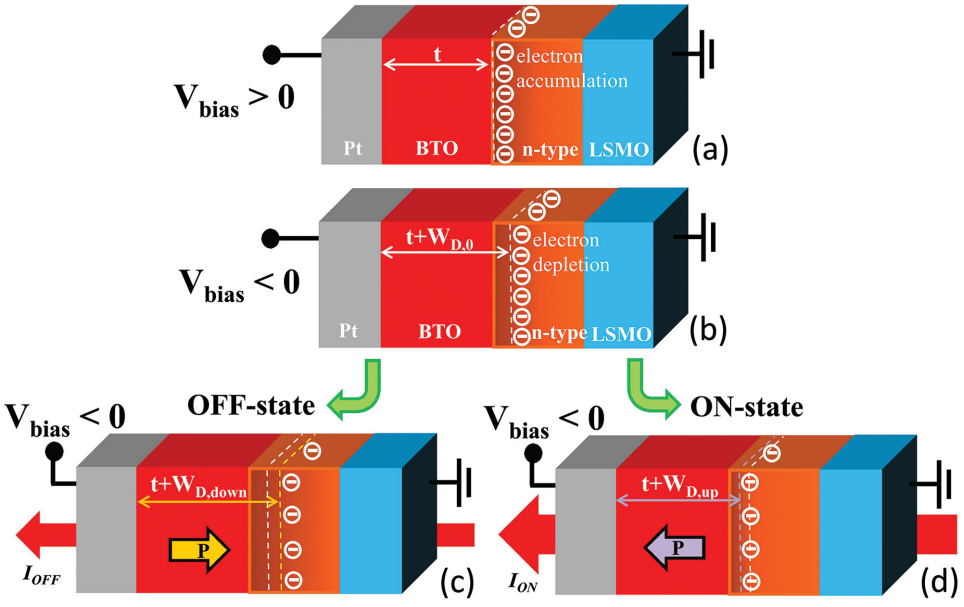


**Figure 3.** Sketch of a Pt/BTO/n-type/LSMO heterostructure. a,b) accumulation ($V_{bias} > 0$) and depletion ($V_{bias} < 0$) regions, respectively, in the nonprepoled state. $W_{D,0}$ and $t$ are the width of the depletion region and the thickness of the dielectric BTO film, respectively. The total width of the dielectric in the capacitor in a) and b) are given by ($t$) and ($t + W_{D,0}$), respectively (horizontal white arrows). The vertical dashed lines indicate the edge of the depletion region. The carrier distribution at negative external bias is controlled by the direction of the ferroelectric polarization. According to capacitance measurements ($C_{down} < C_0 < C_{up}$), the polarization yields either an increase ($W_{D,down} > W_{D,0}$) (pannel c)) or a decrease ($W_{D,up} < W_{D,0}$) (pannel d)) of the width of the depletion. In c,d) the initial position of the depletion edge is indicated for reference (dashed vertical line). Notice that in the OFF state the total barrier width ($t + W_{D,down}$) is larger than in the ON state ($t + W_{D,up}$).

In Figure 3c,d we sketch the situation expected to occur when the polarization of the BTO is included and reversed. The capacitance when the polarization is pointing towards LSMO is smaller than when it is pointing away from LSMO. This is in agreement with the experimental data in Figure 2.

Before concluding, some fi nal comments are in order. First, a change of barrier width under polarization reversal could occur when the piezoresponse of the barrier is taken into account.[29] However, the observed bias and frequency dependence of the junction capacitance does not easily fi t with this scenario. Second, we have shown that the width of the depletion region is rather small (≈2 unit cells (uc)) and its change upon $P$ reversal is ≈1 uc. It could not be a surprise that tiny n-type BTO regions may be formed, during thin fi lm growth, at BTO/LSMO interface. Indeed spectroscopic measurements reveal that electronic reconstructions take place at the BTO/LSMO interface[30] either induced by growth-assisted oxygen vacancy formation in BTO by the competing oxygen affi nity at interface between BTO and LSMO (it is well documented the formation of oxygen vacancies at the interface of BTO and platinum[31]) or by simple interdiffusion of chemical species across the interface.[32] Last but not least, in the data analysis presented above the observed change of capacitance upon P reversal has been assigned to the corresponding change of depletion width in an interfacial n-type region. However, capacitance modulation could also be affected by permittivity changes associated to the polarization-dependent interface electronic and ionic reconstructions. Indeed the permittivity of a ferroelectric capacitor does, in general, depend on voltage and, if the capacitor is asymmetric as in the present case, also on the polarization orientation. As shown by Stengel et al.[33] changes of 10% in the permittivity of BTO itself are quite reasonable to expect in the context of the present system. Therefore one could be tempted to argue, at this point, that capacitance changes due to the dielectric nonlinearity of BTO might be suffi cient to explain some of the data reported in this manuscript, without the need of invoking any n-type character of the semiconducting BTO. This hypothesis, however, does not fi t with the experimental data, because it would not allow explaining neither the asymmetric bias effect on capacitance nor its frequency dependence. Still, mapping permittivity at nanoscale would be required to disentangle its contributions.

In summary we have shown that, using appropriate growth conditions, Pt/BTO/LSMO tunnel junctions can be fabricated, by standard optical lithography techniques, displaying record room-temperature TER values reaching up to $3 \times 10^4$%. This large value is a hallmark that indicates that there is much room for TER improvement in simple Pt/BTO/LSMO heterostructures. Moreover, we have shown that junction capacitance is dependent on the bias voltage and the measuring frequency. The junction capacitance is also found to be modulated by the polarization, indicating that electronic reconstruction that may affect the barrier width (by changing the width of the depletion layer) and/or its permittivity add to the change of barrier height and jointly contribute to the measured TER. We stress here that although changes of capacitance had been reported in engineered metal/BTO/semiconducting structures in which a semiconducting electrode was used on purpose,[10] the observed changes of capacitance were fully attributed to the role of the semiconducting electrode, while neglecting the role of BTO, which is known to be a semiconducting ferroelectric. Here, change of capacitance is observed in junctions where the electrodes are assumed to be metallic: Pt and LSMO.

While several sophisticated scenarios could be invoked to explain the observed changes of capacitance, the present results shine light on an unexplored area of TER response in FTJs. A simple description of observed effects can be built by assuming the presence of an n-type SC region within the metal/BTO/metal heterostructures that should be seen as a metal/BTO/n-SC/LSMO junction. Upon biasing, the n-type region is driven to accumulation or depletion regimes with subsequent changes of the effective barrier width for tunnel transport across the junction. We speculate that, as the width of the depletion layer in a SC is controlled by both the doping level of the ferroelectric layer as well as by the Schottky barrier height, it could be expected that there are opportunities for improvement of the relative change of both barrier height and width upon polarization reversal. Overall, we have shown that measurements of capacitance have provided valuable information on the effective width of the tunnel junctions; these results should stimulate a detailed revision of our understanding of FTJs.

## Experimental Section

*Sample Fabrication*: BTO(2–4 nm)/LSMO(30 nm) bilayers were epitaxially grown by pulsed laser deposition on (001)-oriented $SrTiO_3$ (STO) single crystal substrates in a single process.[34,35] Top Pt layers were deposited ex situ by sputtering. Junctions were fabricated into a cross-strip geometry using photolithography and ion milling (see Supporting Information, SI-1). On each sample we fabricated 36 junctions with area $A$ ranging from 4 to 900 μm$^2$.

*Electric Characterization*: Measurements were performed in two-points geometry with a Keithley SourceMeter 2611. Positive bias indicates $V > 0$ applied to the top (Pt/Au) electrode. FE poling was achieved by applying increasing/decreasing poling voltage pulses ($V_{write}$). $I$–$V$ characteristics were measured by using triangular $V(t)$ pulses. Resistances reported here are resistance values ($R = V/I$) at $V = 100$ mV. Tunnel electroresistance (TER) is defined as: TER = $(R_{OFF} - R_{ON})/R_{ON}$, where $R_{OFF}/R_{ON}$ are the junction resistance in the high/low resistance state (see Supporting Information, SI-3).

*Capacitance Measurements*: Measurements were performed at various frequencies (10 kHz–1 MHz) under a driving AC-field of 100 mV and variable $V_{bias}$ by using a HP 4192LF (Agilent Co.) impedance analyzer. $V_{bias} > 0$ corresponds to positive voltage applied to the top (Pt/Au) electrode.

*Ferroelectric Characterization*: FE properties of 2, 3, and 4 nm thick BTO layers were examined at room-temperature and in $N_2$ flow by piezoresponse measurements using a Nanoscope V set-up (Bruker), using CrPt coated cantilevers (≈40 N m$^{-1}$) at an excitation frequency of 35 kHz and AC voltage of 1.5 V (peak-to-peak) and Stanford Research SR830 external lock-in amplifiers. DC poling was performed with CrPt tips by applying a voltage between −3 V and +3.5 V to the bottom electrode (LSMO) while the tip is grounded.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

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