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A comparison of modeling approaches for current transport in polysilicon-channel nanowire and macaroni GAA MOSFETs

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Abstract
In this paper, we compare quantitatively the results obtained from the numerical simulation of current transport in polysilicon-channel MOSFETs under different modeling assumptions typically adopted to reproduce the basic physics of the devices, including the effective medium approximation and the description of polysilicon as the haphazard ensemble of monocrystalline silicon grains separated by highly defective grain boundaries. In the latter case, both pure drift-diffusion transport and a mix of intra-grain drift-diffusion and inter-grain thermionic emission are considered. Interest is focused on cylindrical nanowire and macaroni gate-all-around structures, due to their relevance in the field of 3-Dimensional NAND Flash memories, focusing not only on the average behavior but also on the variability in the electrical characteristics of the devices.

Keywords Polysilicon · Nanowire MOSFETs · Macaroni MOSFETs · Semiconductor device modeling

1 Introduction

The recent transition of NAND Flash arrays from planar to 3-dimensional (3-D) [1, 2] has boosted interest towards deca-nanometer polysilicon-channel MOSFETs. The mainstream technological solution to vertically stack many layers of memory cells in 3-D NAND Flash arrays, in fact, is the so-called punch-and-plug process and allows to create strings of cylindrical gate-all-around (GAA) memory transistors in series connection along a silicon channel with polycrystalline structure [3–6]. The presence of grains separated by highly defective grain boundaries in the polysilicon channel of the strings introduces some relevant issues in the operation and in the reliability of the array. Among them, it is worth mentioning (i) a severe limitation to the string current, especially at low temperature [7]; (ii) transient instabilities in the string current, due to the dependence of the average occupancy of the traps at the grain boundaries on the bias history of the string [8–10]; (iii) variability in the cell threshold voltage (V_T) and in its temperature dependence, due to the haphazardness in the configuration of the polysilicon grains [11, 12]; (iv) the worsening of the amplitude statistics of random telegraph noise (RTN) affecting cell V_T, due to the contribution to percolative channel conduction of the nonuniform inversion of the intra-grain and inter-grain regions [13–19]. The adoption of a thin annular channel instead of a full nanowire was demonstrated to be a successful solution to mitigate some of these issues [20, 21]. In that case, which is commonly referred to as macaroni channel, the inner part of the annular region is filled up with silicon oxide and the thickness of the polysilicon region is decreased down to the $10 \div 20$ nm range, taking benefits from the thin-body device electrostatics.

In order to optimize the performance and the reliability of 3-D NAND Flash arrays from the standpoint of polysilicon-related issues, accurate models able to reproduce the polysilicon physics in deca-nanometer MOSFETs are mandatory. In this regard, it is worth mentioning that quite different approaches have been proposed in the literature to address polysilicon-channel transistors. In the simplest case, polysilicon is treated under the effective medium approximation, i.e., by neglecting its granular nature and introducing a spatially uniform distribution of traps in the volume of the material [22–25]. This approach is assumed to be valid when the nonuniformities in device electrostatics arising from the localized nature of the traps at the grain boundaries are negligible. In a more physics-based approach, the polysilicon channel is considered as the haphazard ensemble of

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monocrystalline grains separated by highly defective grain boundaries. In this latter case, pure drift-diffusion transport [26–28] or a mix of intra-grain drift-diffusion and inter-grain thermionic emission have been considered [12, 18, 29, 30]. In the presence of variety of approaches, a clear assessment of the impact of different modeling assumptions on the results for the electrical characteristics of the devices has not been provided so far. In this paper, which extends our preliminary work presented in [31], we provide such an assessment, focusing on both the average value and the variability in the electrical characteristics of polysilicon-channel GAA nanowire and macaroni MOSFETs.

2 Device structures and models

Figure 1 shows a cross section of the two 3-D polysilicon-channel cylindrical GAA devices investigated in this work. Both devices feature a channel outer radius $r_c = 25$ nm, a silicon dioxide gate insulator with thickness $t_{ox} = 12.5$ nm and a metal gate (work function $\phi_m = 4.5$ eV). The inner radius of the channel, corresponding to the radius r_f of the filler oxide, was varied between 0 (nanowire channel) and 20 nm. In (a), a single and very long gate region (length $L_G = 950$ nm) was introduced to drive channel inversion. The long gate length allows not only to avoid any short-channel effect in device operation but also to average along the channel direction the nonuniformities coming from the haphazardness in the configuration of the polysilicon grains. Note that this structure can be considered representative of a 3-D NAND string with all of its word lines driven by the same voltage. In case (b) of Fig. 1, instead, channel inversion is driven by three gates with length equal to 100 nm, 30 nm and 100 nm, with spacing regions with length $L_s = 30$ nm in between them. By biasing the lateral gates with a pass voltage V_{pass} and sweeping the voltage applied to the central gate, this structure can be considered representative of a 3-D NAND string under read conditions and allows to investigate the variability in the read outcome due to the random configuration of polysilicon grains in the channel. Both in cases (a) and (b) of Fig. 1, the channel was doped with a donor concentration N_D equal to 10^{15} cm^{-3} in the inner regions of the string and 10^{20} cm^{-3} beyond the upper and lower gate edges.

The device structures shown in Fig. 1 were implemented in a commercial device simulator [32]. In order to reproduce the polycrystalline nature of the silicon channel, two different approaches were used. In the first, the channel was considered as monocrystalline silicon with the volumetric acceptor trap density adopted in [23] and is reported in Fig. 2. This latter density was uniformly introduced in the channel volume to account for the high defect density that is typically present in polysilicon, neglecting its localization at the grain boundaries of the material (effective medium approximation). In the second approach, the channel was divided into Voronoi volumes of average size $\phi_g = 40$ nm separated by surfaces representing the polysilicon grain boundaries [11, 12, 30]. At these surfaces, a planar acceptor

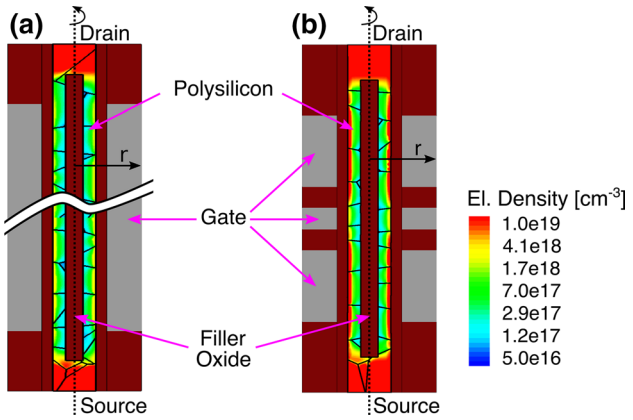

Fig. 1 Schematic cross section of the 3-D polysilicon-channel cylindrical GAA devices investigated in this work: **a** single-gate structure used in Sect. 3.1 to address the average polysilicon current and **b** three-gate structure used in Sect. 3.2 to address current variability. The color scale represents the electron concentration in the polysilicon channel at $V_G = 1.5$ V

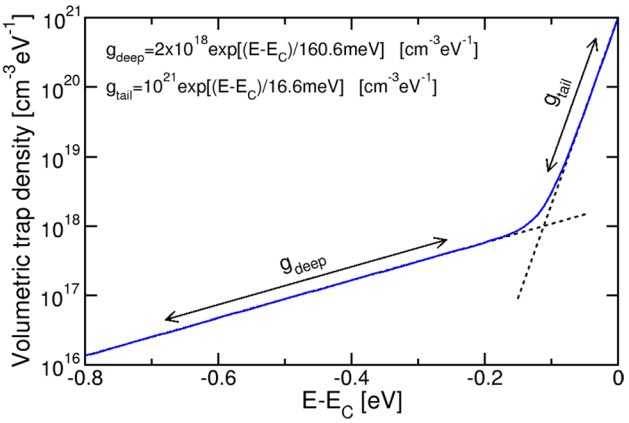

Fig. 2 Volumetric acceptor trap density assumed when modeling polysilicon under the effective medium approximation [23]. The distribution features a double-exponential behavior in energy, with tail and deep states (see the formulas in the inset). E_C is the conduction band edge, E is energy

trap density calibrated to give the same total number of traps in the channel resulting from the effective medium approximation was introduced.

The device drain current versus gate voltage (I_D–V_G) transcharacteristic was simulated for a drain voltage $V_D = 0.5$ V, assuming pure drift-diffusion transport (effective medium approximation and Voronoi grains) or mixed intra-grain drift-diffusion and inter-grain thermionic emission (Voronoi grains only, see [11, 12] for details). A constant electron mobility $\mu_n = 100\,\mathrm{cm}^2/\mathrm{Vs}$ [24, 25] and a Richardson velocity $v_r = 2\sqrt{kT/2\pi m_n}$ [33] were adopted, respectively, for the drift-diffusion process and for thermionic emission. As a final remark, note that quantum corrections to the electrostatics of the simulated devices were verified to have a negligible impact on the results presented in this work. For the sake of simplicity, then, the results presented here will not include these corrections.

3 Simulation results

3.1 Average polysilicon current

Figure 3 shows the simulated I_D–V_G curve of the device in Fig. 1a as resulting from different polysilicon models described in the previous section, at room temperature (RT) and for different filler oxide radii r_f. Similarly to what shown in [31] for nanowire channels, relevant discrepancies appear among the predictions of different polysilicon models in the on-state regime, while negligible mismatches among the models are present in the subthreshold regime. This can be explained by considering that in the subthreshold regime the low free-electron concentration in the intra-grain regions and the low trapped-electron concentration at the grain boundaries give rise to weak nonuniformities in channel electrostatics. This makes the effective medium approximation a valid description of the polysilicon channel, minimizing the constraints of the localized grain boundaries on current transport. In the on-state regime, instead, strong nonuniformities in channel electrostatics arise from the high free-electron concentration in the intra-grain regions and the strong filling of the acceptor traps at the grain boundaries. In particular, the nonuniformities in channel electrostatics result in high energy barriers at the grain boundaries [11, 12, 31], strongly limiting current transport through the polysilicon channel. This makes the gradual channel approximation less accurate and the activation of thermionic emission at the grain boundaries more relevant for I_D.

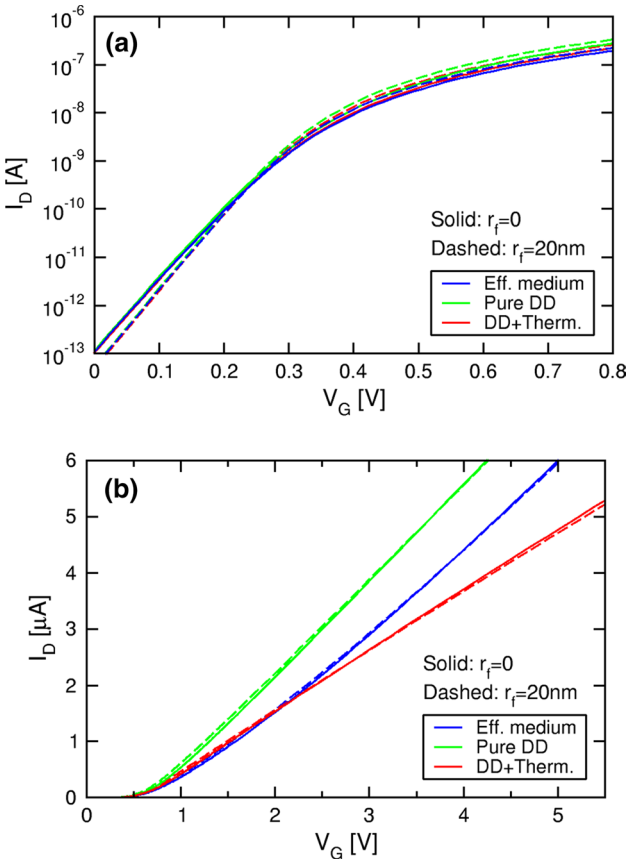

Fig. 3 Simulated I_D–V_G curve of the device in Fig. 1a, as resulting from the different polysilicon models described in Sect. 2, at RT and for different filler oxide radii r_f. Current is shown on a **a** logarithmic and **b** linear scale

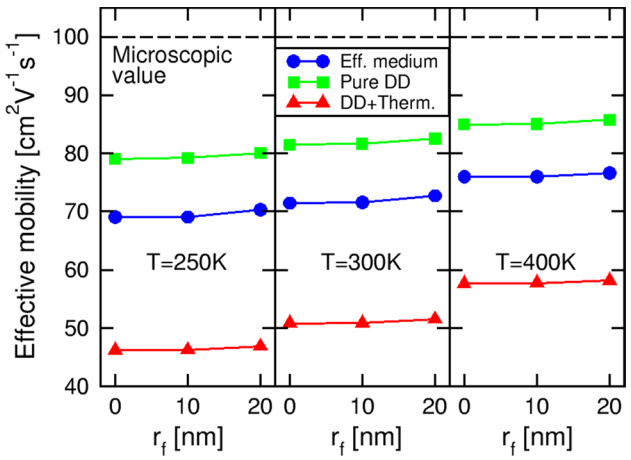

Fig. 4 Effective electron mobility extracted from the simulated I_D–V_G curve of the device in Fig. 1a in the on-state, for different polysilicon models, different temperatures and as a function of r_f

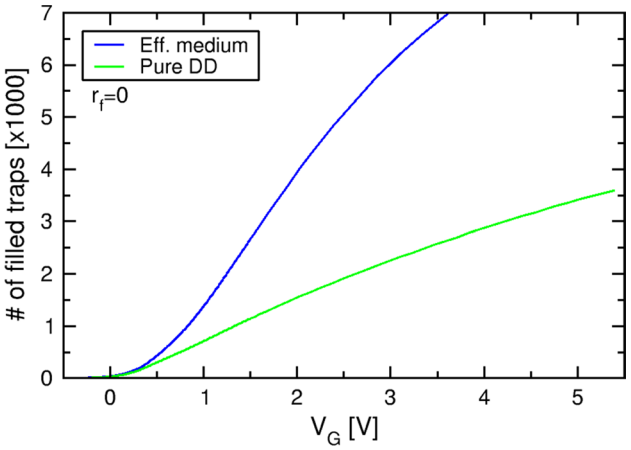

Fig. 5 Average number of filled acceptor traps in the channel of the device in Fig. 1a as a function of V_G, under the effective medium approximation and with Voronoi grains with pure drift-diffusion transport. Results for $r_f = 0$ are reported

It is worth noting that the differences among the predictions of the investigated models in the on-state can be summarized in a different device transconductance and, in turn, in a different effective mobility of electrons in the channel, as shown in Fig. 4. The effective medium approximation provides, in this regard, an effective mobility that is intermediate between the values resulting in the presence of Voronoi grains with pure drift-diffusion transport and with mixed intra-grain drift-diffusion and inter-grain thermionic emission. Referring, first, to the case of pure drift-diffusion simulations, this result can be explained by considering that moving from the effective medium approximation to the Voronoi grains corresponds to clustering the acceptor traps in the channel at localized grain boundaries. This reduces the average number of filled traps in the channel, as shown in Fig. 5, since trap filling is more affected by the electrostatic feedback reducing the local potential when negative charge builds up in the filled acceptor states. As a result of that, I_D is higher and increases more rapidly in the presence of Voronoi grains than with the effective medium approximation. When thermionic emission is activated at the grain boundaries, then, the reduction in the current (Fig. 3) and of the effective electron mobility (Fig. 4) with respect to the effective medium approximation is the direct consequence of a stronger constraint to the electron flow coming from the relatively high energy barriers arising at the grain boundaries due to acceptor trap filling [11, 12, 31]. All these differences among the models must be carefully considered when investigating current transport through polysilicon-channel devices in the on-state regime.

The results in Fig. 3a also reveal that, irrespective of the polysilicon model, the increase in r_f gives rise to an improvement in the subthreshold slope of the device. This is expected since the first proposals of the macaroni channel [20] and can be attributed to the removal of all the acceptor traps in the region of the channel that is replaced with the filler oxide. The removal of these traps, in fact, reduces the amount of spurious fixed negative charge that is present in the region of the device at radii less than r_c as the gate voltage is increased. This leads to a more rapid increase in the free electron density in the channel and to a steeper rise of I_D in the subthreshold regime. On the other hand, a weak dependence of I_D on r_f is observed in the on-state regime. This is attributed to the fact that (i) for the adopted trap density in the polysilicon channel the change of device V_T is rather small (see Fig. 3) and (ii) once strong inversion is reached, I_D depends mainly on the electron concentration at the outer surface of the channel, whose growth is weakly affected by the removal of the acceptor traps at radii less than r_f.

As a final remark, note that the increase in temperature results in the increase in device current in the on-state, but qualitatively preserving all the previously discussed trends, as shown in Fig. 6. The current increase with temperature in the on-state is a typical signature of polysilicon conduction [7, 25, 26] and is due both to the reduction in trap occupancy and to the enhancement of thermionic emission at the grain boundaries [12]. This effect results in the increase in the

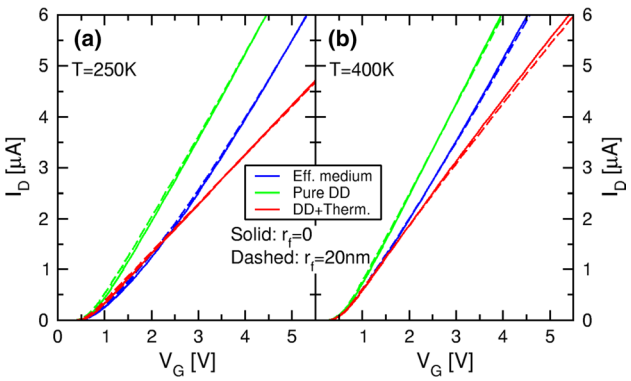

Fig. 6 Same as in Fig. 3b, but at **a** $T = 250$ K and **b** $T = 400$ K

electron effective mobility with temperature, with a stronger growth in the case inter-grain thermionic emission is activated, as shown in Fig. 4.

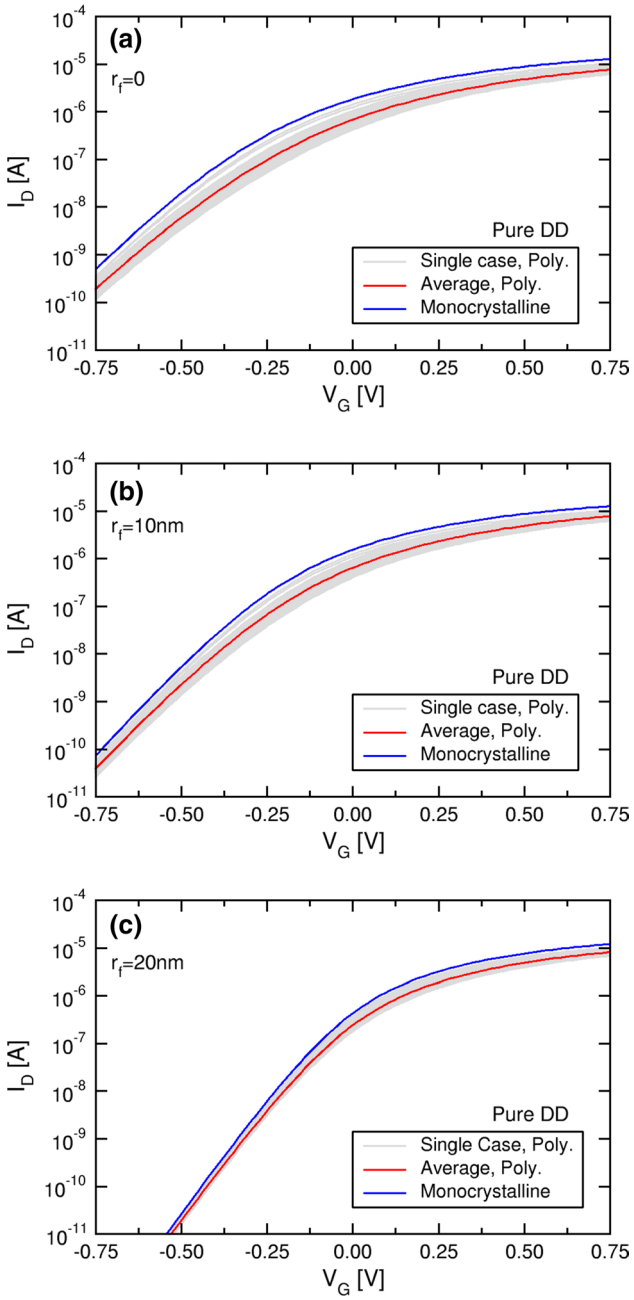

Fig. 7 Simulated I_D–V_G curves (gray lines) of the device in Fig. 1b for different randomly generated configurations of the polysilicon grains in the channel, at RT, with pure DD transport and for r_f equal to **a** 0, **b** 10 nm and **c** 20 nm. The average curve resulting from about 100 Monte Carlo simulations is also highlighted (red lines) for each r_f, along with the curve obtained in the case of monocrystalline silicon (blue lines) (Color figure online)

3.2 Current variability

In order to investigate the variability in the channel current coming from the haphazardness in the configuration of the polysilicon grains, we calculated I_D when sweeping the voltage applied to the central gate of the device structure in Fig. 1b, with lateral gates kept at a constant $V_{pass} = 7$ V. This voltage scheme makes the lateral transistors operate as pass transistors. This means that I_D is mainly limited by the portion of the channel under (or next to) the central gate up to currents making the voltage drop over the remaining part of the channel relevant with respect to V_D. This solution allows, on the one hand, to investigate the variability in the current through a short region of polysilicon comparable to the grain size and, on the other hand, to keep the focus on the read operation of a cell in a 3-D NAND string. In the variability analysis, the I_D–V_G curve was simulated for about 100 randomly generated Voronoi configurations of the polysilicon channel.

Figure 7 shows the results obtained at RT in the case of r_f equal to (a) 0, (b) 10 nm and (c) 20 nm, in the case of pure drift-diffusion transport through the channel. The variability in I_D arising from the polycrystalline silicon channel is clearly evident in all cases. Along with that, the figures also reveal that the increase in r_f gives rise to a rightward shift of the average I_D–V_G curve of the devices (see the red lines) and to an enhancement of the subthreshold slope of this curve. These latter trends appear also in the case of monocrystalline silicon channel (blue lines) and are attributed to a stronger electrostatic control of the central gate over the silicon region under it when r_f is increased. Note, in fact, that the lateral gates biased at V_{pass} may significantly contribute to the increase in the electrostatic potential and of the electron concentration in the deep silicon region under the

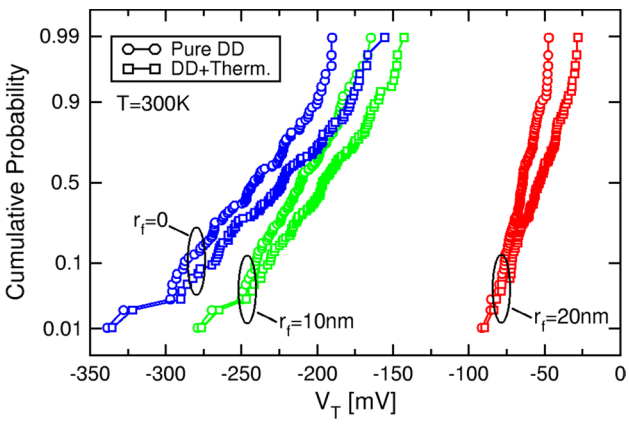

Fig. 8 Cumulative distributions of V_T obtained at RT for different r_f, with pure drift-diffusion transport and with mixed intra-grain drift-diffusion and inter-grain thermionic emission

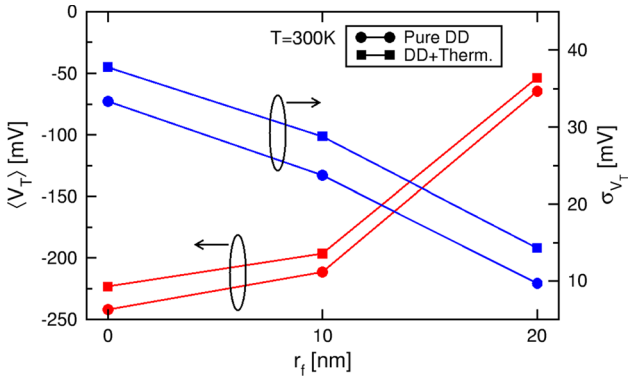

Fig. 9 $\langle V_T \rangle$ and σ_{V_T} as a function of r_f, at RT

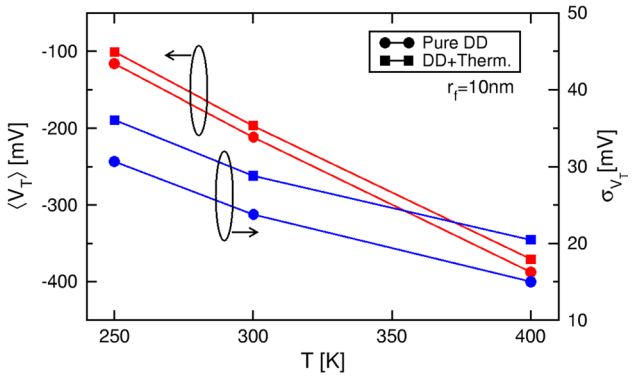

Fig. 10 $\langle V_T \rangle$ and σ_{V_T} as a function of temperature, for $r_f = 10$ nm

central gate when r_f is small, creating a sort of short-channel effect impacting the electrostatics of the central transistor. This effect makes the impact of r_f on the I_D–V_G curve much stronger than that observed in the previous section on the structure of Fig. 1a, resulting in a relevant degradation of the subthreshold slope of the devices and in a relevant reduction in their V_T for small r_f. In the case of a polysilicon channel, this effect comes along with the change of the subthreshold slope with r_f discussed with Fig. 3a.

In order to quantify the statistical spread in polysilicon conduction, we extracted a constant current V_T at $I_D = 100$ nA from the curves in Fig. 7 and from similar curves calculated with inter-grain thermionic emission on. The obtained statistical distributions of V_T are reported in Fig. 8. Results reveal that not only the average value ($\langle V_T \rangle$) but also the spread (σ_{V_T}) of the V_T distribution changes with r_f. These trends are highlighted in Fig. 9, where the benefits expected from the increase in r_f in terms of variability [20] are clearly evident. Besides, the figure also reveals that the activation of thermionic emission at the grain boundaries gives rise to a higher σ_{V_T}. Since V_T is extracted at an I_D not far from the on-state regime, this is attributed to the more severe limitation to current transport introduced by the polysilicon grain boundaries when thermionic emission is on, making the haphazardness in their number and position more relevant for the current flow. Finally, Fig. 10 highlights that the increase in temperature results in a reduction in both $\langle V_T \rangle$ and σ_{V_T}. While the reduction in $\langle V_T \rangle$ with temperature is a well-known dependence affecting also monocrystalline MOSFETs, the reduction in σ_{V_T} is strictly related to the dependence on temperature of the nonuniformities in channel inversion arising from the highly defective grain boundaries. In particular, the increase in temperature smooths the nonuniformities in channel inversion induced by the grain boundaries, making their configuration less relevant for current transport and leading, in turn, to the decrease in σ_{V_T} highlighted in Fig. 10. The reduction in the nonuniformities in channel electrostatics with temperature arises both from the reduction in trap occupancy at the grain boundaries [12] and to a less severe constraint of thermionic emission. All of these points must be carefully considered when addressing the variety of phenomena affected by percolative channel conduction, such as RTN [7, 13, 19, 34–36] and charge detrapping [37–40], when performing spectroscopic analyses of oxide traps based on local tunneling currents [41–44] and when addressing the impact of localized electron storage in charge trap layers on nonuniform channel inversion [45].

4 Conclusions

In this paper, we have shown that the models and approximations typically adopted to reproduce the physics of polysilicon channels in a simulation framework may lead to non-negligible differences in the results, both in terms of average current and of current variability. This has to be carefully considered when investigating technology performance and reliability by means of TCAD tools. Besides, the analyses as a function of the filler oxide radius of cylindrical GAA transistors clearly confirmed the benefits coming from the adoption of a macaroni over a nanowire polysilicon channel, representing a cornerstone for the design of 3-D NAND Flash arrays.

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References

1. Monzio Compagnoni, C., Goda, A., Spinelli, A.S., Feeley, P., Lacaita, A.L., Visconti, A.: Reviewing the evolution of the NAND Flash technology. Proc. IEEE **105**, 1609–1633 (2017). https://doi.org/10.1109/JPROC.2017.2665781
2. Monzio Compagnoni, C., Spinelli, A.S.: Reliability of NAND Flash arrays: a review of what the 2-D-to-3-D transition meant. IEEE Trans. Electron. Devices **66**, 4504–4516 (2019). https://doi.org/10.1109/TED.2019.2917785
3. Tanaka, H., Kido, M., Yahashi, K., Oomura, M., Katsumata, R., Kito, M., Fukuzumi, Y., Sato, M., Nagata, Y., Matsuoka, Y., Iwata, Y., Aochi, H., Nitayama, A.: Bit cost scalable technology with punch and plug process for ultra high density Flash memory. In: VLSI Symp Tech Dig, pp. 14–15 (2007). https://doi.org/10.1109/VLSIT.2007.4339708
4. Katsumata, R., Kito, M., Fukuzumi, Y., Kido, M., Tanaka, H., Komori, Y., Ishiduki, M., Matsunami, J., Fujiwara, T., Nagata, Y., Zhang, L., Iwata, Y., Kirisawa, R., Aochi, H., Nitayama, A.: Pipe-shaped BiCS Flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices. In: VLSI Symp Tech Dig, pp. 136–137 (2009)
5. Jang, J., Kim, H.S., Cho, W., Cho, H., Kim, J., Shim, S.I., Jang, Y., Jeong, J.H., Son, B.K., Kim, D.W., Kim, K., Shim, J.J., Lim, J.S., Kim, K.H., Yi, S.Y., Lim, J.Y., Chung, D., Moon, H.C., Hwang, S., Lee, J.W., Son, Y.H., Chung, U.I., Lee, W.S.: Vertical cell array using TCAT (Terabit Cell Array Transistor) technology for ultra high density NAND flash memory. In: VLSI Symp Tech Dig, pp. 192–193 (2009)
6. Parat, K., Dennison, C.: A floating gate based 3-D NAND technology with CMOS under array. In: IEDM Tech Dig, pp. 48–51 (2015). https://doi.org/10.1109/IEDM.2015.7409618
7. Resnati, D., Goda, A., Nicosia, G., Miccoli, C., Spinelli, A.S., Monzio Compagnoni, C.: Temperature effects in NAND Flash memories: a comparison between 2-D and 3-D arrays. IEEE Electron. Device Lett. **38**, 461–464 (2017). https://doi.org/10.1109/LED.2017.2675160
8. Tsai, W.J., Lin, W.L., Cheng, C.C., Ku, S.H., Chou, Y.L., Liu, L., Hwang, S.W., Lu, T.C., Chen, K.C., Wang, T., Lu, C.Y.: Polycrystalline-silicon channel trap induced transient read instability in a 3D NAND Flash cell string. In: IEDM Tech Dig, pp. 288–291 (2016). https://doi.org/10.1109/IEDM.2016.7838395
9. Kang, H.J., Jeong, M.K., Joe, S.M., Seo, J.H., Park, S.K., Jin, S.H., Park, B.G., Lee, J.H.: Effect of traps on transient bit-line current behavior in word-line stacked NAND Flash memory with poly-Si body. In: VLSI Symp Tech Dig, pp. 1–2 (2014). https://doi.org/10.1109/VLSIT.2014.6894348
10. Zambelli, C., Micheloni, R., Scommegna, S., Olivo, P.: First evidence of temporary read errors in TLC 3-D NAND Flash memories exiting from an idle state. IEEE J. Electron. Devices Soc. **8**, 99–104 (2020). https://doi.org/10.1109/JEDS.2020.2965648
11. Resnati, D., Mannara, A., Nicosia, G., Paolucci, G.M., Tessariol, P., Lacaita, A.L., Spinelli, A.S., Monzio Compagnoni, C.: Temperature activation of the string current and its variability in 3-D NAND Flash arrays. In: IEDM Tech Dig, pp. 103–106 (2017). https://doi.org/10.1109/IEDM.2017.8268329
12. Resnati, D., Mannara, A., Nicosia, G., Paolucci, G.M., Tessariol, P., Spinelli, A.S., Lacaita, A.L., Monzio Compagnoni, C.: Characterization and modeling of temperature effects in 3-D NAND Flash arrays—part I: polysilicon-induced variability. IEEE Trans. Electron. Devices **65**, 3199–3206 (2018). https://doi.org/10.1109/TED.2018.2838524
13. Ghetti, A., Monzio Compagnoni, C., Spinelli, A.S., Visconti, A.: Comprehensive analysis of random telegraph noise instability and its scaling in deca-nanometer Flash memories. IEEE Trans. Electron. Devices **56**, 1746–1752 (2009). https://doi.org/10.1109/TED.2009.2024031
14. Monzio Compagnoni, C., Gusmeroli, R., Spinelli, A.S., Lacaita, A.L., Bonanomi, M., Visconti, A.: Statistical model for random telegraph noise in Flash memories. IEEE Trans. Electron. Devices **55**, 388–395 (2008). https://doi.org/10.1109/TED.2007.910605
15. Goda, A., Miccoli, C., Monzio Compagnoni, C.: Time dependent threshold-voltage fluctuations in NAND Flash memories: from basic physics to impact on array operation. In: IEDM Tech Dig, pp. 374–377 (2015). https://doi.org/10.1109/IEDM.2015.7409699
16. Spinelli, A.S., Monzio Compagnoni, C., Lacaita, A.L.: Reliability of NAND Flash memories: planar cells and emerging issues in 3D devices. Computers **6**, 1–55 (2017). https://doi.org/10.3390/computers6020016
17. Nicosia, G., Mannara, A., Resnati, D., Paolucci, G.M., Tessariol, P., Lacaita, A.L., Spinelli, A.S., Goda, A., Monzio Compagnoni, C.: Impact of temperature on the amplitude of RTN fluctuations in 3-D NAND Flash cells. In: IEDM Tech Dig, pp. 521–524 (2017). https://doi.org/10.1109/IEDM.2017.8268434
18. Nicosia, G., Mannara, A., Resnati, D., Paolucci, G.M., Tessariol, P., Spinelli, A.S., Lacaita, A.L., Goda, A., Monzio Compagnoni, C.: Characterization and modeling of temperature effects in 3-D NAND Flash arrays—part II: random telegraph noise. IEEE Trans. Electron. Devices **65**, 3207–3213 (2018). https://doi.org/10.1109/TED.2018.2839904
19. Nicosia, G., Goda, A., Spinelli, A.S., Monzio Compagnoni, C.: Impact of cycling on random telegraph noise in 3-D NAND Flash arrays. IEEE Electron. Device Lett. **39**, 1175–1178 (2018). https://doi.org/10.1109/LED.2018.2847341
20. Fukuzumi, Y., Katsumata, R., Kito, M., Kido, M., Sato, M., Tanaka, H., Nagata, Y., Matsuoka, Y., Iwata, Y., Aochi, H., Nitayama, A.: Optimal integration and characteristics of vertical array devices for ultra-high density, bit-cost scalable Flash memory. In: IEDM Tech Dig, pp. 449–452 (2007). https://doi.org/10.1109/IEDM.2007.4418970
21. Ishiduki, M., Fukuzumi, Y., Katsumata, R., Kito, M., Kido, M., Tanaka, H., Komori, Y., Nagata, Y., Fujiwara, T., Maeda, T., Mikajiri, Y., Oota, S., Honda, M., Iwata, Y., Kirisawa, R., Aochi, H., Nitayama, A.: Optimal device structure for pipe-shaped BiCS Flash memory for ultra high density storage device with excellent performance and reliability. In: IEDM Tech Dig, pp. 27.3.1–27.3.4 (2009)
22. Hack, M., Shaw, J.G., Lecomber, P.G., Willums, M.: Numerical simulations of amorphous and polycrystalline silicon thin-film transistors. Jpn. J. Appl. Phys. **29**, 2360–2362 (1990). https://doi.org/10.1143/JJAP.29.L2360
23. Jacunski, M.D., Shur, M.S., Hack, M.: Threshold voltage, field effect mobility, and gate-to-channel capacitance in polysilicon TFT's. IEEE Trans. Electron. Devices **43**, 1433–1440 (1996). https://doi.org/10.1109/16.535329
24. Valdinoci, M., Colalongo, L., Baccarani, G., Pecora, A., Policicchio, I., Fortunato, G., Plais, F., Legagneux, P., Reita, C., Pribat, D.: Analysis of electrical characteristics of polycrystalline silicon thin-film transistors under static and dynamic conditions. Solid State Electron. **41**, 1363–1369 (1997). https://doi.org/10.1016/S0038-1101(97)00130-5
25. Han, Z., Wang, M.: Analysis of the Meyer-Neldel rule based on a temperature-dependent model for thin-film transistors. IEEE Trans. Electron. Devices **64**, 145–152 (2017). https://doi.org/10.1109/TED.2016.2623764

26. Li, T.S., Lin, P.S.: On the pseudo-subthreshold characteristics of polycrystalline-silicon thin-film transistors with large grain size. IEEE Electron. Device Lett. **14**, 240–242 (1993). https://doi.org/10.1109/55.215180
27. Chou, T.K.A., Kanicki, J.: Two-dimensional numerical simulation of solid-phase-crystallized polysilicon thin-film transistor characteristics. Jpn. J. Appl. Phys. **38**, 2251–2255 (1999). https://doi.org/10.1143/JJAP.38.2251
28. Degraeve, R., Clima, S., Putcha, V., Kaczer, B., Roussel, P., Linten, D., Groeseneken, G., Arreghini, A., Karner, M., Kernstock, C., Stanojevic, Z., Van den bosch, G., Van Houdt, J., Furnemont, A., Thean, A.: Statistical poly-Si grain boundary model with discrete charging defects and its 2D and 3D implementation for vertical 3D NAND channels. In: IEDM Tech Dig, pp. 121–124 (2015). https://doi.org/10.1109/IEDM.2015.7409636
29. Yamada, S., Yokoyama, S., Koyanagi, M.: Two-dimensional device simulation for avalanche induced short channel effect in poly-Si TFT. In: IEDM Tech Dig, pp. 859–862 (1990). https://doi.org/10.1109/IEDM.1990.237027
30. Yang, C.W., Su, P.: Simulation and investigation of random grain-boundary-induced variabilities for stackable NAND Flash using 3-D voronoi grain patterns. IEEE Trans. Electron. Devices **61**, 1211–1214 (2014). https://doi.org/10.1109/TED.2014.2308951
31. Mannara, A., Spinelli, A.S., Lacaita, A.L., Monzio Compagnoni, C.: Current transport in polysilicon-channel GAA MOSFETs: A modeling perspective. In: Proc ESSDERC, pp. 222–225 (2019). https://doi.org/10.1109/ESSDERC.2019.8901786
32. Synopsys, Zurich, Switzerland: Sentaurus device user guide, M-2016.12 edn. (2016)
33. Schroeder, D.: Modelling of Interface Carrier Transport for Device Simulation. Springer, Wien (1994)
34. Ghetti, A., Amoroso, S.M., Mauri, A., Monzio Compagnoni, C.: Impact of nonuniform doping on random telegraph noise in Flash memory devices. IEEE Trans. Electron. Devices **59**, 309–315 (2012). https://doi.org/10.1109/TED.2011.2175399
35. Amoroso, S.M., Monzio Compagnoni, C., Ghetti, A., Gerrer, L., Spinelli, A.S., Lacaita, A.L., Asenov, A.: Investigation of the RTN distribution of nanoscale MOS devices from subthreshold to on-state. IEEE Electron. Device Lett. **34**, 683–685 (2013). https://doi.org/10.1109/LED.2013.2250477
36. Nicosia, G., Goda, A., Spinelli, A.S., Monzio Compagnoni, C.: Investigation of the temperature dependence of random telegraph noise fluctuations in nanoscale polysilicon-channel 3-D Flash cells. Solid State Electron. **151**, 18–22 (2019). https://doi.org/10.1016/j.sse.2018.10.010
37. Paolucci, G.M., Monzio Compagnoni, C., Miccoli, C., Spinelli, A.S., Lacaita, A.L., Visconti, A.: Revisiting charge trapping/detrapping in Flash memories from a discrete and statistical standpoint—part I: V_T instabilities. IEEE Trans. Electron. Devices **61**, 2802–2810 (2014). https://doi.org/10.1109/TED.2014.2327661
38. Paolucci, G.M., Monzio Compagnoni, C., Miccoli, C., Spinelli, A.S., Lacaita, A.L., Visconti, A.: Revisiting charge trapping/detrapping in Flash memories from a discrete and statistical standpoint—part II: on-field operation and distributed-cycling effects. IEEE Trans. Electron. Devices **61**, 2811–2819 (2014). https://doi.org/10.1109/TED.2014.2327149
39. Resnati, D., Nicosia, G., Paolucci, G.M., Visconti, A., Monzio Compagnoni, C.: Cycling-induced charge trapping/detrapping in Flash memories—part I: experimental evidence. IEEE Trans. Electron. Devices **63**, 4753–4760 (2016). https://doi.org/10.1109/TED.2016.2617888
40. Resnati, D., Nicosia, G., Paolucci, G.M., Visconti, A., Monzio Compagnoni, C.: Cycling-induced charge trapping/detrapping in Flash memories—part II: modeling. IEEE Trans. Electron. Devices **63**, 4761–4768 (2016). https://doi.org/10.1109/TED.2016.2617890
41. Adamu-Lema, F., Monzio Compagnoni, C., Amoroso, S.M., Castellani, N., Gerrer, L., Markov, S., Spinelli, A.S., Lacaita, A.L., Asenov, A.: Accuracy and issues of the spectroscopic analysis of RTN traps in nanoscale MOSFETs. IEEE Trans. Electron. Devices **60**, 833–839 (2013). https://doi.org/10.1109/TED.2012.2230004
42. Castellani, N., Monzio Compagnoni, C., Mauri, A., Spinelli, A.S., Lacaita, A.L.: Three-dimensional electrostatics- and atomistic doping-induced variability of RTN time constants in nanoscale MOS devices—part I: physical investigation. IEEE Trans. Electron Devices **59**, 2488–2494 (2012). https://doi.org/10.1109/TED.2012.2202910
43. Monzio Compagnoni, C., Castellani, N., Mauri, A., Spinelli, A.S., Lacaita, A.L.: Three-dimensional electrostatics- and atomistic doping-induced variability of RTN time constants in nanoscale MOS devices—part II: spectroscopic implications. IEEE Trans. Electron- Devices **59**, 2495–2500 (2012). https://doi.org/10.1109/TED.2012.2203412
44. Palestri, P., Barin, N., Brunel, D., Busseret, C., Campera, A., Childs, P.A., Driussi, F., Fiegna, C., Fiori, G., Gusmeroli, R., Iannaccone, G., Karner, M., Kosina, H., Lacaita, A.L., Langer, E., Majkusiak, B., Monzio Compagnoni, C., Poncet, A., Sangiorgi, E., Selmi, L., Spinelli, A.S., Walczak, J.: Comparison of modeling approaches for the capacitance-voltage and current-voltage characteristics of advanced gate stacks. IEEE Trans. Electron. Devices **54**, 106–114 (2007). https://doi.org/10.1109/TED.2006.887226
45. Mauri, A., Monzio Compagnoni, C., Amoroso, S.M., Maconi, A., Ghetti, A., Spinelli, A.S., Lacaita, A.L.: Comprehensive investigation of statistical effects in nitride memories—part I: physics-based modeling. IEEE Trans. Electron. Devices **57**, 2116–2123 (2010). https://doi.org/10.1109/TED.2010.2054472