Proceedings of the
2020 Design, Automation & Test in Europe Conference & Exhibition (DATE 2020)

09 to 13 March, 2020

Grenoble, France

Editors

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Dear Colleague,

We proudly present the Advance Programme of **DATE 2020**. DATE combines the world's favourite electronic systems design and test conference with an international exhibition for electronic design, automation and test, from system-level hardware and software implementation right down to integrated circuit design.

The DATE conference will take place from 9 to 13 March 2020 at the AlpExpo congress centre in Grenoble, France. Grenoble has a great number of assets such as its manufacturing companies, renowned higher-education institutions and internationally-recognised research laboratories, that make it one of the largest technology and research centres in Europe. Grenoble is the key European semiconductor site with more than 200 companies in micro/nano technologies and embedded software, including 100 start-ups and 90 SMEs, offering the working environment for 38,000 people.

Out of a total of 748 paper submissions received, a large share (39%) is coming from authors in Europe, 27% of submissions are from the Americas, 33% from Asia, and 1% from the rest of the world. Submissions involved more than 2400 authors from 45 different countries, a distribution that clearly demonstrates DATE's international character, global reach and impact.

For the 23rd year in a row, DATE has prepared an exciting technical programme. With the help of the 328 members of the Technical Programme Committee, who carried out 3014 reviews (mostly four reviews per submission), 194papers (26%) were finally selected for regular presentation and 82 additional ones (cumulatively 37%, including all papers) for interactive presentation.

On the first day of the DATE week, **six in-depth technical tutorials** on the main topics of DATE as well as **one industry hands-on tutorial** will be given by leading experts in their respective fields. The topics cover Early Reliability Analysis in Microprocessor Systems, AI Chip Technologies and DFT Methodologies, Data Analytics for Scalable Computing Systems Design, Security in the Post-Quantum Era, HW/SW code sign of Heterogeneous Parallel dedicated Systems, Evolutionary computing for EDA, and the Deployment of deep learning networks on FPGA (Mathworks).

The first day of the conference will close with the **PhD Forum**, where 32 selected students who have completed their PhD thesis or are about to, can showcase their work to the academia and the industrial community.

During the Opening Ceremony on Tuesday, **plenary keynote lectures** will be given by Philippe Magarshack, Corporate Vice President at ST Microelectronics, and Luca Benini, chair of digital Circuits and Systems at ETH Zurich and Professor at University of Bologna. On the same day, the **Executive Track** offers hot-topic presentations given by executive speakers from companies leading the design and automation industry. Furthermore, a talk by Catherine Schuman from Oak Ridge National Laboratory, will give an overview of the history of neuromorphic computing and will present the current state of research in the field.

The main conference programme from Tuesday to Thursday includes 55 technical sessions organized in parallel tracks from the four areas
D – Design Methods & Tools
A – Application Design
T – Test and Dependability
E – Embedded and Cyber-physical Systems

and from several special sessions on Hot Topics, such as Memories for Emerging Applications, Architectures for Emerging Technologies (Quantum Computing, Edge Computing, Neural Algorithms, In-Memory Computing, Bio-Inspired Adaptive Hardware), Hardware Security, 3D Integration and Logic Reasoning for Functional ECO, as well as results and lessons learned from European projects. Additionally, there are numerous Interactive Presentations which are organised into five IP sessions.

Two Special Days in the programme will focus on areas bringing new challenges to the system design community: **Embedded AI and Silicon Photonics**. Each of the Special Days will have a full programme of keynotes, panels, tutorials and technical presentations.

The Special Day on **Embedded Artificial Intelligence** will cover new trends in cognitive algorithms, hardware architectures, software designs, emerging device technologies as well as the application space for deploying AI into edge devices. The topics will include technical areas to enable the realization of embedded artificial intelligence on specialized chips, such as bio-inspired chips, with and without self-learning capabilities, special low-power accelerator chips for aiding in vector/matrix-based computations, convolution and deep-net chips for possible machine learning, cognitive, and perception applications in health, automotive, robotics, or smart cities applications. A particular highlight of the day will be the luncheon keynote given by Jim Tung, who will present Mathworks' vision on how to leverage Embedded Intelligence in Industry.

The Special Day on **Silicon Photonics** will focus on data communication via photonics for both data centre/high-performance computing and optical networks on chip applications. Industrial and academic experts will highlight recent advances on devices and integrated circuits. The sessions will also feature talks on design automation and link-level simulations. Other applications of silicon photonics such as sensing and optical compute will also be discussed. As a highlight of the special day, Joachim Schultze from DZNE will talk about bottlenecks and challenges for HPC in medicinal and genomics research during his luncheon keynote.

A timely Special Initiative "Autonomous Systems Design – Automated Vehicles and beyond" is held on Thursday and Friday, consisting of reviewed and invited papers as well as working sessions.

To inform attendees on commercial and design-related topics, there will be a full programme in the **Exhibition Theatre**, which will combine presentations by exhibiting companies, best-practice reports by industry leaders on their latest design projects and selected conference special sessions. A special industrial keynote will be given by Philippe Quinio, STMicroelectronics.

The conference is complemented by an **exhibition, running for three days (Tuesday – Thursday),** including exhibition booths from companies, and collaborative research initiatives among which, also EU project presentations. The exhibition provides a unique networking opportunity and is the perfect venue for industries to meet University Professors to foster University Programmes and especially for PhD Students to meet future employers.

On Friday, **eight full-day workshops** cover several hot topics from areas like Autonomous Systems Design, Optical/Photonic Interconnects, Computation-In-Memory, Open-Source Design Automation, Stochastic Computing for Neuromorphic Architectures, Hardware Security, Quantum Computing and Imaging Solutions.

For further information, please visit: www.date-conference.com

We wish you an exciting and memorable DATE 2020, a successful exhibition visit and an entertaining DATE party on Wednesday evening.

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T1 Modeling and Mitigation of Defects, Faults, Variability, and Reliability

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T2 Test Generation, TestArchitectures, Design for Test, and Diagnosis

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Keynote Speakers

Title	*The Industrial IoT Microelectronics Revolution*
Speaker	**Philippe Magarshack** STMicroelectronics, France

Abstract

Industrial IoT (IIoT) Systems are now becoming a reality. IIoT is distributed by nature, encompassing many complementary technologies. IIoT systems are composed of sensors, actuators, a means of communication and control units, and are moving into the factories, with the Industry 4.0 generation. In order to operate concurrently, all these IIoT components will require a wide range of technologies, in order to maintain such system-of-systems in a full operational, coherent and secure state. We identify and describe the four key enablers for the Industrial IoT: 1) more powerful and diverse embedded computing, available on ST's latest STM32 microcontrollers and microprocessors, 2) augmented by AI applications at the edge (in the end devices), whose development is becoming enormously simplified by our specialized tools, 3) a wide set of connectivity technology, either with complete System-on-chip, or ready-to-use modules, and 4) a scalable security offer, thanks to either integrated features or dedicated security devices. We conclude with some perspective on the usage of Digital Twins in the IIoT.

Biography

Philippe Magarshackis currently MDG Group Vice President at ST Microelectronics, in charge of Microcontrollers and Digital ICs Group (MDG) Strategic Technology & System Architecture. Magarshack is also President of the Minalogic Collaborative R&D Cluster in Grenoble since June 2014.

In 2012, he was made Vice President in charge of Design Enablement & Services, and was CTO of the Embedded Processing Solutions during 2015. In 2005, Magarshack was appointed Group Vice President and General Manager of Central CAD and Design Solutions at STMicroelectronics' Technology R&D and Manufacturing organization. In 1994, Magarshack joined the Central R&D Group of SGS-THOMSON Microelectronics (now STMicroelectronics), where he held several roles in CAD and Libraries management for advanced integrated-circuit manufacturing processes. From 1985 to 1989, Magarshack worked as a microprocessor designer at AT&T Bell Labs in the USA, after which he joined Thomson-CSF in Grenoble, France, and took responsibility for libraries and ASIC design kits for the military market, until 1994. Philippe graduated with an engineering degree in Physics from EcolePolytechnique, Paris, France, and with an Electronics Engineering degree from EcoleNationaleSupérieure des Télécommunications in Paris, France.

Title	*Open Parallel Ultra-Low Power Platforms for Extreme Edge AI*
Speaker	**Luca Benini** ETHZ, Switzerland

Abstract

Edge Artificial Intelligence is the new megatrend, as privacy concerns and networks bandwidth/latency bottlenecks prevent cloud offloading of sensor analytics functions in many application domains, from autonomous driving to advanced prosthetic. The next wave of "Extreme Edge AI" pushes aggressively towards sensors and actuators, opening major research and business development opportunities. In this talk I will give an overview of recent efforts in developing an Extreme Edge AI platform based on open source parallel ultra-low power (PULP) Risc-V processors and accelerators. I will then look at what comes next in this brave new world of hardware reinaissance.

Biography

Luca Beniniholds the chair of digital Circuits and systems at ETHZ and is Full Professor at the Universita di Bologna. He received a PhD from Stanford University. He has been visiting professor at Stanford University, IMEC, EPFL. In 2009-2012 he served as chief architect in STmicroelectronics France. Dr. Benini's research interests are in energy-efficient computing systems design, from embedded to high-performance. He is also active in the design ultra-low power VLSI Circuits and smart sensing micro-systems. He has published more than 1000 peer-reviewed papers and five books. He is an ERC-advanced grant winner, a Fellow of the IEEE, of the ACM and a member of the Academia Europaea. He is the recipient of the 2016 IEEE CAS Mac Van Valkenburgaward and of the 2019 IEEE TCAD Donald O. Pederson Best Paper Award.

Title	*Neuromorphic Computing: Past, Present, and Future*
Speaker	**Catherine Schuman** Oak Ridge National Laboratory, United States

Abstract

Though neuromorphic systems were introduced decades ago, there has been a resurgence of interest in recent years due to the looming end of Moore's law, the end of Dennard scaling, and the tremendous success of AI and deep learning for a wide variety of applications. With this renewed interest, there is a diverse set of research ongoing in neuromorphic computing, ranging from novel hardware implementations, device and materials to the development of new training and learning algorithms. There are many potential advantages to neuromorphic systems that make them attractive in today's computing landscape, including the potential for very low power, efficient hardware that can perform neural network computation. Though some compelling results have been demonstrated thus far that demonstrate these advantages, there is still significant opportunity for innovations in hardware, algorithms, and applications in neuromorphic computing. In this talk, a brief overview of the history of neuromorphic computing will be discussed, and a summary of the current state of research in the field will be presented. Finally, a list of key challenges, open questions, and opportunities for future research in neuromorphic computing will be enumerated.

Biography

Catherine (Katie) Schumanis a research scientist at Oak Ridge National Laboratory (ORNL). She received her Ph.D. in Computer Science from the University of Tennessee, where she completed her dissertation on the use of evolutionary algorithms to train spiking neural networks for neuromorphic systems. She is continuing her study of models and algorithms for neuromorphic computing at ORNL. Katie has a joint faculty appointment with the Department of Electrical Engineering and Computer Science at the University of Tennessee, where she co-leads the TENNLab neuromorphic research group. Katie has over 45 publications as well as six patents in the field of neuromorphic computing. Katie received the Department of Energy Early Career Award in 2019.

Title	*Leveraging Embedded Intelligence in Industry: Challenges and Opportunities*
Speaker	**Jim Tung** MathWorks Fellow, United States

Abstract

The buzz about AI is deafening. Compelling applications are starting to emerge, dramatically changing the customer service that we experience, the marketing messages that we receive, and some systems we use. But, as organizations decide whether and how to incorporate AI in their systems and services, they must bring together new combinations of specialized knowledge, domain expertise, and business objectives. They must navigate through numerous choices – algorithms, processors, compute placement, data availability, architectural allocation, communications, and more. At the same time, they must keep their focus on the applications that will create compelling value for them. In this keynote, Jim Tung looks at the promising opportunities and practical challenges of building AI into our systems and services.

Biography

Jim Tungis a 30-year veteran of MathWorks, focusing on business and technology strategy, and working with key customers and partners. Jim previously held the positions of vice president of marketing and vice president of business development. Prior to joining MathWorks, Jim held management positions at Lotus Development and Keithley DAS, a pioneering manufacturer of PC-based data acquisition systems.

Title	*Design-in-the-Cloud: Myth and Reality*
Speaker	**Philippe Quinio** STMicroelectronics, France

Abstract

The Cloud is promising orders of magnitude savings in time to market for integrated circuits, owing to CPU elasticity. However, practical limitations still mandate a selective approach to the product design flow and the business models have yet to be fully defined by vendors. The economic equation of designing in the cloud is challenging. In addition, design houses, IDMs and OEM customers have to decide to what extent they want to rely on Cloud service providers to maintain the confidentiality of their IP or SOC databases and honor export control requirements, in a context where such concerns are increasingly relevant in EDA vendor and IC supplier selection. This keynote will explore those topics based on ST's own experience and trials.

Biography

Philippe Quinio After an initial career in R&D in Japan, Philippe worked for a major US consulting firm in Europe & South America. He joined ST in 1995 in a Strategic Planning role. He then led the strategic marketing activities of ST's Consumer Group till 2002, when he became Marketing Director for ST's Imaging Division. In 2007, he moved to Corporate Finance, where he led several M&A projects. Since 2010, he heads the IP Sourcing & Strategy team, owns the IP/technology Make vs. Buy process, performs technology intelligence and oversees all IP/technology in-licensing for ST's businesses. More recently, this was expanded to cover EDA Strategy and Sourcing, where he chairs a company-wide EDA governance forum. Philippe was born in Versailles, France, in 1965 and graduated in Telecommunications Engineering from TelecomParis school in 1987. He also holds an MBA from INSEAD and is a Certified Licensing Professional (CLP™).

Title	*Memory Driven Computing to Revolutionize the Medical Sciences*
Speaker	**Joachim Schultze** German Center for Neurodegenerative Diseases, Germany

Abstract

As any other area of our lives, medicine is experiencing the digital revolution. We produce more and more quantitative data in medicine, and therefore, we need significantly more compute power and data storage capabilities in the near future. Yet, since medicine is inherently decentralized, current compute infrastructures are not build for that. Central cloud storage and centralized super computing infrastructures are not helpful in a discipline such as medicine that will produce data always at the edge. Here we completely need to rethink computing. What we require are distributed federated cloud solutions with sufficient memory at the edge to cope with the large sensor data that record many medical data of individual patients. Here memory-driven computing comes in as a perfect solution. Its potential to provide sufficiently large memory at the edge, where data is generated, yet its potential to connect these new devices to build distributed federated cloud solutions will be key to drive the digital revolution in medicine. I will provide our own efforts using memory driven computing towards this direction.

Biography

Joachim L. Schultzeis Professor for Genomics & Immunoregulation at the Life and Medical Sciences (LIMES)-Institute and Founding Director of the PRECISE Platform for Single Cell Genomics and Epigenomics at the German Center for Neurodegenerative Diseases and the University of Bonn. He went to Medical School at the University of Tübingen, spent almost 10 years at Dana-Farber Cancer Institute, Harvard Medical School, in Boston before he returned to Germany with a Sofia Kovalevskaya Award of the Humboldt Foundation. He is the coordinator of the German DFG-funded NGS competence centers in Germany, one of the speakers of the West German Genome Center, and one of the speakers of the only German Excellence Cluster in Immunology: ImmunoSensation2. He contributes his expertise to several EU consortia, amongst them SYSCID. He is an expert in macrophage biology and works at the interphase between immunology, genomics and the computational sciences. With his team he was the first to apply memory driven computing to genomics research. With his own research group and the PRECISE platform, his goal is to bring single cell technologies and machine learning approaches to the clinical arena. He is leading several programs on applying single cell technologies and memory driven computing to patients with Alzheimer's disease, chronic obstructive pulmonary disease, lung cancer or HIV. He has established research collaborations with HPE, AstraZeneca, BoehringerIngelheim, Becton Dickinson and other companies.

Program Overview

Monday, 09 March 2020

	13:30	Tutorial and Conference Registration							
	14:00 - 15:30	Tutorials							
	15:30 - 16:00	Break							
	16:00 - 18:00	Tutorials							
	18:00 - 21:00	Welcome Reception & PhD Forum							
Tuesday, 10 March 2020	08:30 - 10:30	1.1 Opening Session: Plenary, Awards Ceremony & Keynote Addresses 1 & 2							
	10:30 - 11:30	CB1 Coffee Break							
	11:30 - 13:00	Session 2.1	Session 2.2	Session 2.3	Session 2.4	Session 2.5	Session 2.6	Session 2.7	
	13:00 - 14:30	LB1 Lunch Break							
	13:50 - 14:20	3.0 LUNCH TIME KEYNOTE SESSION: Neuromorphic Computing: Past, Present, and Future							
	14:30 - 16:00	Session 3.1	Session 3.2	Session 3.3	Session 3.4	Session 3.5	Session 3.6	Session 3.7	
	16:00 - 16:30	IP1 Interactive Presentations							
	16:00 - 17:00	CB2 Coffee Break							
	17:00 - 18:30	Session 4.1	Session 4.2	Session 4.3	Session 4.4	Session 4.5	Session 4.6	Session 4.7	
Wednesday, 11 March 2020	08:30 - 10:00	Session 5.1	Session 5.2	Session 5.3	Session 5.4	Session 5.5	Session 5.6	Session 5.7	Session 5.8
	10:00 - 10:30	IP2 Interactive Presentations							
	10:00 - 11:00	CB3 Coffee Break							
	11:00 - 12:30	Session 6.1	Session 6.2	Session 6.3	Session 6.4	Session 6.5	Session 6.6	Session 6.7	
	12:30 - 14:30	LB2 Lunch Break							
	13:35 - 14:20	7.0 LUNCH TIME KEYNOTE SESSION							
	14:30 - 16:00	Session 7.1	Session 7.2	Session 7.3	Session 7.4	Session 7.5	Session 7.6	Session 7.7	
	16:00 - 16:30	IP3 Interactive Presentations							
	16:00 - 17:30	CB4 Coffee Break							
	17:00 - 18:30	Session 8.1	Session 8.2	Session 8.3	Session 8.4	Session 8.5	Session 8.6	Session 8.7	
	19:30 - 23:00	DATE Party | Networking Event							
Thursday, 12 March 2020	08:30 - 10:00	Session 9.1	Session 9.2	Session 9.3	Session 9.4	Session 9.5	Session 9.6	Session 9.7	Session 9.8
	10:00 - 10:30	IP4 Interactive Presentations							
	10:00 - 11:00	CB5 Coffee Break							
	11:00 - 12:30	Session 10.1	Session 10.2	Session 10.3	Session 10.4	Session 10.5	Session 10.6	Session 10.7	Session 10.8
	12:30 - 13:20	LB3 Lunch Break							
	13:20 - 13:50	11.0 LUNCH TIME KEYNOTE SESSION:							
	14:00 - 15:30	Session 11.1	Session 11.2	Session 11.3	Session 11.4	Session 11.5	Session 11.6	Session 11.7	Session 11.8
	15:30 - 16:00	CB6 Coffee Break IP5 Interactive Presentations							
	16:00 - 17:30	Session 12.1	Session 12.2	Session 12.3	Session 12.4	Session 12.5	Session 12.6	Session 12.7	Session 12.8

Friday, 13 March 2020

07:00 - 08:30	Workshop Registration and Welcome Refreshments
08:30 - 17:30	Workshops

DATE Best Paper Awards

DATE Best Paper Awards

Each year the Design, Automation and Test in Europe Conference presents awards to the authors of the best papers. The selection is performed by the award committee composed of the Track Chairs Cristiana Bolchini, Theocharis Theocharides, Jaume Abella and Valeria Bertacco and the following members:Borzoo Bonakdarpour,Andrea Calimera, Ramon Canal, Luca Carloni, Alessandro Cimatti, Ayse Coskun, Nikil Dutt, Ioannis Papaefstathiou, Dionisios Pnevmatikatos, Davide Quaglia,Muhammad Shafique, Olivier Sentieys, Luis Miguel Silveira, Juergen Teich, Vasileios Tenentes, Jerzy Tyszer, Arnaud Virazel.

The **DATE 2020** best papers are:

D Track
Impact of Magnetic Coupling and Density on STT-MRAM Performance
Lizhou Wu[1]; Siddharth Rao[2]; Mottaqiallah Taouil[1]; Erik Jan Marinissen[2];
Gouri Sankar Kar[2]; Said Hamdioui[1]
1 *Delft University of Technology, 2 IMEC*

A Track
A Flexible and Scalable NTT Hardware:
Applications from Homomorphically Encrypted Deep Learning to Post-Quantum Cryptography
Ahmet Can Mert[1]; Emre Karabulut[2]; Erdinc Ozturk[1]; Erkay Savas[1];
Michela Becchi[2]; Aydin Aysu[2]
1 Sabanci University, 2 North Carolina State University

T Track
DEFCON: Generating and Detecting Failure-prone Instruction Sequences via Stochastic Search
Ioannis Tsiokanos[1]; Lev Mukhanov[2]; Giorgis Georgakoudis[3];
Dimitrios S. Nikolopoulos[4]; Georgios Karakonstantis[1]
1 Queen's University Belfast, 2 QUB, 3 Lawrence Livermore National Laboratory,
4 Virginia Tech

E Track
Statistical Time-based Intrusion Detection in Embedded Systems
Nadir Carreon Rascon; Allison Gilbreath; Roman Lysecky
University of Arizona

Best Paper Award Nominations

Best Paper Award Nominations

D Track

Fast and Accurate DRAM Simulation: Can we Further Accelerate it?
Johannes Feldmann[1]; Matthias Jung[2]; Kira Kraft[1]; Lukas Steiner[1]; Norbert Wehn[1]
1 TU Kaiserslautern, 2 Fraunhofer IESE

ESP4ML: Platform-Based Design of Systems-on-Chip for Embedded Machine Learning
Davide Giri; Kuan-Lin Chiu; Giuseppe Di Guglielmo; Paolo Mantovani; Luca Carloni
Columbia University

Verification Runtime Analysis: Get the Most Out of Partial Verification
Martin Ring[1]; Fritjof Bornebusch[1]; ChristophLüth[1,2]; Robert Wille[3]; Rolf Drechsler[1,2]
1 DFKI, 2 University of Bremen, 3 Johannes Kepler University Linz

Gap-free Processor Verification by S²QED and Property Generation
Keerthikumara Devarajegowda[1]; Mohammad Rahmani Fadiheh[2]; Eshan Singh[3]; Clark Barrett[3]; Subhasish Mitra[3]; Wolfgang Ecker[1]; Dominik Stoffel[2]; Wolfgang Kunz[2]
1 Infineon Technologies, 2 TU Kaiserslautern, 3 Stanford University

GANA: Graph Convolutional Network Based Automated Netlist Annotation for Analog Circuits
Kishor Kunal[1]; Tonmoy Dhar[1]; Meghna Madhusudan[1]; Jitesh Poojary[1]; Arvind Sharma[1]; Wenbin Xu[2]; Steven Burns[3]; Jiang Hu[2]; Ramesh Harjani[1]; Sachin S. Sapatnekar[1]
1 University of Minnesota, 2 Texas A&M University, 3 Intel Corporation

Backtracking Search for Optimal Parameters of a PLL-based True Random Number Generator
Brice Colombier; Nathalie Bochard; Florent Bernard; Lilian Bossuet
University of Lyon

GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation
Biresh Kumar Joardar[1]; Nitthilan Kannappan Jayakodi[1]; Jana Doppa[1]; Partha Pratim Pande[1]; Hai (Helen) Li[2]; Krishnendu Chakrabarty[3]
1 Washington State University, 2 Duke University/TUM-IAS, 3 Duke University

PSB-RNN: A Processing-in-Memory Systolic ArrayArchitecture using Block Circulant Matrices for Recurrent Neural Networks
Nagadastagiri[1]; Sahithi Rampalli[1]; Makesh Tarun Chandran[1]; Gurpreet Singh Kalsi[2]; John (Jack) Sampson[1]; Sreenivas Subramoney[2]; Vijaykrishnan Narayanan[1]
1 The Pennsylvania State University, 2 Processor Architecture Research Lab, Intel Labs

A Learning-Based Thermal Simulation Framework
for Emerging Two-Phase Cooling Technologies
Zihao Yuan[1]; Geoffrey Vaartstra[2]; Prachi Shukla[1]; Zhengmao Lu[2]; Evelyn Wang[2]; Sherief Reda[3]; Ayse Coskun[1]
1 Boston University, 2 Massachusetts Institute of Technology, 3 Brown University

ProxSim: Simulation Framework for Cross-Layer Approximate DNN Optimization
Cecilia De la Parra[1]; Andre Guntoro[1]; Akash Kumar[2]
1 Robert Bosch GmbH, 2 TU Dresden

A Framework for Adding Low-Overhead, Fine-Grained Power Domains to CGRAs
Ankita Nayak; Keyi Zhang; Raj Setaluri; Alex Carsello; Makai Mann; Stephen Richardson; Rick Bahr; Pat Hanrahan; Mark Horowitz; Priyanka Raina
Stanford University

Floating Random Walk Based Capacitance Solver for VLSI Structures
with Non-Stratified Dielectrics
Mingye Song; Ming Yang; Wenjian Yu
Tsinghua University

Ternary Compute-Enabled Memory based on Ferroelectric Transistors
for Accelerating Deep Neural Networks
Sandeep Krishna Thirumala; Shubham Jain; Sumeet Gupta; Anand Raghunathan
Purdue University

Impact of Magnetic Coupling and Density on STT-MRAM Performance
Lizhou Wu[1]; Siddharth Rao[2]; Mottaqiallah Taouil[1]; Erik Jan Marinissen[2];
Gouri Sankar Kar[2]; Said Hamdioui[1]
1 *Delft University of Technology, 2 IMEC*

A Track

GenieHD: Efficient DNA Pattern Matching Accelerator Using Hyperdimensional Computing
Yeseong Kim; Mohsen Imani; Niema Moshiri;Tajana Rosing
University of California San Diego

Achieving Determinism in Adaptive AUTOSAR
Christian Menard[1]; Andres Goens[1]; Marten Lohstroh[2]; Jeronimo Castrillon[1]
1 TU Dresden, 2 University of California, Berkeley

A Flexible and Scalable NTT Hardware: Applications from Homomorphically Encrypted Deep Learning to Post-Quantum Cryptography
Ahmet Can Mert[1]; Emre Karabulut[2]; Erdinc Ozturk[1]; Erkay Savas[1];
Michela Becchi[2]; Aydin Aysu[2]
1 Sabanci University, 2 North Carolina State University

AntiDOte: Attention-based Dynamic Optimization for Neural Network Runtime Efficiency
Fuxun Yu[1]; Chenchen Liu[2]; Di Wang[3]; Yanzhi Wang[1]; Xiang Chen[1]
1 George Mason University, 2 University of Maryland, 3 Microsoft

Go Unary: A Novel Synapse Coding and Mapping Scheme
for Reliable ReRAM-based Neuromorphic Computing
Chang Ma; Yanan Sun; Weikang Qian; Ziqi Meng; Rui Yang; Li Jiang
Shanghai Jiao Tong University

T Track

On Improving Fault Tolerance of Memristor Crossbar Based Neural Network Designs
by Target Sparsifying
Song Jin[1]; Songwei Pei[2]; Yu Wang[1]
1 North China Electric Power University,
2 Beijing University of Posts and Telecommunications

Synthesis of Fault-Tolerant Reconfigurable Scan Networks
Sebastian Brandhofer; Michael Kochte; Hans-Joachim Wunderlich
University of Stuttgart

DEFCON: Generating and Detecting Failure-prone Instruction Sequences
via Stochastic Search
Ioannis Tsiokanos[1]; Lev Mukhanov[2]; Giorgis Georgakoudis[3];
Dimitrios S. Nikolopoulos[4]; Georgios Karakonstantis[1]
1 Queen's University Belfast, 2 QUB, 3 Lawrence Livermore National Laboratory,
4 Virginia Tech

Thermal-Cycling-aware Dynamic Reliability Management in Many-Core System-on-Chip
Mohammad-Hashem Haghbayan[1]; Antonio Miele[2]; Zhuo Zou[3];
Hannu Tenhunen[1]; Juha Plosila[1]
1 University of Turku, 2 Politecnico di Milano,
3 Nanjing University of Computer Science and Technology

E Track

Deeper Weight Pruning without Accuracy Loss in Deep Neural Networks
Byungmin Ahn; Taewhan Kim
Seoul National University

ACOUSTIC: Accelerating Convolutional Neural Networks
through Or-Unipolar Skipped Stochastic Computing
Wojciech Romaszkan; Tianmu Li; Tristan Melton; Sudhakar Pamarti; Puneet Gupta
University of California Los Angeles

Statistical Time-based Intrusion Detection in Embedded Systems
Nadir Carreon Rascon; Allison Gilbreath; Roman Lysecky
University of Arizona

Energy-efficient runtime resource management for adaptable multi-application mapping
Robert Khasanov; Jeronimo Castrillon
TU Dresden

CPS-oriented Modeling and Control of Traffic Signals Using Adaptive Back Pressure
Wanli Chang[1]; Debayan Roy[2]; Shuai Zhao[1]; Anuradha Annaswamy[3]; Samarjit Chakraborty[2]
1 University of York, 2 Technical University of Munich,
3 Massachusetts Institute of Technology

DATE PhD Forum2020

DATE PhD Forum2020

The PhD Forum of the DATE Conference is a poster session and a buffet style dinner hosted by the European Design Automation Association (EDAA), the ACM Special Interest Group on Design Automation (SIGDA), and the IEEE Council on Electronic Design Automation (CEDA). The purpose of the PhD Forum is to offer a forum for PhD students to discuss their thesis and research work with people of the design automation and system design community. It represents a good opportunity for students to get exposure on the job market and to receive valuable feedback on their work.

The DATE PhD Forum is associated with the DATE 2020 Welcome Reception and will take place on Monday, March 9, 2020, from 1800 - 2100 at the DATE venue in the Lunch Area. All registered conference delegates and exhibition visitors are kindly invited.

Robert Wille, Johannes Kepler University Linz(Chair,DATE PhD Forum 2020)

PhD Forum Committee

Juergen Alt, Intel Germany
Iris Bahar, Brown University
Davide Bertozzi, University of Ferrara
Armin Biere, Johannes Kepler University Linz
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Felipe Rocha da Rosa, UFRGS
Andreas Steininger, Vienna University of Technology
Sander Stuijk, Eindhoven University
Daniel Tille, Infineon Technologies
Shigeru Yamashita, Ritsumeikan University

Admitted Presentations

FM01.1.1 Networks-on-Chip for Heterogeneous 3D Systems-on-Chip
Jan Moritz Joseph, Otto-von-Guericke Universität Magdeburg, Germany

FM01.1.2 Intelligent Scheduling Algorithms for Energy Optimization in Smart Grid
Nilotpal Chakraborty, IIT Patna, India

FM01.1.3 Enhanced Detection and Prevention Techniques to Ensure a Secured Hardware with Improved Performance Metrics
Sree Ranjani, IIT Madras, India

FM01.1.4 QoS-aware Cross-layer Reliability-integrated Design of Heterogeneous Embedded Systems
Siva Satyendra Sahoo, Technische Universität Dresden, Germany

FM01.1.5 Design and implementation aspects of post-quantum cryptography
Angshuman Karmakar, imec-COSIC, KU Leuven, Belgium

FM01.1.6 Security implications of power management systems in multicore devices
Philipp Miedl, ETH Zurich, Switzerland

FM01.1.7 Towards Sustainable Logic Encryption in an Age of Mistrust
Amin Rezaei, Northwestern University, United States

FM01.1.8 Architectures And Automation For Beyond-CMOS Technologies
Debjyoti Bhattacharjee, Nanyang Technological University, Singapore

FM01.1.9 On-chip Thermal Monitoring and Optimization for New-generation Manycore Systems
Mengquan Li, Nanyang Technological University, Singapore

FM01.1.10 Instruction-Level Abstraction (ILA): A Uniform Specification for System-on-Chip (SoC) Verification
Bo-Yuan Huang, Student, Taiwan

FM01.1.11 A Formal Approach towards Pattern Guided Scheduling in Embedded Control Systems
Sumana Ghosh, TUM, Germany

FM01.1.12 Design and Evaluation of Ethernet-based E/E-Architectures for Latency- and Safety-critical Applications
Fedor Smirnov, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

FM01.1.13 System-Level Mapping, Analysis, and Management of Real-Time Applications in Many-Core Systems
Behnaz Pourmohseni, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

FM01.1.14 Self Aware Nature Inspired Approaches Ensuring Embedded Security
Krishnendu Guha, University of Calcutta, India

FM01.1.15 CAD Frameworks for Advancing Design IP Protection
Satwik Patnaik, New York University, United States

FM01.1.16 Design Automation for Error-Tolerant Sample Preparation with Digital Microfluidic Biochips
Sudip Poddar, National Taiwan University of Science and Technology, Taiwan

FM01.1.17 Automated Test Generation with SystemC Designs for Pre-Silicon Validation
Bin Lin, Portland State University, United States

FM01.1.18 Dynamic Energy Management of Mixed-Criticality Real-Time Networks-on-Chip
Thawra Kadeed, TU Braunschweig, Germany

FM01.1.19 Proving Correctness of Industrial Multipliers using Symbolic Computer Algebra
Alireza Mahzoon, University of Bremen, Germany

FM01.1.20 A Holistic Approach to Functional Safety for Networked Cyber-Physical Systems
Enrico Fraccaroli, Università degli Studi di Verona, Italy

FM01.1.21 Automated Analysis of Virtual Prototypes at the Electronic System Level– Design Understanding and Applications–
Mehran Goli, University of Bremen, Germany

FM01.1.22 A Novel Test Flow for Approximate Digital Circuits
Marcello Traiola, LIRMM, France

FM01.1.23 Heterogeneous HW/SW Techniques for Reliable Systems
Florian Kriebel, Vienna University of Technology, Austria

FM01.1.24 Efficient Scale-Up and Scale-Out of Beam Longitudinal Dynamics Simulations
Konstantinos Iliakis, National Technical University of Athens, Greece

FM01.1.25 On Improving Statistical Model Checking by Qualitative Verification
Tim Gonschorek, Otto von Guericke University Magdeburg, Germany

FM01.1.26 Verifying Multipliers using Computer Algebra
Daniela Kaufmann, Johannes Kepler University, Austria

FM01.1.27 Energy-efficient Photonic Architectures for Large-scale Computing
Dharanidhar Dang, University of California, San Diego, United States

FM01.1.28 Energy Efficient and Reliable Deep Learning Accelerator Design
Jeff Zhang, New York University, United States

FM01.1.29 Connecting the Dots: From Theory to Application of IP Protection
Abhrajit Sengupta, New York University, United States

FM01.1.30 Realistic Scheduling Models and Analyses for Advanced Real-Time Embedded Systems
Georg von der Brüggen, TU Dortmund University, Germany

FM01.1.31 Energy-efficient and Performance-driven Implementation of Computational Pipelines of Whole Genome Sequencing on Embedded Platforms
Sidharth Maheshwari, Newcastle University, United Kingdom

FM01.1.32 Complexity Reduction for Embedded System-Level Design
Valentina Richthammer, Ulm University, Germany

University Booth at DATE 2020

University Booth at DATE 2020

The University Booth is organised during DATE and will be located in the **exhibition area at booth 11**. All demonstrations will take place from **Tuesday, March 10 to Thursday, March 12, 2020** during DATE. Universities and public research institutes have been invited to submit hardware or software demonstrators.

The University Booth programme is composed of **42 demonstrations** from **11 countries**, presenting software and hardware solutions. The programme is organised in **11 sessions** of 2 or 2.5 h duration and will cover the topics:

- **Electronic Design Automation Prototypes**
- **Hardware Design and Test Prototypes**
- **Embedded Systems Design**

The University Booth at DATE 2020 invites you to find out more about the latest trends in software and hardware from the international research community.

Most demonstrators will be shown more than once, giving visitors more flexibility to come to the booth and find out about the latest innovations.

We are sure that the demonstrators will give an attractive supplement to the DATE conference program and exhibition. We would like to thank all contributors to this programme.

More information is available online at https://www.date-conference.com/exhibition/university-booth.The University Booth programme is included in the conference booklet and available online at https://www.date-conference.com/exhibition/university-booth/programme.The following demonstrators will be presented at the University Booth.

A BINARY TRANSLATION FRAMEWORK FOR AUTOMATED HARDWARE GENERATION

Authors:
Nuno Paulino and João Canas Ferreira, INESC TEC / University of Porto, PT

Timeslots:

- UB07.3 (Wednesday, March 11, 2020 14:00 - 16:00)

***Abstract**: Hardware specialization is an efficient solution for maximization of performance and minimization of energy consumption. This work is based on automated detection of workload by analysis of a compiled application, and on the automated generation of specialized hardware modules. We will present the current version of the binary analysis and translation framework. Currently, our implementation is capable of processing ARMv8 and MicroBlaze (32-bit) Executable and Linking Format (ELF) files or instruction traces. The framework can interpret the instructions for these two ISAs, and detect different types of instruction patterns. After detection, segments are converted into CDFG representations exposing the underlying Instruction Level Parallelism which we aim to exploit via automated hardware generation. On-going work is addressing the extraction of cyclical execution traces or static code blocks, more methods of hardware generation.*

A DIGITAL MICROFLUIDICS BIO-COMPUTING PLATFORM

Authors:
Georgi Tanev, Luca Pezzarossa, Winnie Edith Svendsen and Jan Madsen, TU Denmark, DK

Timeslots:

- UB02.2 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB06.1 (Wednesday, March 11, 2020 12:00 - 14:00)

***Abstract**: Digital microfluidics is a lab-on-a-chip (LOC) technology used to actuate small amounts of liquids on an array of individually addressable electrodes. Microliter sized droplets can be programmatically dispensed, moved, mixed, split, in a controlled environment which combined with miniaturized sensing techniques makes LOC suitable for a broad range of applications in the field of medical diagnostics and synthetic biology. Furthermore, a programmable digital microfluidics platform holds the potential to add a "fluidic subsystem" to the classical computation model thus opening the doors for cyber-physical bio-processors. To facilitate the programming and operation of such bio-fluidic computing, we propose dedicated instruction set architecture and virtual machine. A set of digital microfluidic core instructions as well as classic computing operations are executed on a virtual machine, which decouples the protocol execution from the LOC functionality.*

AT-SPEED DFT ARCHITECTURE FOR BUNDLED-DATA CIRCUITS

Authors:
Ricardo Aquino Guazzelli and Laurent Fesquet, Université Grenoble Alpes, FR

Timeslots:

- UB02.5 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB05.7 (Wednesday, March 11, 2020 10:00 - 12:00)

***Abstract**: At-speed testing for asynchronous circuits is still an open concern in the literature. Due to its timing constraints between control and data paths, Design for Testability (DfT) methodologies must test both control and data paths at the same time in order to guarantee the circuit correctness. As Process Voltage Temperature (PVT) variations significantly impact circuit design in newer CMOS technologies and low-power techniques such as voltage scaling, the timing constraints between control and data paths must be tested after fabrication not only under nominal conditions but through a range of operating conditions. This work explores an at-speed testing approach for bundled data circuits, targetting the micropipeline template. The main target of this test approach focuses on whether the sized delay lines in control paths respect the local timing assumptions of the data paths.*

ATECES: AUTOMATED TESTING THE ENERGY CONSUMPTION OF EMBEDDED SYSTEMS

Authors:
Eduard Enoiu, Mälardalen University, SE

Timeslots:

- UB10.10 (Thursday, March 12, 2020 12:00 - 14:30)
- UB11.1 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: The demostrator will focus on automatically generating test suites by selecting test cases using random test generation and mutation testing is a solution for improving the efficiency and effectiveness of testing. Specifically, we generate and select test cases based on the concept of energy-aware mutants, small syntactic modifications in the system architecture, intended to mimic real energy faults. Test cases that can distinguish a certain behavior from its mutations are sensitive to changes, and hence considered to be good at detecting faults. We applied this method on a brake by wire system and our results suggest that an approach that selects test cases showing diverse energy consumption can increase the fault detection ability. This kind of results should motivate both academia and industry to investigate the use of automatic test generation for energy consumption.*

BCFELEAM: BACKFLOW: BACKWARD EDGE CONTROL FLOW ENFORCEMENT FOR LOW END ARM REAL-TIME SYSTEMS

Authors:
Bresch Cyril[1], David Hély[1], Roman Lysecky[2] and Stephanie Chollet[1]
[1]LCIS, FR; [2]University of Arizona, US

Timeslots:

- UB05.4 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB07.2 (Wednesday, March 11, 2020 14:00 - 16:00)

***Abstract**: The C programming language is one of the most popular languages in embedded system programming. Indeed, C is efficient, lightweight and can easily meet high performance and deterministic real-time constraints. However, these assets come at a certain price. Indeed, C does not provide extra features for memory safety. As a result, attackers can easily exploit spatial memory vulnerabilities to hijack the execution flow of an application. The demonstration features a real-time connected infusion pump vulnerable to memory attacks. First, we showcase an exploit that remotely takes control of the pump. Then, we demonstrate the effectiveness of BackFlow, an LLVM-based compiler extension that enforces control-flow integrity in low-end ARM embedded systems.*

BROOK SC: HIGH-LEVEL CERTIFICATION-FRIENDLY PROGRAMMING FOR GPU-POWERED SAFETY CRITICAL SYSTEMS

Authors:
Marc Benito, Matina Maria Trompouki and Leonidas Kosmidis, BSC / UPC, ES

Timeslots:

- UB04.7 (Tuesday, March 10, 2020 17:30 - 19:30)

***Abstract**: Graphics processing units (GPUs) can provide the increased performance required in future critical systems, i.e. automotive and avionics. However, their programming models, e.g. CUDA or OpenCL, cannot be used in such systems as they violate safety critical programming guidelines. Brook*

SC (https://github.com/lkosmid/brook) was developed in UPC/BSC to allow safety-critical applications to be programmed in a CUDA-like GPU language, Brook, which enables the certification while increasing productivity. In our demo, an avionics application running on a realistic safety critical GPU software stack and hardware is show cased. In this Bachelor's thesis project, which was awarded a 2019 HiPEAC Technology Transfer Award, an Airbus prototype application performing general-purpose computations with a safety-critical graphics API was ported to Brook SC in record time, achieving an order of magnitude reduction in the lines of code to implement the same functionality without performance penalty.

CATANIS: CAD TOOL FOR AUTOMATIC NETWORK SYNTHESIS

Authors:
Davide Quaglia, Enrico Fraccaroli, Filippo Nevi and Sohail Mushtaq, Università di Verona, IT

Timeslots:

- UB01.8 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB05.8 (Wednesday, March 11, 2020 10:00 - 12:00)

***Abstract**: The proliferation of communication technologies for embedded systems opened the way for new applications, e.g., Smart Cities and Industry 4.0. In such applications hundreds or thousands of smart devices interact together through different types of channels and protocols. This increasing communication complexity forces computer-aided design methodologies to scale up from embedded systems in isolation to the global inter-connected system. Network Synthesis is the methodology to optimally allocate functionality onto network nodes and define the communication infrastructure among them. This booth will demonstrate the functionality of a graphic tool for automatic network synthesis developed by the Computer Science Department of University of Verona. It allows to graphically specify the communication requirements of a smart space (e.g., its map can be considered) in terms of sensing and computation tasks together with a library of node types and communication protocols to be used.*

CSI-REPUTE: A LOW POWER EMBEDDED DEVICE CLUSTERING APPROACH TO GENOME READ MAPPING

Authors:
Tousif Rahman[1], Sidharth Maheshwari[1], Rishad Shafik[1], Ian Wilson[1], Alex Yakovlev[1] and Amit Acharyya[2]
[1]Newcastle University, GB; [2]IIT Hyderabad, IN

Timeslots:

- UB03.6 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.6 (Tuesday, March 10, 2020 17:30 - 19:30)

***Abstract**: The big data challenge of genomics is rooted in its requirements of extensive computational capability and results in large power and energy consumption. To encourage widespread usage of genome assembly tools there must be a transition from the existing predominantly software-based mapping tools, optimized for homogeneous high-performance systems, to more heterogeneous low power and cost-effective mapping systems. This demonstration will show a cluster system implementation for the REPUTE algorithm, (An OpenCL based Read Mapping Tool for Embedded Genomics) where cluster nodes are composed of low power single board computer (SBC) devices and the algorithm is deployed on each node spreading the genomic workload, we propose a working concept prototype to challenge current conventional high-performance many-core CPU based cluster nodes. This*

demonstration will highlight the advantage in the power and energy domains of using SBC clusters enabling potential solutions to low-cost genomics.

DEEPSENSE-FPGA: FPGA ACCELERATION OF A MULTIMODAL NEURAL NETWORK

Authors:
Mehdi TrabelsiAjili and Yuko Hara-Azumi, Tokyo Institute of Technology, JP

Timeslots:

- UB07.7 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB10.7 (Thursday, March 12, 2020 12:00 - 14:30)

***Abstract**: Currently, Internet of Things and Deep Learning (DL) are merging into one domain and creating outstanding technologies for various classification tasks. Such technologies require complex DL networks that are mainly targeting powerful platforms with rich computing resources like servers. Therefore, for resource-constrained embedded systems, new challenges of size, performance and power consumption have to be considered, particularly when edge devices handle multimodal data, i.e., different types of real-time sensing data (voice, video, text, etc.). Our ongoing project is focused on DeepSense, a multimodal DL framework combining Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN) to process time-series data, such as accelerometer and gyroscope to detect human activity. We aim at accelerating DeepSense by FPGA (Xilinx Zynq) in a hardware-software co-design manner. Our demo will show the latest achievements through latency and power consumption evaluations.*

DESIGN AUTOMATION FOR XBM AUTOMATA IN WORKCRAFT: DESIGN AUTOMATION FOR EXTENDED BURST-MODE AUTOMATA IN WORKCRAFT

Authors:
Alex Chan, Alex Yakovlev, Danil Sokolov and Victor Khomenko, Newcastle University, GB

Timeslots:

- UB05.6 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB07.6 (Wednesday, March 11, 2020 14:00 - 16:00)

***Abstract**: Asynchronous circuits are known to have high performance, robustness and low power consumption, which are particularly beneficial for the area of so-called "little digital" controllers where low latency is crucial. However, asynchronous design is not widely adopted by industry, partially due to the steep learning curve inherent in the complexity of formal specifications, such as Signal Transition Graphs (STGs). In this demo, we promote a class of the Finite State Machine (FSM) model called Extended Burst-Mode (XBM) automata as a practical way to specify many asynchronous circuits. The XBM specification has been automated in the Workcraft toolkit (https://workcraft.org) with elaborate support for state encoding, conditionals and "don't care" signals. Formal verification and logic synthesis of the XBM automata is implemented via conversion to the established STG model, reusing existing methods and CAD tools. Tool support for the XBM flow will be demonstrated using several case studies.*

DISTRIBUTING TIME-SENSITIVE APPLICATIONS ON EDGE COMPUTING ENVIRONMENTS

Authors:
EudaldSabaté Creixell[1], Unai Perez Mendizabal[1], Elli Kartsakli[2], Maria A. Serrano Gracia[3] and Eduardo Quiñones Moreno[3]
[1]BSC / UPC, ES; [2]BSC, GR; [3]BSC, ES

Timeslots:

- UB04.10 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB08.3 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB11.3 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: The proposed demonstration aims to showcase the capabilities of a task-based distributed programming framework for the execution of real-time applications in edge computing scenarios, in the context of smart cities. Edge computing shifts the computation close to the data source, alleviating the pressure on the cloud and reducing application response times. However, the development and deployment of distributed real-time applications is complex, due to the heterogeneous and dynamic edge environment where resources may not always be available. To address these challenges, our demo employs COMPSs, a highly portable and infrastructure-agnostic programming model, to efficiently distribute time-sensitive applications across the compute continuum. We will exhibit how COMPSs distributes the workload on different edge devices (e.g., NVIDIA GPUs and a Rasberry Pi), and how COMPSs re-adapts this distribution upon the availability (connection or disconnection) of devices.*

DL PUF ENAU: DEEP LEARNING BASED PHYSICALLY UNCLONABLE FUNCTION ENROLLMENT AND AUTHENNTICATION

Authors:
Amir Alipour[1], David Hely[2], Vincent Beroulle[2] and Giorgio Di Natale[3]
[1]Grenoble INP / LCIS, FR; [2]Grenoble INP, FR; [3]CNRS / Grenoble INP / TIMA, FR

Timeslots:

- UB07.1 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB10.4 (Thursday, March 12, 2020 12:00 - 14:30)
- UB11.4 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: Physically Unclonable Functions (PUFs) have been addressed nowadays as a potential solution to improve the security in authentication and encryption process in Cyber Physical Systems. The research on PUF is actively growing due to its potential of being secure, easily implementable and expandable, using considerably less energy. To use PUF in common, the low level device Hardware Variation is captured per unit for device enrollment into a format called Challenge-Response Pair (CRP), and recaptured after device is deployed, and compared with the original for authentication. These enrollment + comparison functions can vary and be more data demanding for applications that demand robustness, and resilience to noise. In this demonstration, our aim is to show the potential of using Deep Learning for enrollment and authentication of PUF CRPs. Most importantly, during this demonstration, we will show how this method can save time and storage compared to other classical methods.*

ECLT FPGA COMPONENT: EDGE-TO-CLOUD LOCATION-TRANSPARENT FPGA COMPONENT

Authors:
Takeshi Ohkawa, Tokai University, JP

Timeslots:

- UB06.5 (Wednesday, March 11, 2020 12:00 - 14:00)
- UB08.4 (Wednesday, March 11, 2020 16:00 - 18:00)

***Abstract**: To exploit the benefits of FPGA, it is necessary to improve the usability of FPGA from the software system as well as the design productivity of FPGA circuitry itself. Therefore, an FPGA component technology is expected in which software can access FPGA circuitry easily and communicate with other FPGA/software components through the network in the whole edge-to-cloud system using a variety of communication protocols. In this demonstration, a location-transparent FPGA component which is capable of image recognition processing and communicating with ROS (Robot Operating System) protocol are exhibited. The FPGA component works in the ROS system and the component can be in an arbitrary location in the Edge-to-Cloud network system.*

EEC: ENERGY EFFICIENT COMPUTING VIA DYNAMIC VOLTAGE SCALING AND IN-NETWORK OPTICAL PROCESSING

Authors:
Ryosuke Matsuo[1], Jun Shiomi[1], Yutaka Masuda[2] and Tohru Ishihara[2]
[1]Kyoto University, JP; [2]Nagoya University, JP

Timeslots:

- UB01.7 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB09.7 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: This poster demonstration will show results of our two research projects. The first one is on a project of energy efficient computing. In this project we developed a power management algorithm which keeps the target processor always running at the most energy efficient operating point by appropriately tuning the supply voltage and threshold voltage under a specific performance constraint. This algorithm is applicable to wide variety of processor systems including high-end processors and low-end embedded processors. We will show the results obtained with actual RISC processors designed using a 65nm technology. The second one is on a project of in-network optical computing. We show optical functional units such as parallel multipliers and optical neural networks. Several key techniques for reducing the power consumption of optical circuits will be also presented. Finally, we will show the results of optical circuit simulation, which demonstrate the light speed operation of the circuits.*

ELSA: EIGENVALUE BASED HYBRID LINEAR SYSTEM ABSTRACTION: BEHAVIORAL MODELING OF TRANSISTOR-LEVEL CIRCUITS USING AUTOMATIC ABSTRACTION TO HYBRID AUTOMATA

Authors:
Ahmad Tarraf and Lars Hedrich, University of Frankfurt, DE

Timeslots:

- UB03.2 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.2 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB05.2 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB06.2 (Wednesday, March 11, 2020 12:00 - 14:00)

- UB08.2 (Wednesday, March 11, 2020 16:00 - 18:00)

***Abstract**: Model abstraction of transistor-level circuits, while preserving an accurate behavior, is still an open problem. In this demo an approach is presented that automatically generates a hybrid automaton (HA) with linear states from an existing circuit netlist. The approach starts with a netlist at transistor level with full SPICE accuracy and ends at the system level description of the circuit in matlab or in Verilog-A. The resulting hybrid automaton exhibits linear behavior as well as the technology dependent nonlinear e.g. limiting behavior. The accuracy and speed-up of the Verilog-A generated models is evaluated based on several transistor level circuit abstractions of simple operational amplifiers up to a complex filters. Moreover, we verify the equivalence between the generated model and the original circuit. For the generated models in matlab syntax, a reachability analysis is performed using the reachability tool cora.*

EUCLID-NIR GPU: AN ON-BOARD PROCESSING GPU-ACCELERATED SPACE CASE STUDY DEMONSTRATOR

Authors:
Ivan Rodriguez and Leonidas Kosmidis, BSC / UPC, ES

Timeslots:

- UB05.3 (Wednesday, March 11, 2020 10:00 - 12:00)

***Abstract**: Embedded Graphics Processing Units (GPUs) are very attractive candidates for on-board payload processing of future space systems, thanks to their high performance and low-power consumption. Although there is significant interest from both academia and industry, there is no open and publicly available case study showing their capabilities, yet. In this master thesis project, which was performed within the GPU4S (GPU for Space) ESA-funded project, we have parallelised and ported the Euclid NIR (Near Infrared) image processing algorithm used in the European Space Agency's (ESA) mission to be launched in 2022, to an automotive GPU platform, the NVIDIA Xavier. In the demo we will present in real-time its significantly higher performance achieved compared to the original sequential implementation. In addition, visitors will have the opportunity to examine the images on which the algorithm operates, as well as to inspect the algorithm parallelisation through profiling and code inspection.*

FASTHERMSIM: FAST AND ACCURATE THERMAL SIMULATIONS FROM CHIPLETS TO SYSTEM

Authors:
Yu-Min Lee, Chi-Wen Pan, Li-Rui Ho and Hong-Wen Chiou, National Chiao Tung University, TW

Timeslots:

- UB01.5 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB03.10 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB08.8 (Wednesday, March 11, 2020 16:00 - 18:00)

***Abstract**: Recently, owing to the scaling down of technology and 2.5D/3D integration, power densities and temperatures of chips have been increasing significantly. Though commercial computational fluid dynamics tools can provide accurate thermal maps, they may lead to inefficiency in thermal-aware design with huge runtime. Thus, we develop the chip/package/system-level thermal analyzer, called FasThermSim, which can assist you to improve your design under thermal constraints in pre/post-silicon*

stages. In FasThermSim, we consider three heat transfer modes, conduction, convection, and thermal radiation. We convert them to temperature-independent terms by linearization methods and build a compact thermal model (CTM). By applying numerical methods to the CTM, the steady-state and transient thermal profiles can be solved efficiently without loss of accuracy. Finally, an easy-to-use thermal analysis tool is implemented for your design, which is flexible and compatible, with the graphic user interface.

FLETCHER: TRANSPARENT GENERATION OF HARDWARE INTERFACES FOR ACCELERATING BIG DATA APPLICATIONS

Authors:
Zaid Al-Ars, Johan Peltenburg, Jeroen van Straten, Matthijs Brobbel and Joost Hoozemans, TU Delft, NL

Timeslots:

- UB02.1 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB03.1 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.1 (Tuesday, March 10, 2020 17:30 - 19:30)

***Abstract**: This demo created by TUDelft is a software-hardware framework to allow for an efficient integration of FPGA hardware accelerators both on edge devices as well as in the cloud. The framework is called Fletcher, which is used to automatically generate data communication interfaces in hardware based on the widely used big data format Apache Arrow. This provides two distinct advantages. On the one hand, since the accelerators use the same data format as the software, data communication bottlenecks can be reduced. On the other hand, since a standardized data format is used, this allows for easy-to-use interfaces on the accelerator side, thereby reducing the design and development time. The demo shows how to use Fletcher for big data acceleration to decompress Snappy compressed files and perform filtering on the whole Wikipedia body of text. The demo enables 25 GB/s processing throughput.*

FPGA-DSP: A PROTOTYPE FOR HIGH QUALITY DIGITAL AUDIO SIGNAL PROCESSING BASED ON AN FPGA

Authors:
Bernhard Riess and Christian Epe, University of Applied Sciences Düsseldorf, DE

Timeslots:

- UB02.4 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB03.4 (Tuesday, March 10, 2020 15:00 - 17:30)

***Abstract**: Our demonstrator presents a prototype of a new digital audio signal processing system which is based on an FPGA. It achieves a performance that up to now has been preserved to costly high-end solutions. Main components of the system are an analog/digital converter, an FPGA to perform the digital signal processing tasks, and a digital/analog converter implemented on a printed circuit board. To demonstrate the quality of the audio signal processing, infinite impulse response, finite impulse response filters and a delay effect were realized in VHDL. More advanced signal processing systems can easily be implemented due to the flexibility of the FPGA. Measured results were compared to state of the art audio signal processing systems with respect to size, performance and cost. Our prototype outperforms systems of the same price in quality, and outperforms systems of the same quality at a maximum of 20% of the price. Examples of the performance of our system can be heard in the demo.*

FU: LOW POWER AND ACCURACY CONFIGURABLE APPROXIMATE ARITHMETIC UNITS

Authors:
TomoakiUkezono and Toshinori Sato, Fukuoka University, JP

Timeslots:

- UB05.10 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB09.10 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: In this demonstration, we will introduce the approximate arithmetic units such as adder, multiplier, and MAC that are being studied in our system-architecture laboratory. Our approximate arithmetic units can reduce delay and power consumption at the expense of accuracy. Our approximate arithmetic units are intended to be applied to IoT edge devices that can process images, and are suitable for battery-driven and low-cost devices. The biggest feature of our approximate arithmetic units is that the circuit is configured so that the accuracy is dynamically variable, and the trade-off relationship between accuracy and power can be selected according to the usage status of the device. In this demonstration, we show the power consumption according to various accuracy-requirements based on actual data and claim the practicality of the proposed arithmetic units.*

FUZZING EMBEDDED BINARIES LEVERAGING SYSTEMC-BASED VIRTUAL PROTOTYPES

Authors:
Vladimir Herdt[1], Daniel Grosse[2] and Rolf Drechsler[2]
[1]DFKI, DE; [2]University of Bremen / DFKI GmbH, DE

Timeslots:

- UB01.1 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB03.7 (Tuesday, March 10, 2020 15:00 - 17:30)

***Abstract**: Verification of embedded Software (SW) binaries is very important. Mainly, simulation-based methods are employed that execute (randomly) generated test-cases on Virtual Prototypes (VPs). However, to enable a comprehensive VP-based verification, sophisticated test-case generation techniques need to be integrated. Our demonstrator combines state-of-the-art fuzzing techniques with SystemC-based VPs to enable a fast and accurate verification of embedded SW binaries. The fuzzing process is guided by the coverage of the embedded SW as well as the SystemC-based peripherals of the VP. The effectiveness of our approach is demonstrated by our experiments, using RISC-V SW binaries as an example.*

GENERATING ASYNCHRONOUS CIRCUITS FROM CATAPULT

Authors:
Yoan Decoudu[1], Jean Simatic[2], Katell Morin-Allory[3] and Laurent Fesquet[3]
[1]University Grenoble Alpes, FR; [2]HawAI.Tech, FR; [3]Université Grenoble Alpes, FR

Timeslots:

- UB02.7 (Tuesday, March 10, 2020 12:30 - 15:00)

- UB06.7 (Wednesday, March 11, 2020 12:00 - 14:00)
- UB10.8 (Thursday, March 12, 2020 12:00 - 14:30)
- UB11.8 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: In order to spread asynchronous circuit design to a large community of designers, High-Level Synthesis (HLS) is probably a good choice because it requires limited design technical skills. HLS usually provides an RTL description, which includes a data-path and a control-path. The desynchronization process is only applied to the control-path, which is a Finite State Machine (FSM). This method is sufficient to make asynchronous the circuit. Indeed, data are processed step by step in the pipeline stages, thanks to the desynchronized FSM. Thus, the data-path computation time is no longer related to the clock period but rather to the average time for processing data into the pipeline. This tends to improve speed when the pipeline stages are not well-balanced. Moreover, our approach helps to quickly designing data-driven circuits while maintaining a reasonable cost, a similar area and a short time-to-market.*

INTACT: A 96-CORE PROCESSOR WITH 6 CHIPLETS 3D-STACKED ON AN ACTIVE INTERPOSER AND A 16-CORE PROTOTYPE RUNNING GRAPHICAL OPERATING SYSTEM

Authors:
Eric Guthmuller[1], Pascal Vivet[1], César Fuguet[1], Yvain Thonnart[1], Gaël Pillonnet[2] and Fabien Clermidy[1]
[1]Université Grenoble Alpes / CEA List, FR; [2]Université Grenoble Alpes / CEA-Leti, FR

Timeslots:

- UB01.6 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB02.6 (Tuesday, March 10, 2020 12:30 - 15:00)

***Abstract**: We built a demonstrator for our 96-cores cache coherent 3D processor and a first prototype featuring 16 cores. The demonstrator consists in our 16-cores processor running commodity operating systems such as Linux and NetBSD on a PC-like motherboard with user-friendly devices such as a HDMI display, keyboard and mouse. A graphical desktop is displayed, and the user will interact with it through the keyboard and mouse. The demonstrator is able to run parallel applications to benchmark its performance in terms of scalability. The main innovation of our processor is its scalable cache coherent architecture based on distributed L2-caches and adaptive L3-caches. Additionally, the energy consumption is also measured and displayed by reading dynamically from the monitors of power-supply devices. Finally we will also show open packages of the 3D processor featuring 6 16-core chiplets (28 nm FDSOI) on an active interposer (65 nm) embedding Network-on-Chips, power management and IO controllers.*

JOINTER: JOINING FLEXIBLE MONITORS WITH HETEROGENEOUS ARCHITECTURES

Authors:
Giacomo Valente[1], Tiziana Fanni[2], Carlo Sau[3], Claudio Rubattu[2], Francesca Palumbo[2] and Luigi Pomante[1]
[1]Università degliStudidell'Aquila, IT; [2]Università degliStudi di Sassari, IT; [3]Università degliStudi di Cagliari, IT

Timeslots:

- UB01.10 (Tuesday, March 10, 2020 10:30 - 12:30)

- UB02.10 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB06.10 (Wednesday, March 11, 2020 12:00 - 14:00)

***Abstract**: As embedded systems grow more complex and shift toward heterogeneous architectures, understanding workload performance characteristics becomes increasingly difficult. In this regard, run-time monitoring systems can support on obtaining the desired visibility to characterize a system. This demo presents a framework that allows to develop complex heterogeneous architectures composed of programmable processors and dedicated accelerators on FPGA, together with customizable monitoring systems, keeping under control the introduced overhead. The whole development flow (and related prototypal EDA tools), that starts with the accelerators creation using a dataflow model, in parallel with the monitoring system customization using a library of elements, showing also the final joining, will be shown. Moreover, a comparison among different monitoring systems functionalities on different architectures developed on Zynq7000 SoC will be illustrated.*

LAGARTO: FIRST SILICON RISC-V ACADEMIC PROCESSOR DEVELOPED IN SPAIN

Authors:
Guillem Cabo Pitarch[1], Cristobal Ramirez Lazo[1], Julian Pavon Rivera[1], Vatistas Kostalabros[1], Carlos Rojas Morales[1], Miquel Moreto[1], Jaume Abella[1], Francisco J. Cazorla[1], Adrian Cristal[1], Roger Figueras[1], Alberto Gonzalez[1], Carles Hernandez[1], Cesar Hernandez[2], Neiel Leyva[2], Joan Marimon[1], Ricardo Martinez[3], Jonnatan Mendoza[1], Francesc Moll[4], Marco Antonio Ramirez[2], Carlos Rojas[1], Antonio Rubio[4], Abraham Ruiz[1], Nehir Sonmez[1], Lluis Teres[3], Osman Unsal[5], Mateo Valero[1], Ivan Vargas[1] and Luis Villa[2]
[1]BSC / UPC, ES; [2]CIC-IPN, MX; [3]IMB-CNM (CSIC), ES; [4]UPC, ES; [5]BSC, ES

Timeslots:

- UB01.3 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB04.4 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB08.1 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB10.5 (Thursday, March 12, 2020 12:00 - 14:30)
- UB11.5 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: Open hardware is a possibility that has emerged in recent years and has the potential to be as disruptive as Linux was once, an open source software paradigm. If Linux managed to lessen the dependence of users in large companies providing software and software applications, it is envisioned that hardware based on ISAs open source can do the same in their own field. In the Lagartotapeout four research institutions were involved: Centro de InvestigaciónenComputación of the Mexican IPN, Centro Nacional de Microelectrónica of the CSIC, UniversitatPolitècnica de Catalunya (UPC) and Barcelona Supercomputing Center (BSC). As a result, many bachelor, master and PhD students had the chance to achieve real-world experience with ASIC design and achieve a functional SoC. In the booth, you will find a live demo of the first ASIC and prototypes running on FPGA of the next versions of the SoC and core.*

LEARNV: LEARNV: A RISC-V BASED EMBEDDED SYSTEM DESIGN FRAMEWORK FOR EDUCATION AND RESEARCH DEVELOPMENT

Authors:
Noureddine Ait Said and Mounir Benabdenbi, TIMA Laboratory, FR

Timeslots:

- UB03.5 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.5 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB06.8 (Wednesday, March 11, 2020 12:00 - 14:00)
- UB08.5 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB11.7 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: Designing a modern System on a Chip is based on the joint design of hardware and software (co-design). However, understanding the tight relationship between hardware and software is not straightforward. Moreover to validate new concepts in SoC design from the idea to the hardware implementation is time-consuming and often slowed by legacy issues (intellectual property of hardware blocks and expensive commercial tools). To overcome these issues we propose to use the open-source Rocket Chip environment for educational purposes, combined with the open-source LowRisc architecture to implement a custom SoC design on an FPGA board. The demonstration will present how students and engineers can take benefit from the environment to deepen their knowledge in HW and SW co-design. Using the LowRisC architecture, an image classification application based on the use of CNNs will serve as a demonstrator of the whole open-source hardware and software flow and will be mapped on a Nexys A7 FPGA board.*

MDD-COP: A PRELIMINARY TOOL FOR MODEL-DRIVEN DEVELOPMENT EXTENDED WITH LAYER DIAGRAM FOR CONTEXT-ORIENTED PROGRAMMING

Authors:
Harumi Watanabe[1], Chinatsu Yamamoto[1], Takeshi Ohkawa[1], Mikiko Sato[1], Nobuhiko Ogura[2] and Mana Tabei[1]
[1]Tokai University, JP; [2]Tokyo City University, JP

Timeslots:

- UB07.10 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB08.10 (Wednesday, March 11, 2020 16:00 - 18:00)

***Abstract**: This presentation introduces a preliminary tool for Model-Driven development (MDD) to generate programs for Context-Oriented Programming (COP). In modern embedded systems such as IoT and Industry 4.0, their software began to process multiple services by following the changing surrounding environments. COP is helpful for programming such software. In COP, we can consider the surrounding environments and multiple services as contexts and layers. Even though MDD is a powerful technique for developing such modern systems, the works of modeling for COP are limited. There are no works to mention the relation between UML (Unified Modeling Language) and COP. To solve this problem, we provide a COP generation from a layer diagram extended the package diagram of UML by stereotypes. In our approach, users draw a layer diagram and other UML diagrams, then xtUML, which is a major tool of MDD, generates XML code with layer information for COP; finally, our tool generates COP code from XML code.*

PA-HLS: HIGH-LEVEL ANNOTATION OF ROUTING CONGESTION FOR XILINX VIVADO HLS DESIGNS

Authors:
Osama Bin Tariq[1], Junnan Shan[1], Luciano Lavagno[1], Georgios Floros[2], Mihai Teodor Lazarescu[1], Christos Sotiriou[2] and Mario Roberto Casu[1]
[1]Politecnico di Torino, IT; [2]University of Thessaly, GR

Timeslots:

- UB07.9 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB08.9 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB09.9 (Thursday, March 12, 2020 10:00 - 12:00)
- UB10.9 (Thursday, March 12, 2020 12:00 - 14:30)

***Abstract**: We will demo a novel high-level backannotation flow that reports routing congestion issues at the C++ source level by analyzing reports from FPGA physical design (Xilinx Vivado) and internal debugging files of the Vivado HLS tool. The flow annotates the C++ source code, identifying likely causes of congestion, e.g., on-chip memories or the DSP units. These shared resources often cause routing problems on FPGAs because they cannot be duplicated by physical design. We demonstrate on realistic large designs how the information provided by our flow can be used to both identify congestion issues at the C++ source level and solve them using HLS directives. The main demo steps are: 1-Extraction of the source-level debugging information from the Vivado HLS database 2-Generation of a list of net names involved in congestion areas and of their relative significance from the Vivado post global-routing database 3-Visualization of the C++ code lines that contribute most to congestion*

PAFUSI: PARTICLE FILTER FUSION ASIC FOR INDOOR POSITIONING

Authors:
Christian Schott, Marko Rößler, Daniel Froß, Marcel Putsche and Ulrich Heinkel, TU Chemnitz, DE

Timeslots:

- UB03.3 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB09.3 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: The meaning of data acquired from IoT devices is heavily enhanced if global or local position information of their acquirement is known. Infrastructure for indoor positioning as well as the IoT device involve the need of small, energy efficient but powerful devices that provide the location awareness. We propose the PAFUSI, a hardware implementation of an UWB position estimation algorithm that fulfils these requirements. Our design fuses distance measurements to fixed points in an environment to calculate the position in 3D space and is capable of using different positioning technologies like GPS, DecaWave or Nanotron as data source simultaneously. Our design comprises of an estimator which processes the data by means of a Sequential Monte Carlo method and a microcontroller core which configures and controls the measurement unit as well as it analyses the results of the estimator. The PAFUSI is manufactured as a monolithic integrated ASIC in a multi-project wafer in UMC's 65nm process.*

PARALLEL ALGORITHM FOR CNN INFERENCE AND ITS AUTOMATIC SYNTHESIS

Authors:
Takashi Matsumoto, Yukio Miyasaka, Xinpei Zhang and Masahiro Fujita, University of Tokyo, JP

Timeslots:

- UB01.4 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB05.9 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB09.6 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: Recently, Convolutional Neural Network (CNN) has surpassed conventional methods in the field of image processing. This demonstration shows a new algorithm to calculate CNN inference using processing elements arranged and connected based on the topology of the convolution. They are connected in mesh and calculate CNN inference in a systolic way. The algorithm performs the convolution of all elements with the same output feature in parallel. We demonstrate a method to automatically synthesize an algorithm, which simultaneously performs the convolution and the communication of pixels for the computation of the next layer. We show with several sizes of input layers, kernels, and strides and confirmed that the correct algorithms were synthesized. The synthesis method is extended to the sparse kernel. The synthesized algorithm requires fewer cycles than the original algorithm. There were the more chances to reduce the number of cycles with the sparser kernel.*

PRE-IMPACT FALL DETECTION ARCHITECTURE BASED ON NEUROMUSCULAR CONNECTIVITY STATISTICS

Authors:
Giovanni Mezzina, Sardar Mehboob Hussain and Daniela De Venuto, Politecnico di Bari, IT

Timeslots:

- UB01.9 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB02.9 (Tuesday, March 10, 2020 12:30 - 15:00)

***Abstract**: In this demonstration, we propose an innovative multi-sensor architecture operating in the field of pre-impact fall detection (PIFD). The proposed architecture jointly analyzes cortical and muscular involvement when unexpected slippages occur during steady walking. The EEG and EMG are acquired through wearable and wireless devices. The control unit consists of an STM32L4 microcontroller and a Simulink modeling. The μC implements the EMG computation, while the cortical analysis and the final classification were entrusted to the Simulink model. The EMG computation block translates EMGs into binary signals, which are used both to enable cortical analyses and to extract a score to distinguish "standard" muscular behaviors from anomalous ones. The Simulink model evaluates the cortical responsiveness in five bands of interest and implements the logical-based network classifier. The system, tested on 6 healthy subjects, shows an accuracy of 96.21% and a detection time of ~371 ms.*

RESCUED: A RESCUE DEMONSTRATOR FOR INTERDEPENDENT ASPECTS OF RELIABILITY, SECURITY AND QUALITY TOWARDS A COMPLETE EDA FLOW

Authors:
Nevin George[1], Guilherme Cardoso Medeiros[2], Junchao Chen[3], Josie Esteban Rodriguez Condia[4],

Thomas Lange[5], Aleksa Damljanovic[4], Raphael Segabinazzi Ferreira[1], Aneesh Balakrishnan[5], Xinhui Lai[6], Shayesteh Masoumian[7], Dmytro Petryk[3], TroyaCagil Koylu[2], Felipe Augusto da Silva[8], Ahmet Cagri Bagbaba[8], CemilCem Gürsoy[6], Said Hamdioui[2], Mottaqiallah Taouil[2], Milos Krstic[3], Peter Langendoerfer[3], Zoya Dyka[3], Marcelo Brandalero[1], Michael Hübner[1], Jörg Nolte[1], Heinrich Theodor Vierhaus[1], Matteo Sonza Reorda[4], Giovanni Squillero[4], Luca Sterpone[4], Jaan Raik[6], Dan Alexandrescu[5], Maximilien Glorieux[5], Georgios Selimis[7], Geert-Jan Schrijen[7], Anton Klotz[8], Christian Sauer[8] and Maksim Jenihhin[6]
[1]Brandenburg University of Technology Cottbus-Senftenberg, DE; [2]TU Delft, NL; [3]Leibniz-Institut für innovative Mikroelektronik, DE; [4]Politecnico di Torino, IT; [5]IROC Technologies, FR; [6]Tallinn University of Technology, EE; [7]Intrinsic ID, NL; [8]Cadence Design Systems GmbH, DE

Timeslots:

- UB09.2 (Thursday, March 12, 2020 10:00 - 12:00)
- UB10.2 (Thursday, March 12, 2020 12:00 - 14:30)

***Abstract**: The demonstrator highlights the various interdependent aspects of Reliability, Security and Quality in nanoelectronics system design within an EDA toolset and a processor architecture setup. The compelling need of attention towards these three aspects of nanoelectronic systems have been ever more pronounced over extreme miniaturization of technologies. Further, such systems have exploded in numbers with IoT devices, heavy and analogous interaction with the external physical world, complex safety-critical applications, and Artificial intelligence applications. RESCUE targets such aspects in the form, Reliability (functional safety, ageing, soft errors), Security (tamper-resistance, PUF technology, intelligent security) and Quality (novel fault models, functional test, FMEA/FMECA, verification/debug) spanning the entire hardware software system stack. The demonstrator is brought together by a group of PhD students under the banner of H2020-MSCA-ITN RESCUE European Union project.*

RETINE: A PROGRAMMABLE 3D STACKED VISION CHIP ENABLING LOW LATENCY IMAGE ANALYSIS

Authors:
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Timeslots:

- UB07.4 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB08.7 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB10.3 (Thursday, March 12, 2020 12:00 - 14:30)

***Abstract**: We have developed and fabricated a 3D stacked imager called RETINE composed with 2 layers based on the replication of a programmable 3D tile in a matrix manner providing a highly parallel programmable architecture. This tile is composed by a 16x16 BSI binned pixels array with associated readout and 16 column ADC on the first layer coupled to an efficient SIMD processor of 16 PE on the second layer. The prototype of RETINE achieves high video rates, from 5500 fps in binned mode to 340 fps in full resolution mode. It operates at 80 MHz with 720 mW power consumption leading to 85 GOPS/W power efficiency. To highlight the capabilities of the RETINE chip we have developed a demonstration platform with an electronic board embedding a RETINE chip that films rotating disks. Three scenarii are available: high speed image capture, slow motion and composed image capture with parallel processing during acquisition.*

RUMORE: A FRAMEWORK FOR RUNTIME MONITORING AND TRACE ANALYSIS FOR COMPONENT-BASED EMBEDDED SYSTEMS DESIGN FLOW

Authors:
Vittoriano Muttillo[1], Luigi Pomante[1], Giacomo Valente[1], Hector Posadas[2], Javier Merino[2] and Eugenio Villar[2]
[1]University of L'Aquila, IT; [2]University of Cantabria, ES

Timeslots:

- UB03.9 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.9 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB11.9 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: The purpose of this demonstrator is to introduce runtime monitoring infrastructures and to analyze trace data. The goal is to show the concept among different monitoring requirements by defining a general reference architecture that can be adapted to different scenarios. Starting from design artifacts, generated by a system engineering modeling tool, a custom HW monitoring system infrastructure will be presented. This sub-system will be able to generate runtime artifacts for runtime verification. We will show how the RUMORE framework provides round-trip support in the development chain, injecting monitoring requirements from design models down to code and its execution on the platform and trace data back to the models, where the expected behavior will then compared with the actual behavior. This approach will be used towards optimizing design models for specific properties (e.g, for system performance).*

SKELETOR: AN OPEN SOURCE EDA TOOL FLOW FROM HIERARCHY SPECIFICATION TO HDL DEVELOPMENT

Authors:
Ivan Rodriguez, Guillem Cabo, Javier Barrera, Jeremy Giesen, Alvaro Jover and Leonidas Kosmidis, BSC / UPC, ES

Timeslots:

- UB01.2 (Tuesday, March 10, 2020 10:30 - 12:30)
- UB09.4 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: Large hardware design projects have high overhead for project bootstrapping, requiring significant effort for translating hardware specifications to hardware design language (HDL) files and setting up their corresponding development and verification infrastructure. Skeletor (https://github.com/jaquerinte/Skeletor) is an open source EDA tool developed as a student project at UPC/BSC, which simplifies this process, by increasing developer's productivity and reducing typing errors, while at the same time lowers the bar for entry in hardware development. Skeletor uses a C/verilog-like language for the specification of the modules in a hardware project hierarchy and their connections, which is used to generate automatically the require skeleton of source files, their development and verification testbenches and simulation scripts. Integration with KiCad schematics and support for syntax highlighting in code editors simplifies further its use. This demo is linked with workshop W05.*

SRSN: SECURE RECONFIGURABLE TEST NETWORK

Authors:
Vincent Reynaud[1], Emanuele Valea[2], Paolo Maistri[1], Regis Leveugle[1], Marie-Lise Flottes[2], Sophie Dupuis[2], Bruno Rouzeyre[2] and Giorgio Di Natale[1]
[1]TIMA Laboratory, FR; [2]LIRMM, FR

Timeslots:

- UB04.3 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB06.6 (Wednesday, March 11, 2020 12:00 - 14:00)
- UB08.6 (Wednesday, March 11, 2020 16:00 - 18:00)
- UB10.6 (Thursday, March 12, 2020 12:00 - 14:30)
- UB11.6 (Thursday, March 12, 2020 14:30 - 16:30)

***Abstract**: The critical importance of testability for electronic devices led to the development of IEEE test standards. These methods, if not protected, offer a security backdoor to attackers. This demonstrator illustrates a state-of-the-art solution that prevents unauthorized usage of the test infrastructure based on the IEEE 1687 standard and implemented on an FPGA target.*

SUBRISC+: IMPLEMENTATION AND EVALUATION OF AN EMBEDDED PROCESSOR FOR LIGHTWEIGHT IOT EHEALTH

Authors:
Mingyu Yang and Yuko Hara-Azumi, Tokyo Institute of Technology, JP

Timeslots:

- UB07.8 (Wednesday, March 11, 2020 14:00 - 16:00)
- UB09.8 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: Although the rapid growth of Internet of Things (IoT) has enabled new opportunities for eHealth devices, the further development of complex systems is severely constrained by the power and energy supply on the battery-powered embedded systems. To address this issue, this work presents a processor design called "SubRISC+" targeting lightweight IoT eHealth. SubRISC+ is a processor design to achieve low power/energy consumption through its unique and compact architecture. As an example of lightweight eHealth applications on SubRISC+, we are working on the epileptic seizure detection using the dynamic time wrapping algorithm to deploy on wearable IoT eHealth devices. Simulation results show that 22% reduction on dynamic power and 50% reduction on leakage power and core area are achieved compared to Cortex-M0. As an ongoing work, the evaluation on a fabricated chip will be done within the first half of 2020.*

SYSTEMC-CT/DE: A SIMULATOR WITH FAST AND ACCURATE CONTINUOUS TIME AND DISCRETE EVENTS INTERACTIONS ON TOP OF SYSTEMC.

Authors:
Breytner Joseph Fernandez-Mesa, Liliana Andrade and Frédéric Pétrot, Université Grenoble Alpes / CNRS / TIMA Laboratory, FR

Timeslots:

- UB06.4 (Wednesday, March 11, 2020 12:00 - 14:00)
- UB09.5 (Thursday, March 12, 2020 10:00 - 12:00)

***Abstract**: We have developed a continuous time (CT) and discrete events (DE) simulator on top of SystemC. Systems that mix both domains are critical and their proper functioning must be verified. Simulation serves to achieve this goal. Our simulator implements direct CT/DE synchronization, which enables a rich set of interactions between the domains: events from the CT models are able to trigger DE processes; events from the DE models are able to modify the CT equations. DE-based interactions are, then, simulated at their precise time by the DE kernel rather than at fixed time steps. We demonstrate our simulator by executing a set of challenging examples: they either require a superdense model of time or include Zeno behavior or are highly sensitive to accuracy errors. Results show that our simulator overcomes these issues, is accurate, and improves simulation speed w.r.t. fixed time steps; all of these advantages open up new possibilities for the design of a wider set of heterogeneous systems.*

TAPASCO: THE OPEN-SOURCE TASK-PARALLEL SYSTEM COMPOSER FRAMEWORK

Authors:
Carsten Heinz, Lukas Sommer, Lukas Weber, Jaco Hofmann and Andreas Koch, TU Darmstadt, DE

Timeslots:

- UB05.1 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB09.1 (Thursday, March 12, 2020 10:00 - 12:00)
- UB10.1 (Thursday, March 12, 2020 12:00 - 14:30)

***Abstract**: Field-programmable gate arrays (FPGA) are an established platform for highly specialized accelerators, but in a heterogeneous setup, the accelerator still needs to be integrated into the overall system. The open-source TaPaSCo (Task-Parallel System Composer) framework was created to serve this purpose: The fast integration of FPGA-based accelerators into compute platforms or systems-on-chip (SoC) and their connection to relevant components on the FPGA board. TaPaSCo can support developers in all steps of the development process: from cores resulting from High-Level Synthesis or cores written in an HDL, a complete FPGA-design can be created. TaPaSCo will automatically connect all processing elements to the memory- and host-interface and generate a complete bitstream. The TaPaSCo Runtime API allows to interface with accelerators from software and supports operations such as transferring data to the FPGA memory, passing values and controlling the execution of the accelerators.*

UWB ACKATCK: HIJACKING DEVICES IN UWB INDOOR POSITIONING SYSTEMS

Authors:
Baptiste Pestourie, Vincent Beroulle and Nicolas Fourty, Université Grenoble Alpes, FR

Timeslots:

- UB05.5 (Wednesday, March 11, 2020 10:00 - 12:00)
- UB07.5 (Wednesday, March 11, 2020 14:00 - 16:00)

***Abstract**: Various radio-based Indoor Positioning Systems (IPS) have been proposed during the last decade as solutions to GPS inconsistency in indoor environments. Among the different radio technologies proposed for this purpose, 802.15.4 Ultra-Wideband (UWB) is by far the most performant, reaching up to 10 cm accuracy with 1000 Hz refresh rates. As a consequence, UWB is a popular technology for applications such as assets tracking in industrial environments or robots/drones indoor navigation. However, some security flaws in 802.15.4 standard expose UWB positioning to attacks. In this demonstration, we show how an attacker can exploit a vulnerability on 802.15.4 acknowledgment frames to hijack a device in a UWB positioning system. We demonsrate that using simply one cheap UWB chip, the attacker can take control over the positioning system and generate fake trajectories from a laptop. The results are observed in real-time in the 3D engine monitoring the positioning system.*

VIRTUAL PLATFORMS FOR COMPLEX SOFTWARE STACKS

Authors:
Lukas Jünger and Rainer Leupers, RWTH Aachen University, DE

Timeslots:

- UB02.3 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB06.3 (Wednesday, March 11, 2020 12:00 - 14:00)

***Abstract**: This demonstration is going to showcase our "AVP64" Virtual Platform (VP), which models a multi-core ARMv8 (Cortex A72) system including several peripherals, such as an SDHCI and an ethernet controller. For the ARMv8 instruction set simulation a dynamic binary translation based solution is used. As the workload, the Xen hypervisor with two Linux Virtual Machines (VMs) is executed. Both VMs are connected to the simulation hosts' network subsystem via a virtual ethernet controller. One of the VMs executes a NodeJS-based server application offering a REST API via this network connection. An AngularJS client application on the host system can then connect to the server application to obtain and store data via the server's REST API. This data is read and written by the server application to the virtual SD Card connected to the SDHCI. For this, on SD card partition is passed to the VM through Xen's block device virtualization mechanism.*

WALLANCE: AN ALTERNATIVE TO BLOCKCHAIN FOR IOT

Authors:
Loic Dalmasso, Florent Bruguier, Pascal Benoit and AchrafLamlih, Université de Montpellier, FR

Timeslots:

- UB02.8 (Tuesday, March 10, 2020 12:30 - 15:00)
- UB03.8 (Tuesday, March 10, 2020 15:00 - 17:30)
- UB04.8 (Tuesday, March 10, 2020 17:30 - 19:30)
- UB06.9 (Wednesday, March 11, 2020 12:00 - 14:00)

***Abstract**: Since the expansion of the Internet of Things (IoT), connected devices became smart and autonomous. Their exponentially increasing number and their use in many application domains result in a huge potential of cybersecurity threats. Taking into account the evolution of the IoT, security and interoperability are the main challenges, to ensure the reliability of the information. The blockchain technology provides a new approach to handle the trust in a decentralized network. However, current blockchain implementations cannot be used in IoT domain because of their huge need of computing power and storage utilization. This demonstrator presents a lightweight distributed ledger protocol dedicated to the IoT application, reducing the computing power and storage utilization, handling the scalability and ensuring the reliability of information.*

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About DATE

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