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Wide dynamic range multichannel lock-in amplifier for contactless optical sensors with sub-pS resolution

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***Abstract*—A multichannel impedance-sensing CMOS chip for the readout of non-invasive light detectors in Silicon Photonics is presented. The performance of the lock-in phase-sensitive demodulator is improved thanks to a capacitive feedback transimpedance amplifier (TIA) equipped with an active discharge network, able to keep a DC output offset lower than $3\,\mathrm{mV}$ for leakage currents up to $4\,\mathrm{nA}$ while injecting a noise lower than $40\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$. The addition of a sensor capacitance compensation system at the input of the chip allows a 30-fold increase of the stimulation amplitude, enabling the tracking of sub-picoSiemens conductance variations on a baseline of few $\mu\mathrm{S}$, with a bandwidth of $70\,\mathrm{Hz}$. The chip performance opens the way to multipoint monitoring of complex photonic systems, addressing the challenges posed by the growing complexity of these architectures.**

***Index Terms*—Integrated photonics, low-noise, transimpedance amplifier, lock-in front-end, microsensors.**

I. Introduction

The possibility of integrating a large number of optical devices in a single Silicon Photonics (SiP) chip is enabling the design of complex optical architectures in a very small footprint, that promise to bring optical communications to short and ultrashort distances and open the possibility of all-optical signal processing [1]. However, the integration density made possible by Silicon Photonics revealed the difficulty of operating complex optical architectures in an open-loop fashion, due to their high sensitivity to fabrication parameters and temperature variations. Local light monitoring and active control of each photonic device thus emerged as strong requirements to correctly operate complex optical systems. In this context, a key enabling technology is the ContactLess Integrated Photonic Probe (CLIPP), a non-invasive detector [2] that senses light in silicon waveguides just by exploiting their natural losses. Due to sub-bandgap absorption, light propagating in a silicon waveguide generates a small number of free carriers, changing the electrical conductivity of the core. By placing a couple of metal electrodes on top of the oxide cladding (Fig. 1a), stimulated at a frequency between $100\,\mathrm{kHz}$ and $10\,\mathrm{MHz}$ depending on the sensor geometry, the local light intensity can be assessed by capacitively measuring the conductance of the waveguide core with the lock-in technique, i.e. by homodyne detection, that allows to reconstruct the complex admittance of the sensor. The conductance of the waveguide is in the order of $1\,\mathrm{nS}$ [2], so a resolution better than $10\,\mathrm{pS}$ is targeted to monitor the optical power in photonic devices with an accuracy below $-30\,\mathrm{dBm}$. In order to sense such small admittance variations, CMOS integration of the sensor electronic readout is required. Indeed, an integrated solution allows to directly wire-bond the photonic chip to the electronic one and reduce the stray capacitances, with a beneficial effect on the readout signal-to-noise ratio (SNR). In addition, the small size and multichannel operation offered by the CMOS integration enables the control of many photonic devices in a compact footprint.

Figure 1a schematically shows the CMOS read-out system proposed in the recent past for this application [3], successfully addressing the requirements of bandwidth and noise by using a capacitive TIA with a high-value pseudo-resistor to set its DC bias. However, experimental demonstrations highlighted two peculiar aspects that arise from operating an electronic chip to control a photonic system placed in close proximity. The first is related to photons leaking from the SiP chip and from the surrounding environment, that produce leakage currents at the input node of the TIA up to the nA range, causing a significant DC offset (hundreds of mV) at the output due to the large feedback resistance required to satisfy the noise constraint. Although such constant value is ideally cancelled by the following demodulation and filtering of the lock-in detector, a spurious DC contribution arises due to mismatches in the mixer structure and clock non-idealities,

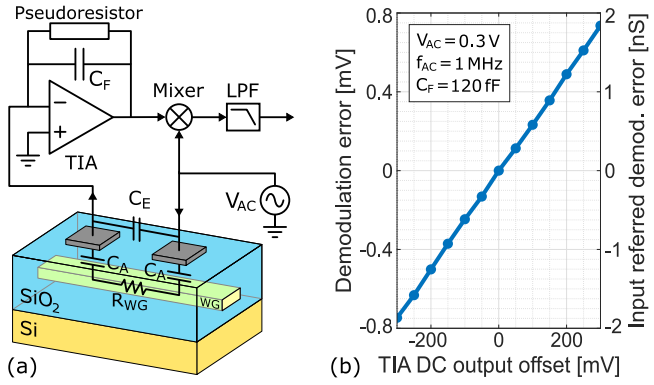

Fig. 1. (a) CLIPP detector structure and its readout scheme. (b) Measured demodulation error as function of the TIA DC output offset.

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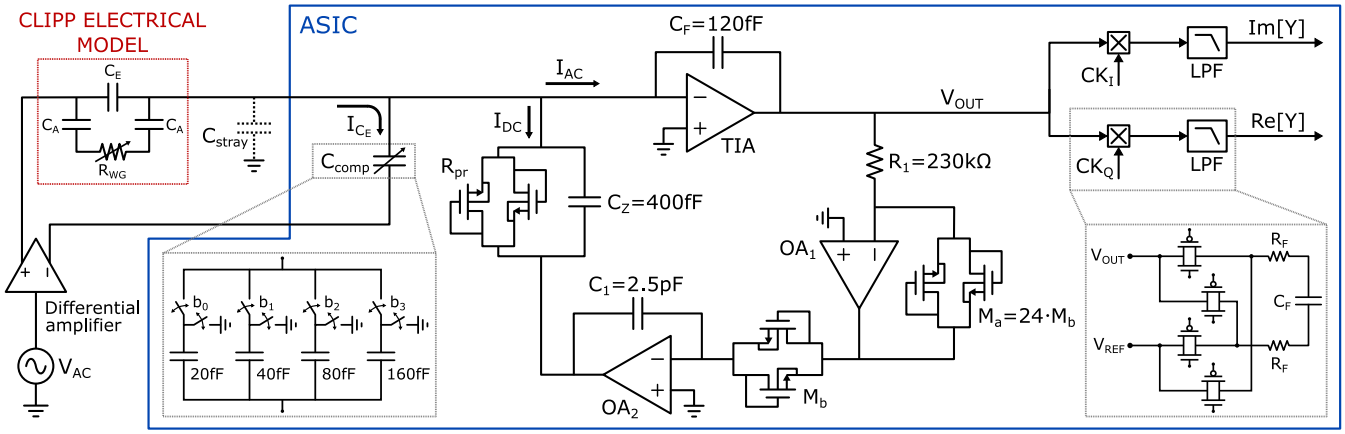

Fig. 2. Schematic of the proposed low-noise wide-bandwidth lock-in front-end. An active network removes leakage currents from the virtual ground, while a tunable capacitor C_{comp} steers the spurious capacitive current of the sensor away from the amplifier, allowing a larger stimulation.

that unbalance the demodulating signal. Since the magnitude of the leakage current depends on parasitic photo-generation, a time-varying output error of about $1\,\mathrm{mV}$ is generated (Fig. 1b), easily comparable with the signals to be detected. The second peculiar aspect of this application comes from the parasitic capacitance between the sensor electrodes, indicated as C_E in Fig. 1a, ranging from 10 to 300 fF depending on the geometry of the sensor and on the positioning of the bonding pads on the SiP chip. This stray coupling causes a spurious AC current up to three orders of magnitude higher than the signal given by the waveguide resistance R_{WG}, limiting the sensor stimulation amplitude and the AC gain before the demodulation and thus setting the maximum accuracy of the measurement.

This paper addresses both these specific aspects with the design of a new capacitive TIA that features an active discharge network able to keep the output offset lower than few millivolts for DC currents up to some nA, allowing an optimal operation of the demodulator. The addition of a sensor capacitance compensation system also allows to increase the stimulation amplitude without saturating the amplifier, leading to significant improvement in the readout resolution.

II. Integrated Circuit Architecture

Fig. 2 shows the architecture of a single readout channel. The TIA operational amplifier was designed with a low-noise resistively loaded nMOS input stage, followed by a folded-cascode topology and a rail-to-rail output stage [3]. The input capacitance $C_{in} = 1.6\,\mathrm{pF}$ of the amplifier matches the expected stray capacitance on the virtual ground, in order to minimize the noise of the TIA [4]. The feedback capacitor was set to $120\,\mathrm{fF}$ to provide a sufficiently high gain, so the closed-loop bandwidth requirement was satisfied by setting the GBWP of the amplifier to around $2\,\mathrm{GHz}$. The designed amplifier features a series white noise $S_v = 2.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ with a corner frequency of $300\,\mathrm{kHz}$ and a bandwidth higher than $80\,\mathrm{MHz}$.

A. Active DC handling network

The DC bias of the capacitive TIA is ensured by a servo loop in parallel to the feedback capacitor C_F that provides an alternative path for the leakage currents on the virtual ground, thus preventing them from reaching the output and creating a DC offset. Since the TIA is conceived to read a capacitively coupled sensor operated at a frequency larger than $100\,\mathrm{kHz}$, the servo loop was designed to compensate leakage currents of up to some nA, with a closed-loop bandwidth of around $35\,\mathrm{kHz}$. The structure is made of an integrator (OA_2), that filters out the high-frequency oscillations of the TIA output and amplifies its DC component, and a high-value pseudo-resistor (R_{pr}), driven to generate the DC reaction current that compensates the leakages on the virtual ground. In order to obtain an integrator with a large time constant without using bulky components, an active structure based on a current reducer (M_a, M_b, OA_1) was used to synthesize a high-value equivalent resistance. The core of this system is the pair of matched nMOS pseudo-resistors M_a and M_b, connected with source and well short circuited. By designing M_a N-times larger than M_b, the overall system acts as a linear and accurate current reducer of a factor N [4]. A physical resistor of $R_1 = 230\,\mathrm{k\Omega}$ was thus used to linearly convert the output voltage of the TIA into a current, then reduced of a factor N by the active structure to obtain an equivalent resistance of $N \cdot R_1$.

The pseudo-resistor R_{pr} was obtained by using a pair of back-to-back diode connected nMOS, with the bulk short-circuited to the source, to ensure very low injection of noise and symmetric behaviour for both positive and negative DC currents [5]. Since the pseudo-resistor is made by MOS transistors operating in sub-threshold, its equivalent small signal resistance R_{pr} changes with the DC input current I_{DC}, according to the relation $R_{pr} = n \cdot V_{th}/I_{DC}$, where V_{th} is the thermal voltage and $n \approx 1.5$ is the sub-threshold coefficient. In order to obtain a closed-loop bandwidth of $35\,\mathrm{kHz}$ irrespective of R_{pr} and I_{DC}, a capacitor C_Z was added in parallel to the pseudo-resistor to provide a well-defined loop gain at medium frequency. The capacitor also introduces a low frequency zero that stabilizes the loop gain, whose approximated expression is:

$$G_{LOOP}(s) = -\frac{1 + sC_Z R_{pr}}{s^2 C_1 C_F N R_1 R_{pr}} \qquad (1)$$

assuming the TIA gain ideal and equal to $-1/sC_F$. The closed-loop bandwidth of the DC control system can be computed as:

$$f_{CL} = \frac{1}{2\pi C_1 N R_1} \cdot \frac{C_Z}{C_F} \tag{2}$$

By selecting $C_Z = 400\,\text{fF}$, a phase margin greater than $45°$ is ensured for input currents up to $3.5\,\text{nA}$. The $35\,\text{kHz}$ bandwidth requirement was instead satisfied by choosing a current reduction factor N equal to 24 and a value of $C_1 = 2.5\,\text{pF}$.

B. Sensor capacitance compensation system

In the frequency range of interest, the CLIPP admittance is dominated by the stray coupling C_E between the electrodes, that generates a signal much larger than the one of interest represented by small variations of the waveguide resistance R_{WG}. This limits the maximum amplitude that can be applied to the sensor without saturating the amplifier and consequently the SNR of the measurement. To mitigate this issue, a capacitance compensation system was added to the circuit. A programmable capacitor, driven in counter-phase with respect to the main stimulation, is connected to the virtual ground of the amplifier to steer away the capacitive current of the sensor without affecting the resistive one. The value of the compensation can be tuned to match the value of C_E with a 4-bit digital-to-capacitance converter (DCC), that connects a bank of capacitors to the virtual ground by means of digitally controlled switches. The LSB of the structure was set to $20\,\text{fF}$, to limit to just $10\,\text{fF}$ the maximum residual error of the compensation and allow the application of up to $10\,\text{V}$ across the sensor. Metal-oxide-metal (MOM) capacitors were used, as they can provide very low and precise value of capacitance with reduced process deviation, as compared to polysilicon capacitors. The maximum capacitance that can be connected to the virtual ground was limited to $300\,\text{fF}$, in order not to introduce too much additional noise due to the increased capacitive load at the TIA input. Nevertheless, with this configuration, for a C_E of $300\,\text{fF}$, the compensation system allows to increase the sensor stimulation amplitude of at least a factor 30 without saturating the amplifier, leading to a corresponding improvement of the SNR.

C. Double-balanced passive mixer

The lock-in front-end is completed by a couple of double-balanced passive mixers based on transmission gates [3], that provide in-phase and quadrature demodulation of the TIA output to reconstruct the complex admittance of the sensor. Passive mixers were preferred over more complex active structures because of their lower $1/f$ noise and output offset, that affect the low frequency signals at the output of the demodulator. The degradation of SNR due to the folding of high-frequency noise components generated by the square-wave mixing is here mitigated by the use of a capacitive TIA. Thanks to a gain that decreases with frequency, the noise spectrum at the output of the TIA is basically white, so the SNR of the measurement is worsened only by 10% with respect to the case of a sinusoidal multiplier. An on-chip passive RC low-pass filter with $1\,\text{MHz}$ cut-off frequency was incorporated at the output of the mixer, to reduce the crosstalk between the two I/Q mixers and the injection of spurs during the commutations. Additional filters are implemented off-chip in the digital domain to easily change the lock-in bandwidth.

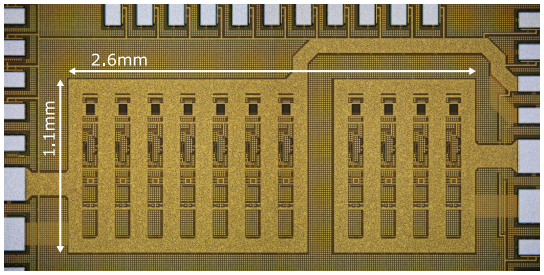

Fig. 3. Micro-photograph of the 11-channel fabricated chip.

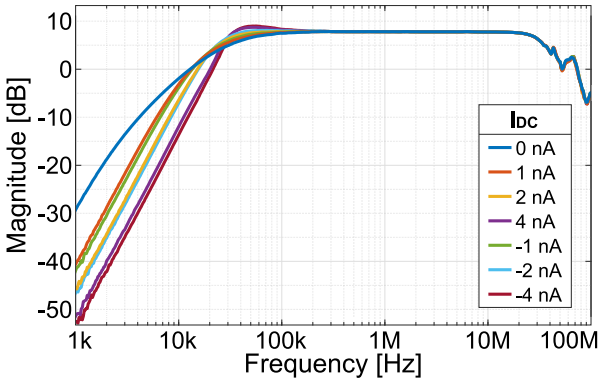

Fig. 4. Transfer function of the TIA for different values of DC leakage current.

III. Experimental Results

The proposed lock-in front-end featuring 11 parallel channels was designed and fabricated in STMicroelectronics BCD8sP $0.18\,\mu\text{m}$ technology, with a supply voltage of $1.8\,\text{V}$, an area occupation of $2.6\,\text{mm}$ x $1.1\,\text{mm}$ without pads (Fig. 3) and a current consumption of $5\,\text{mA}$ per channel.

The transfer function of the amplifier (Fig. 4) was measured by applying a voltage signal to a $0.3\,\text{pF}$ capacitor connected to the virtual ground. A $5\,\text{G}\Omega$ external resistor was used to inject an arbitrary DC current to the input node, to observe the behaviour of the circuit for different values of leakage. As expected, the behaviour of the amplifier in the signal bandwidth $100\,\text{kHz} - 10\,\text{MHz}$ is independent of the injected DC current, with an high frequency limit of $35\,\text{MHz}$ given by the capacitive load on the virtual ground of around $6\,\text{pF}$ in these experimental conditions. In agreement with the analysis of Sec. II-A, the frequency of the servo loop zero changes with the DC current but stability is correctly preserved for currents up to $4\,\text{nA}$ irrespective of the current sign.

The noise of the circuit (Fig. 5) was measured at the output of the TIA and referred to the input of the amplifier by dividing it for its transfer function. At low frequency, the dominant noise contribution is the shot noise of the pseudo-resistor R_{pr}, operating in sub-threshold regime [6]. Consequently, a different noise level is observed when changing the input DC

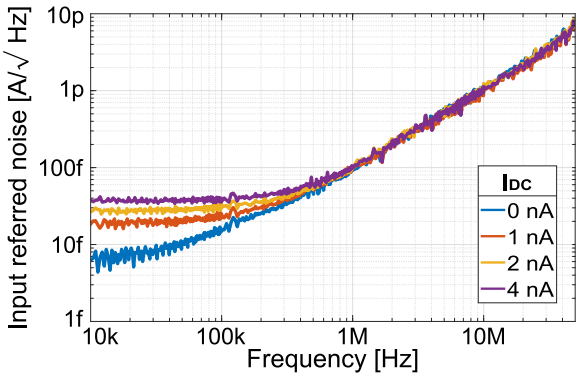

Fig. 5. Equivalent input current noise of the circuit for different values of DC leakage current, for an overall 6 pF capacitive load on the virtual ground.

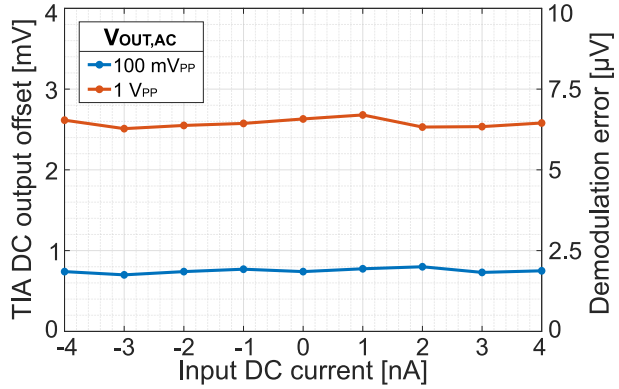

Fig. 6. DC offset at the output of the TIA as a function of the leakage current.

current, with a value of $40\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ in case of maximum leakage. At higher frequency, the noise of the transimpedance amplifier, shaped by the total capacitance on the virtual ground and proportional to ω, becomes dominant.

The effectiveness of the DC handling network was assessed by monitoring the TIA output offset as a function of the leakage current, for two different amplitudes of the output AC signal (Fig. 6). A symmetric behaviour was again observed for both positive and negative DC currents, with the network able to keep the offset lower than $3\,\mathrm{mV}$ in all the explored conditions, leading to a constant and negligible demodulation error. The small increase when a large AC signal is present is caused by the non-linear characteristics of the pseudo-resistors M_a and M_b. Due to the different offset voltages of operational amplifiers OA_1 and OA_2, the two pseudo-resistors have a slightly different bias point, so when a zero average sinusoidal current is injected in M_a through R_1, the reduced version flowing in M_b has a non-zero mean value. Since the loop works to minimize the DC current through M_b, the average value of V_{OUT} needs to move to counterbalance such effect, generating a small offset at the output of the TIA.

The effect of the capacitance compensation system was measured by applying a $500\,\mathrm{kHz}$ signal to a $120\,\mathrm{fF}$ capacitor connected at the input of the TIA. Fig. 7a reports the characterization of the digital-to-capacitance converter, that showed a linear behaviour with a differential non-linearity lower than $2\,\mathrm{fF}$, equivalent to 0.1 LSB. Fig. 7b highlights the measured

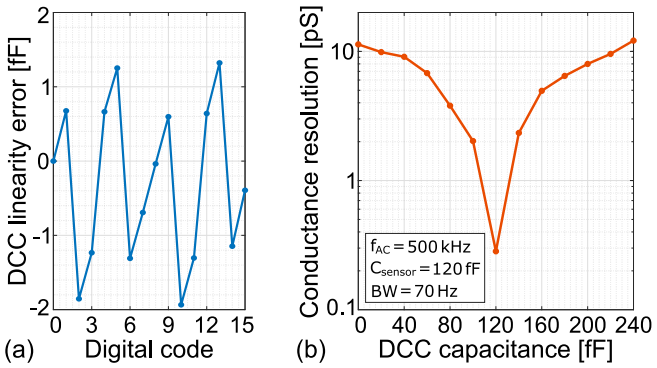

Fig. 7. (a) Measured differential non-linearity of the DCC. (b) Conductance resolution of the lock-in front-end as a function of the DCC capacitance.

conductance resolution of the lock-in front-end as a function of the DCC compensation. The measurement was performed by adjusting the stimulation amplitude for each selected DCC capacitance value, trying to keep the TIA output signal to a constant value of $200\,\mathrm{mV}$ in all conditions. The compensation system allowed to increase the stimulation from $200\,\mathrm{mV}$ to $9\,\mathrm{V}$ when selecting a $120\,\mathrm{fF}$ capacitance, improving the resolution of the measurement and enabling the tracking of conductance variations down to $300\,\mathrm{fS}$ with a lock-in bandwidth of $70\,\mathrm{Hz}$, confirming the effectiveness of the proposed approach.

IV. Conclusions

This paper presented a 11-channel lock-in system for contactless optical detectors in silicon photonics. A new active discharge network guarantees an output offset of the capacitive TIA lower than $3\,\mathrm{mV}$ for DC currents up to $4\,\mathrm{nA}$, while introducing a negligible noise in the signal bandwidth. A sensor capacitance compensation system allows a resolution improvement of a factor 30, enabling the detection of admittance variations down to $300\,\mathrm{fS}$ on a baseline of few µS at $500\,\mathrm{kHz}$, with a bandwidth of $70\,\mathrm{Hz}$. The proposed approach can be extended to all those situations requiring contactless investigation of nanosamples and sensors with very high resolution [7], [8].

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