Wide-area fast-gated single-photon detector with integrated TDC for near-infrared spectroscopy applications

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Time-Domain Near-Infrared Spectroscopy (TD-NIRS) is a powerful technique for estimating the composition and microstructure of biological tissues and other highly scattering media, down to a depth of few centimetres, by retrieving the optical absorption and scattering properties. According to TD-NIRS, laser pulses are injected into the sample and the diffused photons are collected by a single-photon detector [1]. TD-NIRS can take advantage of the so-called "fast time-gated acquisition" technique, combined with a short source-detector distance [1]. However, up to now, TD-NIRS instruments have been quite bulky and expensive.

Here, we present a silicon integrated circuit designed for compact and low-cost TD-NIRS systems, combining a fast-gated single-photon detector array (based on SPADs) with 8.6 mm^2 active area, a Time-to-Digital Converter (TDC) with 72 ps resolution and integrated histogram builder, a gate window generator and a serial interface (for easy communication with low-cost microcontrollers). The chip has been fabricated in a 0.35 µm CMOS technology and it is designed to fit inside a small standalone module (few cm^3 of volume), together with 8 pulsed diode lasers of different wavelengths, in order to build an extremely compact TD-NIRS system with low power consumption. This fully-digital photodetector combines the fast-gating capability of SPAD detectors, previously only demonstrated for single pixels [2], with the large area typically found in detectors like Silicon Photomultipliers (SiPMs). It is therefore called "fast-gated digital SiPM". It allows highly-sensitive time-gated measurements with extended dynamic range (thanks to more than 1700 microcells). Each microcell can be individually disabled either for reducing the overall noise or for adjusting the sensitive area, in order to equalize the signal directly on chip.

Common fast-gating approaches couple a SPAD to a "dummy" device and employ a comparator to extract the avalanche signal while rejecting spurious gating feedthroughs [2]. In this new detector, in order to increase the fill-factor and reduce power consumption, we replaced the dummy structure with a second SPAD and the comparator with a digital XOR gate. We reach a fill-factor of 37% and a maximum gating frequency of 100 MHz. The TDC adopts a Vernier delay line architecture and reaches 72 ps resolution with a Full-Scale Range (FSR) of 9.2 ns, while keeping the conversion time shorter than 100 ns. A 12-bit depth, 128-channel histogram builder accumulates the conversion results and minimizes the bandwidth required for transferring data. The internal gate window generator is used for synchronizing the gate window with the laser pulse. It has adjustable duration with resolution of 1 ns and a range of 24 ns. A low power mode disables the gate generation during TDC conversion.

The detector achieves a temporal response of ~ 300 ps (FWHM) and a dynamic range for gated measurements greater than 50 dB, with a rising edge of the gate window of ~ 300 ps (20% - 80%).

With this solution, TD-NIRS can widen its applications (from labs to hospitals) and even reach mass markets (e.g. in athlete training monitoring and non-destructive assessment of fruit quality).

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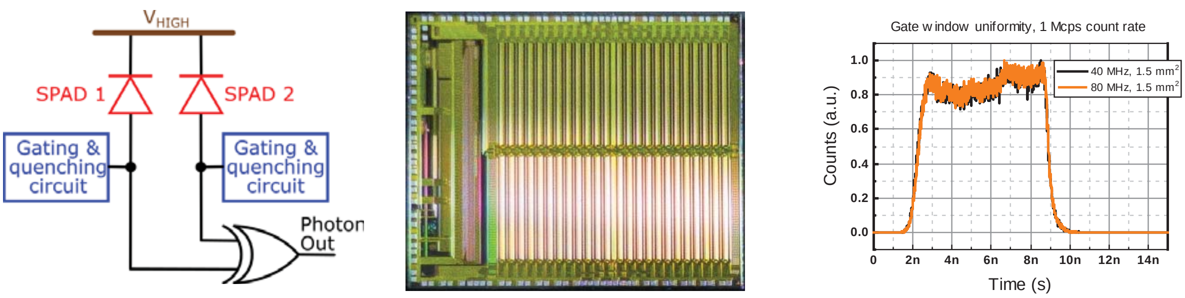

Fig. 1 Left: Microcell block diagram. Center: Fabricated chip. Right: Gate shape when 1.5 mm^2 of the active area is ON.

References

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