

Modeling Nonlinear Wave Digital Elements using the Lambert Function

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Abstract—A large class of transcendental equations involving exponentials can be made explicit using the Lambert W function. In the last fifteen years, this powerful mathematical tool has been extensively used to find closed-form expressions for currents or voltages in circuits containing diodes. Until now almost all the studies about the W function in circuit analysis concern the Kirchhoff (K) domain, while only few works in the literature describe explicit models for diode circuits in the Wave Digital (WD) domain. However explicit models of NonLinear Elements (NLEs) in the WD domain are particularly desirable, especially in order to avoid the use of iterative algorithms. This paper explores the range of action of the W function in the WD domain; it describes a procedure to search for explicit wave mappings, for both one-port and multi-port NLEs containing diodes. WD models, describing an arbitrary number of different parallel and anti-parallel diodes, a transformerless ring modulator and some BJT amplifier configurations, are derived. In particular, an extended version of the BJT Ebers–Moll model, suitable for implementing feedback between terminals, is introduced.

Index Terms—NonLinear Wave Digital Filters, Lambert Function, Diodes, Virtual Analog.

I. INTRODUCTION

WAVE Digital Filter (WDF) theory was introduced by A. Fettweis [1] in the early 70s as a method for designing digital filters through the discretization of analog circuits. A WDF is the result of a linear mapping of circuit port variables in the Kirchhoff (K) domain (voltages and currents) onto variables in the Wave Digital (WD) domain (incident and reflected waves). The presence of reactive components in the circuit also requires a bilinear transformation (from the Laplace domain to the Z domain) in the discretization process. In compliance with circuit theory, components are thought of as connected to each other through ports. A port in the K domain is characterized by a pair of signals (current I and voltage V , respectively). In the WD domain a port is described by a different pair of wave signals (incident wave a and reflected wave b , respectively). The mapping from a K pair onto a WD pair is, in fact, linear and invertible:

$$\underbrace{a = V + IR_0, b = V - IR_0}_{\text{K-WD}}, \underbrace{V = \frac{a+b}{2}, I = \frac{a-b}{2R_0}}_{\text{WD-K}}, \quad (1)$$

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where R_0 is a (non-zero) free parameter called “reference port resistance”. Modeling WD networks requires balancing such free parameters in a port-wise fashion, in order to avoid delay-free loops and make the implementation computable.

Despite the initial motivations, the interest in WDF theory has kept steadily strong throughout the decades, as it progressively shifted from filter design to circuit emulation, with numerous new applications to sound synthesis through physical modeling [2] and virtual analog modeling [3]. In the WD domain we can closely simulate the behavior of a reference circuit in a modular and efficient fashion. Moreover, unlike classical circuit simulation tools such as SPICE, WDFs ensure that many of the good properties of the analog reference circuit will be preserved. For example, passivity and losslessness of analog circuits are preserved by their WD implementation [4]. Furthermore, the behavior of a WD implementation will be insensitive to the quantization of coefficients. This means that a WD implementation will be able to offer a good dynamic range with modest accuracy requirements. In addition, the sensitivity properties of WD implementations also guarantee stability under mild conditions, producing structures that tend to exhibit neither limit cycles nor zero-input parasitic oscillations [5]. Finally, this inherent robustness makes working in the WD domain particularly suitable for interactive real-time applications, where model parameters are altered on the fly, as opposed to the off-line simulations performed by SPICE. Moreover, parameter update turns out to be easier using WD Structures (WDSs) w.r.t. other physical modeling approaches developed for real-time applications, such as the nonlinear state-space formulation, as discussed in [6]. As an example of the major complexity of parameter update using nonlinear state-space systems we refer to [7]. Originally conceived for modeling a linear circuit, WDF theory turned out to be suitable also for describing circuits containing NonLinear Elements (NLEs) without and with memory [8], [9]. In particular, relevant examples of nonlinear circuits in the WD domain for virtual analog applications involve diodes [10]–[13], vacuum tubes [14]–[17], BJTs [18], [19] as well as transformers [20].

Most classical WD implementations are tree-like structures (e.g., Binary Connection Tree [21]). The leaves of such trees are one-port linear elements, while the nodes are adaptors. There are also some circuits that exhibit special interconnection topologies resulting in WDSs that are not binary-tree-like. Such cases can be addressed using SPQR graph decomposition [19], [22]–[24], which remaps the WDS into a tree through the introduction of special (R-type) nodes. One inherent weakness of WDSs is that they can only accommodate one NLE at a

time (see [21]), which must be placed at the root of the tree. Some strategies for overcoming this limitation are described in [3] and consist, for example, of consolidating the NLEs of the reference circuit into a single multi-port NLE. A first example of application of this approach is presented in [17]. The implementation of WD multi-port NLEs, however, very often requires the solution of multidimensional systems of implicit equations, which are very hard to turn into a set of explicit WD equations. A possible remedy, adopted in [17], consists of iteratively finding a solution of the system of equations at every time step. This solution, however, is rather demanding from the computational standpoint, and the convergence of these iterative methods might raise some issues, particularly as the dimensionality of the solution space increases. For these reasons, explicit equations describing the NLE are generally preferable. One method that goes in this direction is proposed in [18] and is based on a piecewise linear approximation of the consolidated NLE. In this work we take a completely different route, seeking exact solutions for a specific class of NLEs.

In circuit theory, there exists a wide class of nonlinearities that exhibits an exponential behavior (e.g., diodes). A good property of many exponential equations is that they can be explicitly solved using the Lambert W function [25]. Banwell and Jayakumar [26] first exploited this property by finding a closed-form expression for the current that passes through a diode in series with a resistance and a voltage generator. Banwell also derived explicit solutions for currents in some circuits containing BJTs [27]. In the WD domain the W function was used in [11] to find a wave mapping of a one-port NLE representing the Shockley diode model. In this manuscript we start from Banwell's approach and explore its applicability to WD circuit models. With this purpose in mind, we define a new family of multi-port exponential NLEs characterized by explicit wave mappings.

Section II defines the W function and focuses on its use in the analysis of diode circuits. Section III describes a procedure for deriving explicit wave mappings of one-port exponential NLEs and presents a new WD model of an arbitrary bank of different parallel and anti-parallel diodes. Section IV extends the procedure of Section III to the multi-port case, by introducing a new type of port that is necessary for modeling multi-port elements. We then present a new family of multi-port exponential NLEs and describe some *Simplified Models* that are useful to widen the class of implementable circuits. Section V presents some examples of application focused on, but not limited to, audio circuitry, such as the asymmetrical electrical damper (used in envelope generation), the ring modulator (a common audio effect) and three configurations of BJT amplifiers. In particular we introduce an extended version of the Ebers–Moll model of the BJT, which is suitable for implementing the feedback between terminals. Section VI concludes this paper.

II. LAMBERT FUNCTION BACKGROUND IN DIODE CIRCUITS ANALYSIS

The so called *Lambert function* $W(z)$ is a well known set of functions of the complex variable z [25], which is implicitly

defined by the exponential equation

$$z = W(z)e^{W(z)} \quad \forall z \in \mathbb{C}. \quad (2)$$

In this work we will restrict the domain of the W function, turning z into a real variable x , so that also $W(x)$ becomes real. In particular we will exploit an application of the W function proposed in [25], which allows us to find an explicit solution of exponential equations of the form

$$p^{\theta y + \beta} = cy + d \quad (3)$$

with $p > 0$, $c, \theta \neq 0$, d and β real parameters and y a real variable. These equations, in fact, can be solved in closed form with respect to the variable y as

$$y = -\frac{W\left(-\frac{\theta \ln p}{c} p^{\beta - \frac{\theta d}{c}}\right) - \frac{d}{c}}{\theta \ln p}. \quad (4)$$

For the evaluation of $W(x)$ we suggest the same iterative approach mentioned in [11] and described in [28], as it is suitable for real time circuit simulation purposes. According to such approach we can write

$$W_{k+1}(x) = \begin{cases} \ln \frac{x}{W_k(x)} & \text{if } x \geq e \\ xe^{-W_k(x)} & \text{if } x < e \end{cases} \quad (5)$$

where $W_{k+1}(x)$ is an improved solution w.r.t. $W_k(x)$ and $k = 0, 1, 2 \dots$ is the iteration index. The initial values $W_0(x)$ can be precisely computed using mathematical softwares, e.g. MATLAB or Mathematica, and then tabulated in a lookup table with the needed granularity. This iterative approach provides high flexibility in terms of computational complexity, as the number of iterations can be adjusted in order to optimize the trade-off between the desired accuracy and the available computational time. A remarkable advantage in using $W(x)$ in exponential circuit models is that we can use the same lookup table for many different nonlinearities, minimizing the required storage resources.

A. Applications in the K Domain

The W function made its first appearance in circuit theory with the work of Banwell and Jayakumar [26], which derived a closed-form expression of the current flowing through a diode connected to a voltage source V_E and a series resistance R_E , as in Fig. 4(a). In the Shockley model the relationship between diode current I and voltage V is

$$I = I_s \left(e^{\frac{V}{\eta V_t}} - 1 \right) \quad (6)$$

where e is Napier's number, V_t is the thermal voltage, η is the ideality factor and I_s is the saturation current of the diode. The problem approached in [26] was finding a closed-form expression for the current I , which satisfies both the Shockley model (6) and the K law $V = V_E - R_E I$. The solution

$$I = \frac{\eta V_t}{R_E} W \left(\frac{I_s R_E}{\eta V_t} e^{\frac{V_E + R_E I_s}{\eta V_t}} \right) - I_s, \quad (7)$$

proposed in [26], is usually referred to as *Generalized Diode Equation* (GDE). This result was later extended by Banwell by considering V_E and R_E as a generic resistive Thévenin

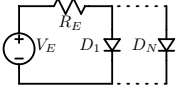


Fig. 1. Multi-exponential Junction Model.

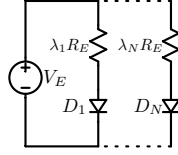


Fig. 2. Alternative Multi-exponential Junction Model.

equivalent [27]. He considered some BJT circuits, whose linear parts can be reduced to Thévenin equivalents, and found analytical solutions.

The study of circuits with diodes is quite common in the photovoltaic field, as the typical models for ideal solar cells involve a parallel bank of diodes, representing the silicon p–n junction, in parallel with a current source. In order to describe real solar cells, a series resistance and a parallel shunt resistance are often added to the model. This is, therefore, one case where the GDE can be put into use. The GDE was, in fact, applied to the solar cell model in [29] and an explicit solution for the current passing through a single exponential junction with a parasitic series and two parasitic parallel shunt resistances was found. Following these results, techniques for estimating solar cell parameters exploiting the W function [30]–[32] were developed. New analytical methods for extracting diode parameters [33], [34] were proposed shortly after.

Real semiconductor p–n junctions, are known to exhibit multiple simultaneous conduction mechanisms, usually described with multi-exponential models, characterized by a parallel bank of diodes with different ideality factors and saturation currents as shown in [35], [36]. In these works the junction model with N conduction mechanisms presented in Fig. 1 is approximated by the alternative model in Fig. 2. The global Thévenin resistance R_E is replaced by N individual series resistances $\lambda_n R_E$ being $1 \leq n \leq N$. λ_n are positive real parameters that must be tuned carefully in order to obtain the best approximation. The alternative model is equivalent to the original one only if all the diodes are identical and we set $\lambda_n = N$ for each branch. In the other cases, however, we can still obtain good approximations. Using the alternative model, an exact closed-form solution for the currents passing through the diodes can be found [35], [36]. The resistances $\lambda_n R_E$ allow us to compute the currents passing through each individual branch using the GDE (7). The individual currents can then be summed in order to find the explicit global solution

$$I = \sum_{n=1}^N \frac{\eta_n V_t}{\lambda_n R_E} W \left(\frac{I_{s_n} \lambda_n R_E}{\eta_n V_t} e^{\frac{V_E + \lambda_n R_E I_{s_n}}{\eta_n V_t}} \right) - I_{s_n} . \quad (8)$$

B. Applications in the WD Domain

Not much effort has been devoted to the development of applications of the W function in the WD domain. In [11] an explicit one-port WD version of the Shockley model (6) is obtained substituting (1) in (6) and using the W function:

$$b = a + 2R_0 I_s - 2nV_t W \left(\frac{R_0 I_s}{nV_t} e^{\frac{R_0 I_s + a}{nV_t}} \right) . \quad (9)$$

In addition, in [11] a one-port diode clipper model containing two identical anti-parallel diodes is presented, where only one of the two diodes is conducting at any time. This way the port current can be approximated with the forward current passing through the conducting diode, while ignoring the reverse leakage current of the other diode. The resulting wave mapping is

$$b = \text{sgn}(a) \left(|a| + 2R_0 I_s - 2nV_t W \left(\frac{R_0 I_s}{nV_t} e^{\frac{R_0 I_s + |a|}{nV_t}} \right) \right) , \quad (10)$$

where $\text{sgn}(a)$ is a function returning the sign of a and suggests which diode is conducting. In [37] an improvement of this model of the diode clipper is proposed. Both in [11] and in [37] the diodes characterizing the NLE are assumed to be equal (i.e., same ideality factor and saturation current). In this paper we will discuss the more general case where diodes are not necessarily identical.

III. EXPLICIT WD MODELS OF ONE-PORT NLES

In order to search for an explicit wave mapping that describes a one-port NLE containing exponentials, we can start from its description in the K domain and then repurpose it in the WD domain. One common way to do so is writing the K port variables directly as (1), but often this substitution leads to complicated systems to solve. One general procedure for determining explicit wave mappings in a straightforward fashion consists of three main steps. We first write the port current, or the port voltage, as

$$I = \frac{a - V}{R_0} , \quad V = a - R_0 I . \quad (11)$$

We then rearrange the system, searching an equation that fits the general form (3) presented in [25]. The unknown variable y can either be V or I , depending on how the substitution was performed. If we succeed in turning the system in the form (3), we obtain an explicit solution for y using (4). We can finally compute the reflected wave using

$$b = 2V - a \quad \text{or} \quad b = a - 2R_0 I . \quad (12)$$

When dealing with one-port NLEs we can often resort to exploiting what we refer to as the “K Domain Analogy” (KDA), which consists of replacing the circuit that the NLE connects to with its Thévenin equivalent, and deriving from this simplified representation the corresponding wave mapping. More specifically, if V_E is the voltage generator of the Thévenin equivalent and R_E its series resistance, as shown in Fig. 4, setting $V_E = a$ and $R_E = R_0$, the K equations describing the one-port element in series to the Thévenin equivalent become identical to (11). Therefore, if we already have K equations expressing I or V of a one-port NLE in series to a Thévenin equivalent, we could skip the first two steps of the procedure and derive the correspondent wave mapping, by simply setting $V_E = a$, $R_E = R_0$ and then using (12).

A. Derivation of the Diode Model using the KDA

Let us now apply the KDA to the same circuit that was analyzed in [26]. Starting from the GDE (7), we derive an

explicit equation, expressing the port voltage V as a function of the incident wave $a = V_E$ and the reference port resistance $R_0 = R_E$:

$$V = a - \eta V_t W \left(\frac{I_s R_0}{\eta V_t} e^{\frac{a + R_0 I_s}{\eta V_t}} \right) + R_0 I_s . \quad (13)$$

Finally, substituting (13) in (12), we obtain exactly the same result presented in [11] (eq. (9)) while skipping all the algebra needed in the second step of the procedure.

B. Parallel and Anti-Parallel Bank of Diodes Model

We apply the KDA to the multi-exponential model represented in Fig. 1, where the NLE is a parallel bank of N diodes. As discussed in [35] and [36] we cannot compute the global current I of the model in Fig. 1 with explicit equations, but we can do it using the alternative model in Fig. 2. So starting from equation (8), we easily derive the following wave mapping:

$$b = a - 2R_0 \sum_{n=1}^N \left[\frac{\eta_n V_t}{\lambda_n R_0} W \left(\frac{\lambda_n R_0 I_{s_n}}{\eta_n V_t} e^{\frac{a + \lambda_n R_0 I_{s_n}}{\eta_n V_t}} \right) - I_{s_n} \right] \quad (14)$$

where η_n and I_{s_n} are the ideality factor and the saturation current of the n th diode, R_0 is the reference port resistance and λ_n is its multiplicative factor relative to the n th branch. When $N = 1$ and $\lambda_1 = 1$, the scattering equation (14) coincides with (9). Notice that this result could not have been obtained by blindly applying the three-step-procedure described at the beginning of this Section, as any of the terms that play the role of y in eq. (3) are neither port currents nor port voltages. In this case, in fact, the “ y variables” are the currents passing through each diode branch, which all contribute to the global port current of the NLE. This, however, does not affect the generality of the three-step-procedure as its validity relies on the fact that R_0 is split into N series resistances $\lambda_n R_0$ to begin with. Both a parallel bank of diodes, such as the one in Fig. 1; and a parallel bank of diodes with a series resistance in each branch, such as the one in Fig. 2; can be described in the WD domain by the wave mapping (14).

Combining eq. (14) with eq. (10), we derive an even more general wave mapping describing an arbitrary number of different parallel and anti-parallel diodes:

$$b = a - 2R_0 \Theta_+(a) \sum_{n=1}^N \frac{\eta_n V_t}{\lambda_n R_0} W \left(\frac{\lambda_n R_0 I_{s_n}}{\eta_n V_t} e^{\frac{|a| + \lambda_n R_0 I_{s_n}}{\eta_n V_t}} \right) - I_{s_n} \\ - 2R_0 \Theta_-(a) \sum_{m=N+1}^{N+M} \frac{\eta_m V_t}{\lambda_m R_0} W \left(\frac{\lambda_m R_0 I_{s_m}}{\eta_m V_t} e^{\frac{|a| + \lambda_m R_0 I_{s_m}}{\eta_m V_t}} \right) - I_{s_m} \quad (15)$$

where $\Theta_+(a)$ and $\Theta_-(a)$ are two functions defined as

$$\Theta_+(a) = \begin{cases} 1 & \text{if } a \geq 0 \\ 0 & \text{if } a < 0 \end{cases} \quad \Theta_-(a) = \begin{cases} 0 & \text{if } a \geq 0 \\ -1 & \text{if } a < 0 \end{cases} .$$

The NLE described by eq. (15) is depicted in Fig. 3. If all diodes are identical, $\lambda_n = N$ and $\lambda_m = M$, (15) reduces to (10). In general, the wave mapping (15) should be used carefully in extreme cases in which $N \gg M$ or $M \ll N$, as the reverse bias saturation currents might be not negligible. By the way, (15) could be used for deriving a WD model of a solar cell with a multi-exponential junction [35], [36]. In Section V other possible applications of (15) are shown.

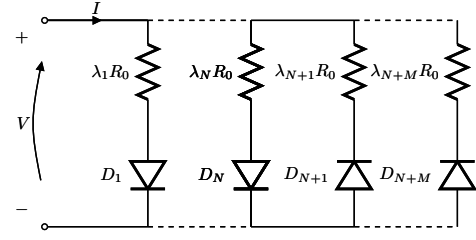


Fig. 3. One-Port NLE characterized by a Parallel Bank of $N + M$ Diodes with Opposite Polarities.

IV. EXPLICIT WD MODELS OF MULTI-PORT NLES

In this Section we focus on the modeling of multi-port NLEs. In particular, we present an extension to the multi-port case of the procedure proposed in Section III for deriving a new family of NLEs in the WD domain (using explicit wave mappings). We finally offer a definition of Simplified Models, which are approximations of circuits containing non-conducting diodes. These models can be useful to widen the class of circuits that can be implemented in the WD domain.

A. Sign Conventions for Port Variables in n -terminal NLEs

Each port of a generic NLE has two prongs, which share the same value of current (the current through one prong equals the current through the other one), called *port current*, which has a well-defined reference orientation. In this work we define the coupled *port voltage* variable according to the passive sign convention as shown in Fig. 3. In traditional one-port NLEs the port current enters the NLE and passes through it. When it comes to defining the ports of a multi-terminal NLE, the situation can easily become more complicated. Instead of defining waves with reference to the NLE, it will often be more practical to define them with reference to the load that is connected to the NLE, rather than with reference to the NLE itself. This results in a change of the reference orientation of the port current as it enters the load instead of the NLE. The change of the reference orientation of the port current implies a change of the roles of the incident and the reflected waves (a and b). For this reason we will need to flip the sign of the waves when defining the port current. This fact was already pointed out in [17]. In order to clarify this, let us first consider the simplest case of a circuit with a one-port NLE in Fig. 4(a) and the relative WD implementation in Fig. 4(b). This is a configuration where port variables can be defined with reference the NLE (port current entering the NLE). When port variables are defined this way, we will refer to the port as a *Port of the First Type* (PFT). The 3-terminal NLE in Fig. 5(a), on the other hand, cannot be easily described using PFTs. In this case it is more convenient to define port variables with reference to the loads that are connected to the NLE, i.e., to pick the reference port currents as entering such loads, as done in [17]. This means interpreting the port configuration as shown in Fig. 5(b). As we can see, two of such ports connect to each other through a prong (ground), which is not a terminal of the NLE. When a port current is defined as directed outward with respect to the NLE, as in the case of Fig. 5(a), we will

talk about a *Port of the Second Type* (PST). While the two prongs of a PFT are always, by definition, terminals of the NLE that we are modeling, in the case of a PST one of the two prongs might not be a terminal of the NLE. In this case it is often useful to choose ground as common external prong of many ports. We can deduce, therefore, that the number of ports N of a generic n -terminal NLE with $n > 2$ may vary according to the topology of the reference circuit in the range $1 \leq N \leq N_{max}$, where

$$N_{max}(n) = \frac{n(n+1)}{2} = \binom{n+1}{2}. \quad (16)$$

In the light of this in Section V we will present a novel model for a generic 3-terminal BJT with $N_{max}(3) = 6$ ports (31).

In order to accommodate PFTs and PSTs we will adopt the following notation for port voltages and port currents:

$$V = \frac{a+b}{2} \quad I = \delta_p \frac{a-b}{2R_0} \quad (17)$$

where $\delta_p = 1$ when in the case of a PFT and $\delta_p = -1$ in the case of a PST. In general, a NLE is modeled using either all PFTs or PSTs.

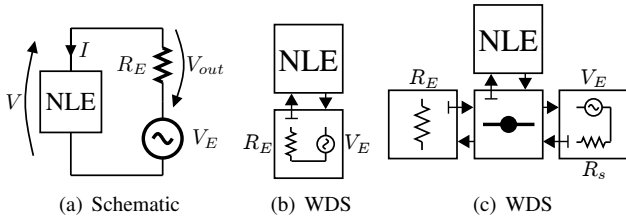


Fig. 4. One-port NLE modeled using one PFT. The WDS in 4(b) refers to Subsection IV-A. The WDS in 4(c) refers to Subsection V-A.

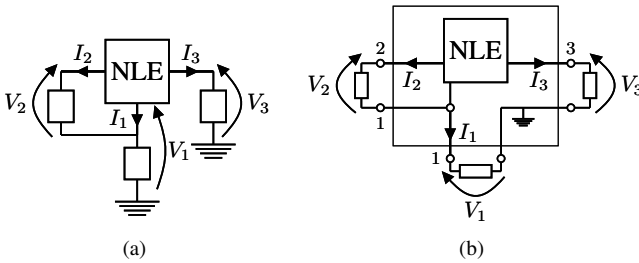


Fig. 5. 5(a) shows a 3-terminal NLE that cannot be easily modeled using 3 PFTs. In 5(b) we have the same NLE shown in 5(a) modeled using three PSTs; two of such ports have a common external prong (ground), which is not one of the 3 terminals of the NLE.

B. WD Multi-port NLEs Derivation

In this Subsection we will describe how to derive WD exponential and explicit multi-port models. We will begin with the simplest case of a NLE made of only one subcircuit and then we will address the general case of a NLE made of K subcircuits that can be independently analyzed. For instance, the circuit in Fig. 7 has a NLE containing $K = 2$ independently analyzable subcircuits, which are the two separated diodes.

Let us first consider the simplest case of a single subcircuit and assume that the whole NLE be connected to the rest of the

circuit through N ports, which in this Subsection are indicated with integers $1, 2, \dots, N$. Let us derive a system of equations describing the subcircuit in the K domain. We then express the Kirchhoff variables of the generic port x with $1 \leq x \leq N$, using one of the two formulas:

$$I_x = \delta_{p_x} \frac{a_x - V_x}{R_{0x}}, \quad V_x = a_x - \delta_{p_x} R_{0x} I_x. \quad (18)$$

We refer to the unknown variable as y , which is either a port voltage or a port current. In order to find explicit wave mappings we need to express each port variable as a linear function of y . If the unknown variable is a port voltage, e.g. $y = V_1$, then each port voltage V_x must satisfy the equation

$$V_x = \tau_x V_1 + \rho_x, \quad (19)$$

where τ_x and ρ_x are scalar functions of the incident waves and the reference port resistances, i.e. they can be written as $\tau_x(a_1, \dots, a_N, R_{01}, \dots, R_{0N})$ and $\rho_x(a_1, \dots, a_N, R_{01}, \dots, R_{0N})$. Similarly, if the unknown variable is a port current, e.g. $y = I_1$, then each port current I_x must satisfy the equation

$$I_x = \zeta_x I_1 + \nu_x, \quad (20)$$

where, again, ζ_x and ν_x are scalar functions, which can be written as $\zeta_x(a_1, \dots, a_N, R_{01}, \dots, R_{0N})$ and $\nu_x(a_1, \dots, a_N, R_{01}, \dots, R_{0N})$.

By defining $\mathbf{V} = [V_1, \dots, V_N]^T$, $\boldsymbol{\tau} = [1, \tau_1, \dots, \tau_N]^T$, $\boldsymbol{\rho} = [0, \rho_1, \dots, \rho_N]^T$, $\mathbf{y} = [V_1, 1]^T$, we obtain a matrix formulation of the mutual relations between port voltages:

$$\mathbf{V} = [\boldsymbol{\tau} \ \boldsymbol{\rho}] \mathbf{y}. \quad (21)$$

Similarly, by defining $\mathbf{I} = [I_1, \dots, I_N]^T$, $\boldsymbol{\zeta} = [1, \zeta_1, \dots, \zeta_N]^T$, $\boldsymbol{\nu} = [0, \nu_1, \dots, \nu_N]^T$, $\mathbf{y} = [I_1, 1]^T$, we obtain:

$$\mathbf{I} = [\boldsymbol{\zeta} \ \boldsymbol{\nu}] \mathbf{y}. \quad (22)$$

Then, starting from the derived mutual relations between port variables, we search an equation fitting the form (3), analogously to what done in the one-port case III. This will allow us to obtain an explicit solution for y in the form (4). Let us define the vector of the incident waves as $\mathbf{a} = [a_1, \dots, a_N]^T$; the vector of the reflected waves as $\mathbf{b} = [b_1, \dots, b_N]^T$; and the diagonal matrix of reference port resistances $\mathbf{R}_0 = \text{diag}(R_{01}, \dots, R_{0N})$. Writing \mathbf{b} as a function of \mathbf{V} or \mathbf{I} we obtain, respectively,

$$\mathbf{b} = 2\mathbf{V} - \mathbf{a} \quad \text{and} \quad \mathbf{b} = \mathbf{a} - \delta_p 2\mathbf{R}_0 \mathbf{I}. \quad (23)$$

Let us now consider the more general case in which the NLE is constituted of K independently analyzable subcircuits as, for instance, the NLE in Fig. 7 where $K = 2$. In this case the derivation described before would be applied separately for each subcircuit. Let us assume that each subcircuit has N_k ports, so that the total number of ports of the NLE is $\sum_{k=1}^K N_k$. In general, we will end up with N explicit scattering vector functions in one of the two forms (23).

C. Simplified Models of NLEs with diodes

Simplified Models (SMs) approximate the behavior of NLEs eliminating diodes which are “not conducting” (i.e., which ones are currently not operating in the first quadrant of their IV characteristics). Such models are based on what we know about the mutual relations between terminal potentials. Thanks to this simplification we can transform many NLEs that could not be modeled with explicit wave mappings into something that now belongs to the family of NLEs described in Subsection IV-B. In order for this approach to be effective, we might need to approximate the target NLE with different SMs, which take turn depending on how the mutual relations between the potentials of the terminals change. An example

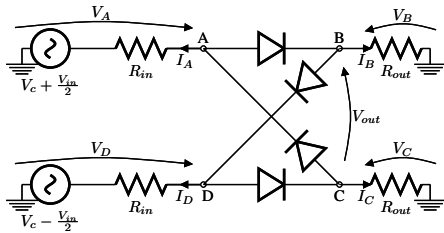


Fig. 6. Parker's Model of a Transformer-less Ring Modulator. The output voltage is $V_{out} = V_B - V_C$.

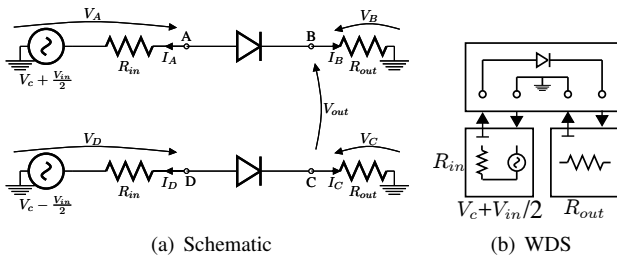


Fig. 7. Ring Modulator SM for $V_c > 0$. The WDS in Fig. 7(b) refers only to the subcircuit with the generator $V_c + V_{in}/2$. The complementary WDS referring to the subcircuit with $V_c - V_{in}/2$ is similar.

of use of SMs is the transformerless ring modulator model of Fig. 6 [38]. In a traditional ring modulator, if we denote the modulator waveform by V_{in} and the carrier waveform by V_c , the voltage at the two input nodes is given by $V_c + V_{in}/2$ and $V_c - V_{in}/2$. The circuit of Fig. 6 can be approximated using two different SMs. The first model (Fig. 7) describes the ring modulator when $V_c > 0$, in which case we remove the non-conducting diodes D_{CA} and D_{BD} . Similarly, when $V_c < 0$, we remove D_{AB} and D_{DC} . This, indeed, is an approximation because the actual voltages applied to the diodes are also affected by the contribution of both $V_{in}/2$ and the resistive voltage loss on R_{in} . However, in this particular example, we can assume $V_{in} \ll V_c$, therefore this approximation is expected not to significantly affect the circuit behavior.

While identifying SMs is readily done through visual circuit inspection, the selection of which SM is active during the WD simulation might not be as straightforward. The problem, in fact, is to select which SM is active at any time using just the values of incident waves \mathbf{a} . The state of activation of a diode depends on the sign of the voltage at its terminals,

which must be derived from the port voltages \mathbf{V} , which, in turn, must be derived from \mathbf{a} . As \mathbf{V} generally depends on \mathbf{a} and \mathbf{b} , this might prove tricky. However, in some cases, the information we need on \mathbf{V} can be derived from properties of \mathbf{a} only, e.g. $\text{sgn}(\mathbf{a})$. Examples are the ring modulator WD model in Section V-C and the one-ports characterized by the wave mappings 10 and 15. A similar discussion about one-port NLEs is also given in [37] where a diode-clipper is analyzed. Here we extend that discussion to the multi-port case.

In general, the K-WD map for a generic N -port element can be written in matrix form as

$$\begin{bmatrix} \mathbf{a} \\ \mathbf{b} \end{bmatrix} = \mathbf{T} \begin{bmatrix} \mathbf{V} \\ \mathbf{I} \end{bmatrix} \quad \text{with } \mathbf{T} = \begin{bmatrix} \mathbf{E}_N & \mathbf{R}_0 \\ \mathbf{E}_N & -\mathbf{R}_0 \end{bmatrix}, \quad (24)$$

where \mathbf{E}_N is the $(N \times N)$ identity matrix. The K-WD transformation 24, characterized by matrix \mathbf{T} is, in fact, independent of the internal complexity of the multi-port element, as it is performed in a port-wise fashion. Therefore, considering the IV characteristics at each port, we can use (24) to check if the mutual relations between elements of the vector \mathbf{V} are mapped onto corresponding mutual relations between elements of the vector \mathbf{a} . Similarly to what we did in [37] for the one-port case, we provide a geometric interpretation of the K-WD transformation, which can be useful to relate \mathbf{a} to the needed information on \mathbf{V} . If we apply the QR decomposition on \mathbf{T} we obtain $\mathbf{T} = \mathbf{Q}\mathbf{R}$, where the two $(2N \times 2N)$ matrices \mathbf{Q} and \mathbf{R} are generally of the form

$$\mathbf{Q} = \begin{bmatrix} \frac{1}{\sqrt{2}} \mathbf{E}_N & \frac{-1}{\sqrt{2}} \mathbf{E}_N \\ \frac{1}{\sqrt{2}} \mathbf{E}_N & \frac{1}{\sqrt{2}} \mathbf{E}_N \end{bmatrix} \quad \mathbf{R} = \begin{bmatrix} \sqrt{2} \mathbf{E}_N & \mathbf{O}_N \\ \mathbf{O}_N & -\sqrt{2} \mathbf{R}_0 \end{bmatrix} \quad (25)$$

where \mathbf{O}_N is an $(N \times N)$ matrix of zeros, therefore \mathbf{R} is diagonal (as \mathbf{R}_0 is diagonal as well). Through (25) we can interpret the K-WD transformation as a non-uniform scaling of the N characteristics (through the matrix \mathbf{R}) followed by a rotation of $-\pi/4$ (through the matrix \mathbf{Q}), which is independent of the port resistance values. If a priori techniques are not sufficient for inferring which diodes are conducting, on line methods should be developed, based on the past simulation parameters. However the formalization of general methods for deriving such information is beyond the scope of this work and deserves future research.

V. EXAMPLES OF APPLICATIONS

In this Section we propose some implementations of typical circuits containing diodes or BJTs. The first two examples are possible applications of the new one-port NLEs presented in III-B. The other examples show different multi-port NLEs belonging to the new family of NLEs described in IV-B, where Simplified Models (SMs) are exploited. In particular, we discuss the case of a transformerless ring modulator and some BJT amplifier configurations, which take advantage of a new 6-port general model of the BJT. This is a model that is suitable for dealing with feedback between the BJT terminals. In each simulation we evaluate $W(x)$ using the MATLAB function `lambertw` and we use a sample rate of 96 kHz.

A. Half-Wave Rectifier with N Different Parallel Diodes

We employ the NLE depicted in Fig. 2 and characterized by the wave mapping (14) for designing a parametric Half-Wave Rectifier (HWR) with a bank of different parallel diodes. The simple reference circuit, consisting of a real sinusoidal voltage generator $V_E(t) = g_E(\sin(2\pi f_{0E} t))$ in series with a resistance $R_E = 8\Omega$ and the one-port NLE, is shown in Fig. 4(a). The NLE is modeled using one PFT. In this Subsection we assume the real voltage generator V_E has an internal series resistance R_s . The WD implementation is drawn in Fig. 4(c). In order to accurately model the NLE, we need to properly select the λ_n parameters in (14). The simplest situation is when the N diodes are identical. In this case, as already mentioned in Subsection III-B, we should set $\lambda_n = N$. In more complex scenarios the N parallel diodes have different parameter values. As an example, we set $N = 2$, $R_s = 3\Omega$, $R_E = 1\Omega$, $g_E = 10\text{ V}$, $f_{0E} = 80\text{ Hz}$, $I_{s1} = I_{s2} = 10^{-12}\text{ A}$ and different ideality factors; $\eta_1 = 0.5$ and $\eta_2 = 1$. Experimentally we found that, setting $\lambda_1 = \lambda_2 = 1.892$, the WD model grasps the circuit behavior. Fig. 8 shows the comparison between the WD and SPICE output voltage signals.

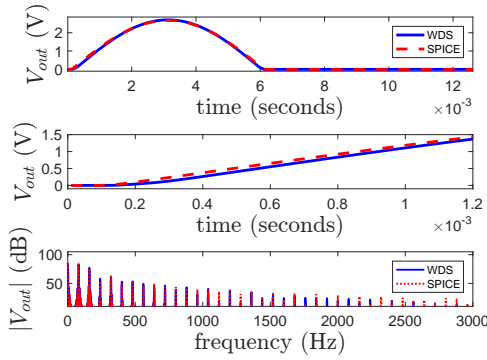


Fig. 8. HWR output voltage (WDS vs SPICE). The upper subplot shows the profile of V_{out} in the time domain. The subplot in the middle shows a zooming of the same curve near the zero-axis, where the nonlinear behavior is more pronounced. The last subplot represents V_{out} in the frequency domain.

B. Electrical Damper

We can use (15) to implement an electrical damper with different attack and release time constants. The reference

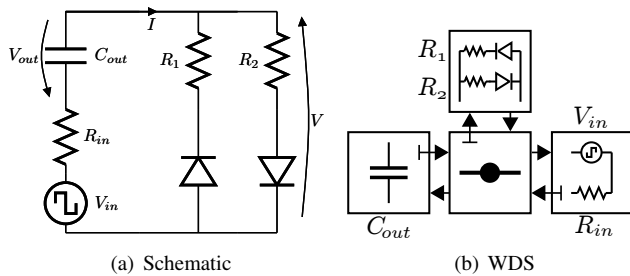


Fig. 9. Asymmetric Electrical Damper.

circuit and the relative WDS are represented in Fig. 9. A WD implementation of the electrical damper, realized with a

different approach, was already presented in [10]. In our implementation diodes and their series resistances are embedded in the NLE. The NLE is modeled using one PFT. The output voltage is detected across the capacitor C_{in} in series to the NLE. The square wave of the input voltage generator is defined as $V_{in}(t) = V_{bias} + g_{in}(\text{sgn}(\sin(2\pi f_{0in} t)))$. The coefficients λ_N and λ_M , which multiply the reference port resistance of the NLE, are tuned in order to match as accurately as possible the resistances R_1 and R_2 , which in our reference circuit are 4Ω and 1Ω , respectively. The circuit parameters and the corresponding actual values of the WD simulation are: $g_{in} = 5\text{ V}$, $f_{0in} = 80\text{ Hz}$, $C_{in} = 1.8 \cdot 10^{-4}\text{ F}$, $\eta_N = 1$, $\eta_M = 1$, $V_{bias} = -6\text{ V}$, $\lambda_{n1} = 3.3$, $\lambda_{m1} = 1.44$, $V_t = 25 \cdot 10^{-3}\text{ V}$, $I_{sN} = 10^{-12}\text{ A}$ and $I_{sM} = 10^{-12}\text{ A}$. Fig. 10 shows the output voltage profile; the good behavior of the WDS is verified comparing it to a SPICE simulation.

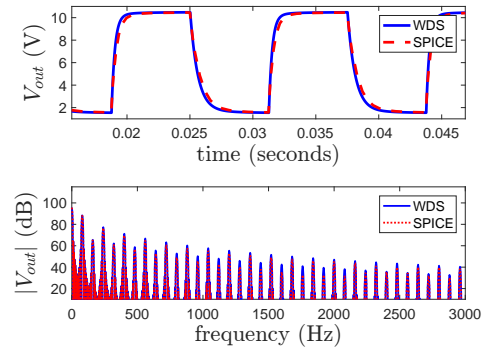


Fig. 10. Asymmetric Electrical Damper output voltage in the time domain and in the frequency domain (WDS vs. SPICE).

C. Ring Modulator

In this Subsection we present an implementation of the ring modulator characterized by higher accuracy w.r.t. the existing solutions in the literature on WDFs [18]. We model the NLE using 4 PSTs, named A , B , C and D . The port voltages are the four terminal potentials: V_A , V_B , V_C and V_D . We use two SMs; one for $V_c > 0$ and one for $V_c < 0$. Hereafter we analyze in detail the subcircuit of the first SM (Fig. 7) containing diode D_{AB} . The subcircuit is described by the system of equations:

$$\begin{cases} I_B = I_s(e^{\frac{V_{AB}}{\eta V_t}} - 1) \\ I_A = -I_B \end{cases} \quad (26)$$

Let us choose $I_B = y$ as independent port variable; therefore, according to (20), we can express the port current I_A as a linear function of I_B by writing $I_A = -I_B$. So in this example the parameters of equation (20) are simply $\zeta_B = -1$ and $\nu_B = 0$. Writing port voltages as functions of incident waves, port currents and port resistances, according to (18), we obtain:

$$I_B = I_s \left(e^{\frac{a_A - a_B - I_B(R_{0A} + R_{0B})}{\eta V_t}} - 1 \right) \quad (27)$$

Eq. (27) is attributable to the form (3), setting

$$\begin{aligned} y &= I_B & \theta &= -(R_{0A} + R_{0B}) / (\eta V_t) & p &= e \\ \beta &= (a_A - a_B) / (\eta V_t) & c &= 1/I_s & d &= 1 \end{aligned} \quad (28)$$

Then through (4) we derive an explicit expression for I_B . The wave mappings for ports A and B are found using (23)

$$b_B = a_B + 2R_{0B}I_B \quad , \quad b_A = a_A + 2R_{0A}I_A \quad . \quad (29)$$

The wave mappings for ports C and D are derived likewise. The equations characterizing the complementary SM are similar to those already shown. The choice of the most suitable SM at each iteration step is performed according to the considerations explained in Section IV-C. When V_c approaches to 0 the signs of a_A and a_D may not agree. In this case the sign of one incident wave is chosen, e.g. a_A , and a small error is introduced. The smaller the magnitude of V_{in} w.r.t. the amplitude of V_c , the smaller the error. In our simulation we chose the circuit parameters in such a way to obtain comparable results to [38]: $g_{in} = 1$ V, $f_{0in} = 500$ Hz, $R_{in} = 80 \Omega$, $g_c = 1$ V, $f_{0c} = 1500$ Hz, $R_{out} = 10^6 \Omega$, $\eta = 2.19$, $I_s = 10^{-12}$ A and $V_t = 26 \cdot 10^{-3}$ V. Notice that $V_{in}(t) = g_{in}(\sin(2\pi f_{0in} t))$ and $V_c(t) = g_c(\sin(2\pi f_{0c} t))$, therefore with this choice of parameters the condition of having $V_{in} \ll V_c$ is not satisfied. Nonetheless, even in these conditions, the WD model shows a good agreement with a SPICE simulation, as shown in Fig. 11. The mismatch is concentrated near zero crossings where the switching between SMs takes place. In addition SMs ignore the reverse-bias currents, which are not negligible near the zero-axis.

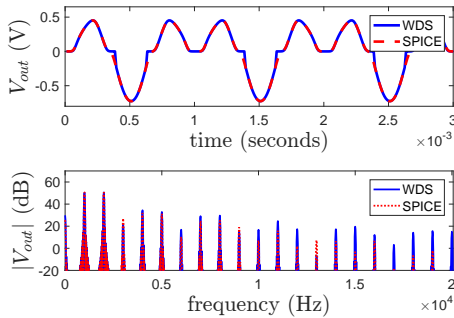


Fig. 11. Ring Modulator output voltage in the time domain and in the frequency domain (WDS vs. SPICE).

D. Bipolar Junction Transistor Amplifiers

For modeling an n-p-n BJT we refer to the large signal Ebers–Moll model (EMM) [39] of Fig. 12. We choose the reference direction of currents I_C , I_E and I_B , referring to Collector, Emitter and Base terminals respectively, as outgoing

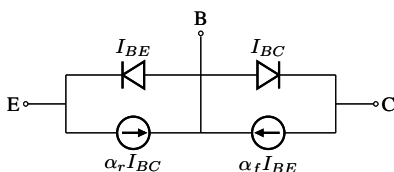


Fig. 12. Ebers Moll Model.

(e.g. see Fig. 13(a)), so that the EMM is described by the system of equations:

$$\begin{cases} I_E = I_{BE} - \alpha_r I_{BC} \\ I_C = I_{BC} - \alpha_f I_{BE} \\ I_E + I_B + I_C = 0 \end{cases} \quad , \quad (30)$$

where

$$I_{BE} = I_{Es} \left(e^{\frac{V_{BE}}{\eta V_t}} - 1 \right) \quad , \quad I_{BC} = I_{Cs} \left(e^{\frac{V_{BC}}{\eta V_t}} - 1 \right) \quad ,$$

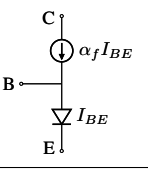
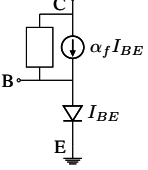
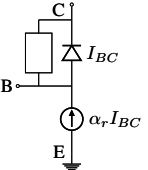
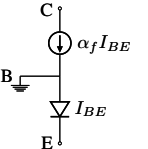
being I_{Es} and I_{Cs} the saturation currents of the two diodes described by the Shockley model (6). The BJT can be characterized by different numbers of PSTs, depending on the topology of the reference circuit. The presence of feedback can increase the number of ports up to 6 (16): 3 port voltages being potentials at terminals (V_C , V_B and V_E) and 3 port voltages being differences of potentials between terminals ($V_{CE} = V_C - V_E$, $V_{CB} = V_C - V_B$ and $V_{EB} = V_E - V_B$). Adding feedback currents to the classical EMM, we obtain an *Extended Ebers–Moll model (EEMM)* of the BJT with 6 PSTs (named E , B , C , CE , CB and EB):

$$\begin{cases} I_E = I_{BE} - \alpha_r I_{BC} + I_{CE} - I_{EB} \\ I_C = I_{BC} - \alpha_f I_{BE} - I_{CE} - I_{CB} \\ I_E + I_B + I_C = 0 \end{cases} \quad , \quad (31)$$

where I_{CE} , I_{EB} and I_{CB} are the port currents passing through the loads of the three feedback ports. We can employ SMs to approximate the EMM and the EEMM. If the Collector–Base junction is reverse-biased the corresponding diode is removed. The same is done if the Emitter–Base junction is reverse-biased. It can be verified that a parametrization leading to an explicit model based on the W function can be found only for SMs of the EEMM with up to 3 ports. Such 3 ports can be either the 3 terminal-ground ports E , C and B , as in Fig. 13, or 2 of them and a feedback port having the 2 “active” terminals as prongs, as in Fig. 15. We notice that if one of the 3 potentials at terminals is zero, we end up with a degenerate case, since the remaining 2 terminal-ground ports and the 2 corresponding feedback ports have their respective pairs of prongs in common, as in Fig. 17. In Table I we show the parameterizations that can be used for finding explicit wave mappings of some SMs of the EEMM in relevant BJT amplifier configurations. In each row of Table I is specified which port variable is chosen as dependent variable y and also the expression of the other parameters in eq. 3.

1) *Common Collector BJT Amplifier*: A 3-port NLE is used for implementing the BJT in the amplifier of Fig. 13. The first SM of Table I is employed together with a “specular” SM describing the BJT when the Emitter–Base junction is reverse-biased. V_{bias} is set to 0 V in order to test the amplifier in cutoff mode. The other parameter values of the simulation are $g_{in} = 1.5$ V, $f_{0in} = 200$ Hz, $R_{in} = 1 \Omega$, $V_g = 15$ V, $R_g = 2 \Omega$, $R_{out} = 5000 \Omega$, $V_t = 25 \cdot 10^{-3}$ V, $\eta = 1$, $I_{Es} = I_{Cs} = 45 \cdot 10^{-14}$ A, $\alpha_f = 0.9$ and $\alpha_r = 0.8$. Fig. 14 shows the voltage across R_{out} , comparing the WD model output with a SPICE simulation. We notice that the contribute of the reversed biased Collector–Base junction is not completely negligible and this fact results in a smaller amplitude of the output voltage in SPICE.

TABLE I
 BJT SIMPLIFIED MODELS IN COMMON AMPLIFIER CONFIGURATIONS

Simplified Model	Linear Dependences among Port Voltages or Port Currents and General Form Parametrization
BJT with a reverse biased Collector–Base junction in a Common Collector (or Emitter Follower) amplifier configuration implemented as a 3-port NLE.	 $y = I_E = I_{BE} \quad I_B = (\alpha_f - 1)y \quad I_C = -\alpha_f y$ $\theta = \frac{R_{0B}(\alpha_f - 1) - R_{0E}}{\eta V_t} \quad \beta = \frac{a_B}{\eta V_t} - \frac{a_E}{\eta V_t} \quad c = \frac{1}{I_{Es}} \quad d = 1 \quad p = e$ $b_E = a_E + 2R_{0E}I_E \quad b_B = a_B + 2R_{0B}I_B \quad b_C = a_C + 2R_{0C}I_C$
BJT with a reverse biased Collector–Base junction in a Common Emitter amplifier with feedback configuration implemented as a 3-port NLE.	 $y = V_B \quad V_C = \frac{y \left(\frac{\alpha_f}{R_{0B}} + \frac{1}{R_{0CB}} \right) + a_C \left(\frac{1 - \alpha_f}{R_{0C}} \right) - \frac{a_B \alpha_f}{R_{0B}} + \frac{a_{CB}}{R_{0CB}}}{(1 - \alpha_f)/R_{0C} + 1/R_{0CB}} \quad V_{CB} = V_C - y$ $\theta = \frac{1}{\eta V_t} \quad \beta = 0 \quad p = e \quad c = \frac{-1}{I_{Es}} \left(\frac{1}{R_{0B}} + \frac{\alpha_f/R_{0B} + 1/R_{0CB}}{1 - \alpha_f + R_{0C}/R_{0CB}} \right)$ $d = \frac{1}{I_{Es}} \left(\frac{a_B}{R_{0B}} \left(\frac{\alpha_f}{1 - \alpha_f + R_{0C}/R_{0CB}} + 1 \right) + \frac{a_C}{R_{0C}} \left(\frac{\alpha_f - 1}{1 - \alpha_f + R_{0C}/R_{0CB} + 1} \right) - \frac{a_{CB}/R_{0CB}}{1 - \alpha_f + R_{0C}/R_{0CB}} \right) + 1$ $b_B = 2V_B - a_B \quad b_C = 2V_C - a_C \quad b_{CB} = 2V_{CB} - a_{CB}$
BJT with a reverse biased Emitter–Base junction in a Common Emitter amplifier with feedback configuration implemented as a 3-port NLE.	 $y = V_B \quad V_C = \frac{y \left(\frac{1}{\alpha_r R_{0B}} + \frac{1}{R_{0CB}} \right) + a_C \left(\frac{1 - 1/\alpha_r}{R_{0C}} \right) - \frac{a_B}{\alpha_r R_{0B}} + \frac{a_{CB}}{R_{0CB}}}{(1 - 1/\alpha_r)/R_{0C} + 1/R_{0CB}} \quad V_{CB} = V_C - y$ $\theta = \frac{1}{\eta V_t} \left(1 - \frac{1/(\alpha_r R_{0B}) + 1/R_{0CB}}{(1 - 1/\alpha_r)/R_{0C} + 1/R_{0CB}} \right) \quad p = e$ $\beta = \frac{1}{\eta V_t} \left(\frac{a_C(1/\alpha_r - 1)}{1 - 1/\alpha_r + R_{0C}/R_{0CB}} + \frac{a_B}{\alpha_r} - \frac{a_{CB}}{R_{0CB}} \right) \quad c = \frac{1}{\alpha_r I_{Cs}} \left(\frac{1}{R_{0B}} + \frac{1/(\alpha_r R_{0B}) + 1/R_{0CB}}{1 - 1/\alpha_r + R_{0C}/R_{0CB}} \right)$ $d = \frac{1}{\alpha_r I_{Cs}} \left(\frac{-a_B}{R_{0B}} \left(\frac{\alpha_r - 1 + \alpha_r R_{0C}/R_{0CB}}{\alpha_r - 1 + \alpha_r R_{0C}/R_{0CB}} + 1 \right) + \frac{a_C}{R_{0C}} \left(\frac{1 - 1/\alpha_r}{1 - 1/\alpha_r + R_{0C}/R_{0CB}} - 1 \right) + \frac{a_{CB}}{R_{0CB}} \frac{1}{1 - 1/\alpha_r + R_{0C}/R_{0CB}} \right) + 1$ $b_B = 2V_B - a_B \quad b_C = 2V_C - a_C \quad b_{CB} = 2V_{CB} - a_{CB}$
BJT with a reverse biased Emitter–Base junction in a Common Base amplifier configuration implemented as a 2-port NLE.	 $y = I_E = I_{BE} \quad I_C = -y \alpha_f \quad V_B = 0$ $\theta = -R_{0E}/(\eta V_t) \quad \beta = -a_E/(\eta V_t) \quad c = 1/I_{Es} \quad d = 1 \quad p = e$ $b_E = a_E + 2R_{0E}I_E \quad b_C = a_C + 2R_{0C}I_C$

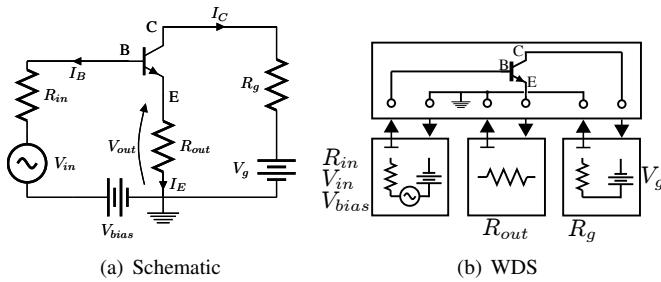


Fig. 13. BJT Common Collector Amplifier.

2) *Common Emitter BJT Amplifier with Base–Collector Feedback*: A 3-port NLE employing both the second and the third SM of Table I is used for implementing the BJT in the amplifier of Fig. 15. The simulation parameters are: $g_{in} = 1.5$ V, $f_{0in} = 200$ Hz, $R_{in} = 1000 \Omega$, $V_{bias} = 2.3$ V, $V_g = 15$ V, $R_g = 1 \Omega$, $R_{fBC} = 400 \Omega$ and $R_{out} = 8 \Omega$. The missing values are the same of V-D1. Fig. 16 shows the output current through R_{out} . Also in this case the contribute of the reversed

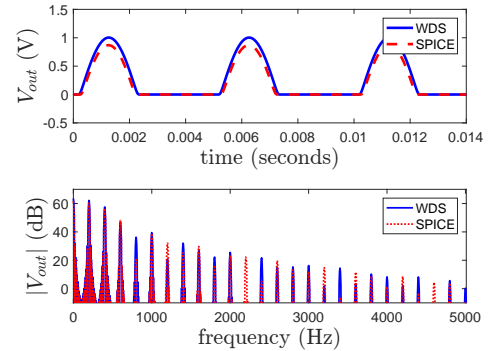


Fig. 14. BJT Common Collector Amplifier output voltage in the time domain and in the frequency domain (WDS vs. SPICE).

biased Collector–Base junction is not negligible and it results in a larger amplitude of the output current in SPICE.

3) *Common Base BJT Amplifier*: A 2-port NLE employing the fourth SM of Table I is used for implementing the amplifier

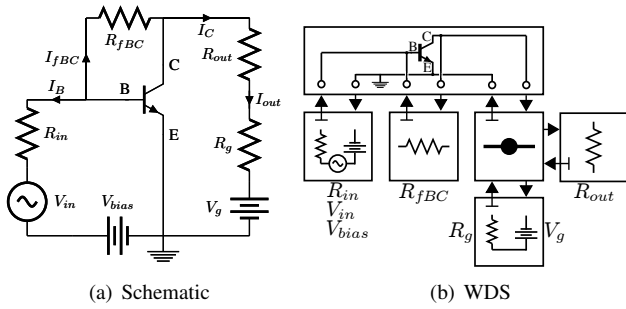


Fig. 15. BJT Common Emitter Amplifier with base-collector feedback.

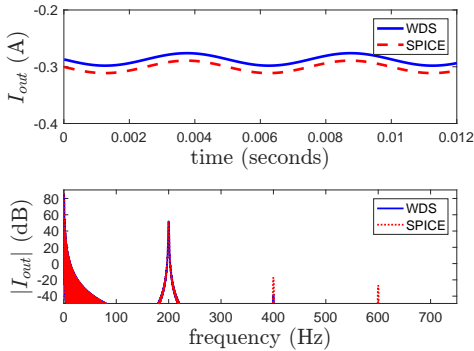


Fig. 16. BJT Common Emitter Amplifier output current in the time domain and in the frequency domain (WDS vs. SPICE).

of Fig. 17. The simulation parameters are: $g_{in} = 5 \text{ V}$,

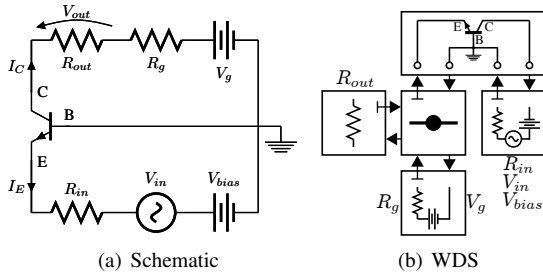


Fig. 17. BJT Common Base Amplifier.

$f_{0in} = 200 \text{ Hz}$, $R_{in} = 15 \Omega$, $V_{bias} = -12.5 \text{ V}$, $V_g = 90 \text{ V}$, $R_g = 15 \Omega$ and $R_{out} = 85 \Omega$. The missing values are the same of V-D1. Fig. 18 shows the voltage across R_{out} . In this case the mismatch w.r.t. to SPICE is smaller, since in the Common-Base configuration, the contribute of the reverse biased Emitter-Base junction has a low impact on V_{out} .

VI. CONCLUSIONS AND FUTURE WORK

In this work we explored the use of the Lambert W function in the WD domain for explicitly modeling exponential NLEs. We derived a new one-port wave mapping describing an arbitrary number of different parallel and antiparallel diodes. We also defined a new family of explicit WD models of multi-port NLEs. We tested our models in a number of applications, including a transformerless ring modulator. We also introduced the novel 6-port EEMM model of the BJT, which allows us to describe the BJT in all the amplifier configurations that

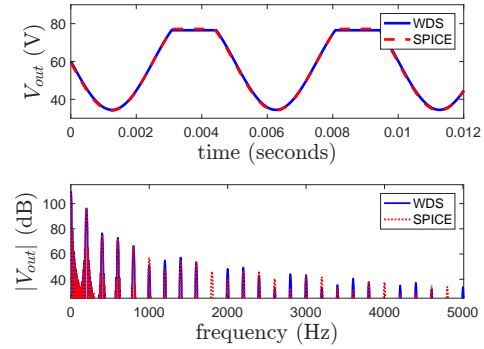


Fig. 18. BJT Common Base Amplifier output voltage in the time domain and in the frequency domain (WDS vs. SPICE).

include feedback. Comparing our results to SPICE outputs we found second order mismatches, as we are forced to trade some accuracy for the possibility of finding a closed-form solution. Although perfect waveform reconstruction is not always required in virtual analog modeling, we need to be careful about unwanted artifacts, as they could be perceivable. As far as future developments are concerned, we are planning to widen the family of WD multi-port NLEs in such a way to include exponential NLEs with memory.

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