Joule Heating in SiO_x RRAM Device Studied by an Integrated Micro-Thermal Stage

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***Abstract*—In this paper we propose a new method of estimating Joule heating in a resistive switching SiO_x based device through the use of a micro-thermal stage (MTS). We show an electro-thermal characterization of the device during set/reset operation using the MTS structure as a thermometer, we then attempt to reconstruct the complete heating profile of the device through numerical modeling in COMSOL, then we simulate the reset condition of the device.**

I. Introduction

Resistive switching memory (RRAM) is emerging as a high speed, low fabrication cost, low power technology for embedded memory [1] [2] and neuromorphic computing [3] [4] [5]. Embedded RRAM has shown a significant reduction of energy for programming operation compared with Flash technology [6], thus supporting RRAM for storage, memory and in-memory computing [7]. Toward this goal, however, the switching variability [8] and noise [9] still represent a strong concern for the development of multilevel RRAM, which is essential for the implementation of deep learning accelerators [3] [4] and spatiotemporal recognition [10]. To improve the conductance control in RRAM, a better understanding of the switching mechanism is needed.

The switching mechanism in RRAM has been studied by several experimental techniques, including time-resolved experiments [11], in-situ and ex-situ TEM studies [12] [13], and temperature-dependent analysis [14]. The latter indicates that the set/reset switching voltage decreases at increasing temperature, thus suggesting that Joule heating plays a leading role in the switching process [15]. A powerful tool to investigate the role of Joule heating is the micro-thermal stage (MTS), consisting of an integrated resistive heater, typically a metallic line, located close to the device. MTS experiments have been conducted to study the crystallization process in phase change memory (PCM), allowing to extend the time-dependent crystallization to the μs scale [16] [17].

Temperature dependent characterization of RRAM with MTS have been reported [18], however in this work we use the MTS to probe the local temperature increase close to the device, showing that Joule heating is uniquely controlled by the dissipate power $P = VI$. By a combination of experimental data and numerical electro-thermal model of the RRAM structure, we evaluate the local temperature within the RRAM filament, representing the active spot in the device. We show that the reset condition can be viewed as a constant temperature at the filament location, thus supporting Joule heating as a critical ingredient accelerating resistive switching in RRAM.

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II. Experiments

The RRAM device consists of a $Ti/SiO_x/C$ stack fabricated in BEOL on a silicon substrate (Fig. 1a) where SiO_x (x around 1) is the active switching material deposited with thickness t_{ox} = 5 nm between a 20 nm thick graphitic C bottom electrode and a 50 nm thick Ti top electrode. The C bottom electrode was 70 nm wide, and contacted with a W plug underneath [19]. The device was first electroformed with a positive voltage of 6 V applied to the top electrode, then set and reset processes were conducted on the device at positive and negative voltages, respectively [20]. The test vehicle was a one-transistor/one-resistor (1T1R) structure fabricated on the front end of the device, where the current was controlled by the select transistor during the electrical characterization (Fig. 1b) (1T1R structure). The current-voltage (I-V) curves were characterized by applying a voltage ramp with increasing values of the compliance current I_C.

The thermal characterization was performed with a micro thermal-stage (MTS) structure (Fig. 1c) consisting of a tungsten wire located in the vicinity of the device (Fig. 1d). The 4 terminals of the W line allow to accurately measure

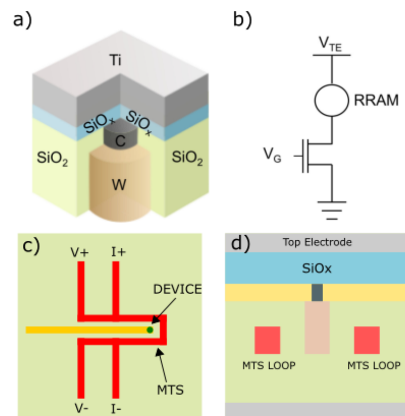

Fig. 1. Structure of the device (a) and experimental setup (b). Top view of the MTS (c) and section (d)

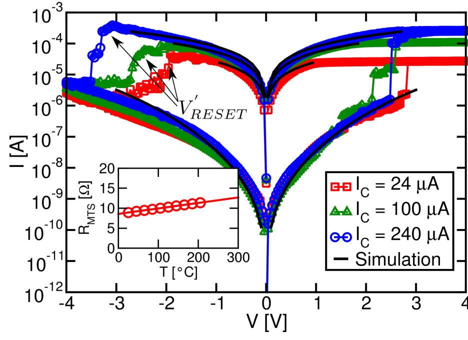

Fig. 2. Experimental IV characteristic of the device for different compliance currents. In the inset calibration curve of the MTS.

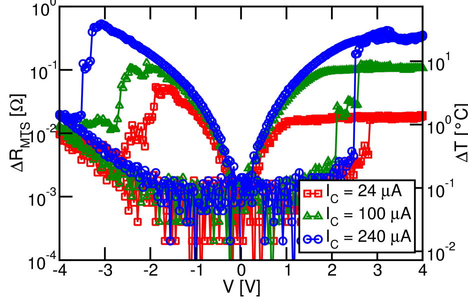

Fig. 3. Experimental resistance variation of the MTS during device operation and corresponding temperature calculated through calibration data.

the resistance hence the temperature enhancement in the line selectively close to the device. Although the MTS was used somewhere else to induce heating within the device [16] [17], here the MTS was used as a thermal probe only, to study the Joule heating during set and reset processes. Fig. 2 shows the measured I-V curves for set and reset processes at increasing I_C. The set transition from the high resistance state (HRS) to the low resistance state (LRS) takes place around V_{SET} = 2.5 V. During set process, the current was limited by the transistor to increasing I_C = 24 μA, 100 μA and 240 μA. As the compliance current increases, the LRS resistance decreases according to $R = V_C/I_C$, where V_C is about 1.6 V in these measurements [15]. On the other hand, the reset current I_{RESET} increases approximately as I_{RESET} = I_C [15]. The reset voltage V_{RESET} also increases with I_C, due to the increasing voltage drop across the transistor at increasing current [21]. The overall resistance window between the HRS and LRS exceeds 3 orders of magnitude, as already observed in SiO_x-based RRAM [19].

To calibrate the MTS, the device was characterized on a thermal chuck at constant temperature T from 25 °C to 200 °C. The inset of Fig. 2 shows the MTS resistance measured with the 4 point technique, as a function of T. The resistance obeys a linear relationship typical of metallic resistors, namely:

$$R_{MTS}(T) = R_0(1+\alpha(T-T_0)) \quad (1)$$

where T_0 = 25 °C and R_0 is the reference value of the resistance at T_0. The temperature coefficient of resistance is $\alpha = 0.0015$ K^{-1} in good agreement with previous works [16].

TABLE I

Material	k_{th}	ρ
Ti	23 W/(m·K)	negligible
W	166 W/(m·K)	negligible
C	2 W/(m·K)	29000 $\mu\Omega$cm
CF	1.43 W/(m·K)	500 $\mu\Omega$cm
SiO_2/SiO_x	1.43 W/(m·K)	-

While measuring the I-V curves in Fig. 2, the resistance of the MTS was monitored to probe the local temperature T within the device. Fig. 3 shows the measured change of resistance ΔR during the set and reset processes of the device, namely the difference between the measured R and R_0 in Eq. (1). The value of ΔR increases with the applied voltage and current, thus revealing the Joule heating effect within the device. From Eq. (1), one can obtain the local temperature increase $\Delta T = \Delta R/\alpha$ within the MTS during set/reset operation, which is reported as the right axis in Fig. 3. The temperature change ranges from few degrees to about 30 K, with the largest heating observed in correspondence of the highest I_C.

To understand the Joule heating effect in our device, Fig. 4 shows the local increase of temperature ΔT as a function of the device current (a) and power, namely $P = VI$ (b). Data for both positive voltage (set process) and negative voltage (reset process) are shown. In the latter case, all curves overlap along a single universal curve, thus indicating that Joule heating is uniquely controlled by the electric power P according to a linear dependence. This can be understood by the analytical formula for Joule heating:

$$\Delta T = R_{th} P \quad (2)$$

Where $R_{th} = 6.5\times10^4 K/W$ is the effective thermal resistance of the device, describing the heat diffusion arising from the electrical power dissipation within the device. Note that ΔT refers to the effective temperature increase at the MTS, thus is significantly smaller than the maximum temperature at the RRAM filament, where the current and electric field take place. Deviations from the universal linear behavior in Fig. 4 are due to the voltage drop across the transistor during the set transition, which does not contribute directly to the Joule heating.

III. Model

To evaluate the temperature profile within the device from the MTS data during set and reset processes, we first estimated the geometry of the conductive filament (CF) from the experimental I-V characteristics, then we simulated the conduction, Joule heating and heat diffusion by a finite element method (FEM) model in cylindrical coordinates [22].

A. CF size

The local temperature of the device is strongly dependent on the geometry of the CF. We estimate the CF diameter ϕ from the resistance R of the device obtained by electrical characterization. For this purpose, however, the various contributions to the total resistance and their respective scaling with

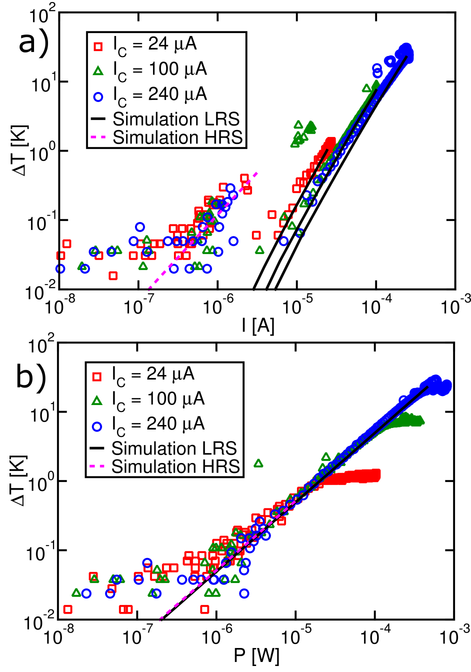

Fig. 4. Simulation of MTS heating during device operation depending on current (a) and power (b) compared with experimental data.

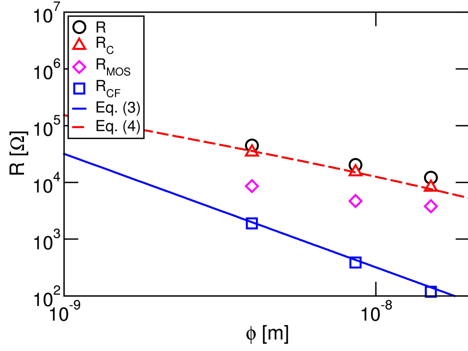

Fig. 5. Analytical and simulated segments of the total resistance of the device

the filament size should be taken into account. The CF was assumed to have a cylindrical shape with a resistance given by:

$$R_{CF} = \rho_{CF} \frac{t_{OX}}{\frac{\pi}{4}\phi^2} \tag{3}$$

where t_{OX} is the SiO_x layer thickness. As the filament is generally much smaller than the electrode size and the carbon resistivity is expected to be higher than the metallic CF, the contribution of resistance of the carbon electrode cannot be neglected. The spreading resistance R_S of the carbon electrode can be estimated analytically by assuming a 45° conical spreading, which yields:

$$R_S = \alpha\rho_C \frac{t_C}{\pi(t_C + \frac{\phi}{2})\frac{\phi}{2}} \sim \frac{\alpha\rho_C}{\frac{\pi}{2}\phi} \tag{4}$$

where alpha = 0.85 is a corrective factor. The transistor resistance was measured experimentally on one-transistor/zero-resistance (1T0R) structures as a function

TABLE II

I_C	ϕ
24 μA	4 nm
100 μA	8.6 nm
240 μA	15 nm

of the gate voltage. From the measured total resistance $R = R_S + R_{MOS} + R_{CF}$, we could extract the CF diameter ϕ in Tab. II. Fig. 5 summarizes the various contribution to R as a function of the extracted ϕ. Note that R_S is the dominant contribution to the total resistance. The carbon electrode can thus be viewed as a heater, thanks to the relatively high resistance and the confined shape (diameter around 70 nm). This analysis thus supports confined structures of the bottom electrode to improve the energy efficiency of RRAM devices.

B. Electrothermal Model

The conduction characteristics of the RRAM device were simulated by assuming an ohmic behavior for LRS and an exponential (Poole) field-dependent current for HRS [23]. Joule heating was described by solving the Fourier heat equation in stationary regime with a generation the current flow inside the filament and the carbon heater:

$$-\nabla(k_{th}\nabla T) = \rho J^2 \tag{5}$$

where k_{th} is the thermal conductivity, ρ is the electrical resistivity, and $J = \sigma\nabla V$ is the current density. An isothermal boundary condition (T = 300K) was assumed at the bottom boundary to account for the heat sink at the substrate, while thermal isolation was assumed on all other boundaries.

C. Simulation Results

The numerical model can reproduce the measured I-V curves in Fig. 2 and the corresponding MTS ΔR and ΔT in Fig. 4 for both LRS and HRS. In particular Fig. 4b shows that the temperature increase in the MTS structure is solely a function of the total dissipated power $P = VI$ in the device, irrespective of the CF size. This can be understood by the MTS temperature increase ΔT_{MTS} resulting from the temperature drop from the hot spot to the MTS.

On the other hand, simulation results indicate the temperature profile depends on the CF size. This is shown in Fig. 6, reporting the simulated structure (a) and the temperature profile for ϕ = 4 nm (b), 8.6 nm (c) and 15 nm (d) for a dissipated power $P = 10\mu$W. The results indicate that the hot spot is located close to the interface between the CF and the bottom electrode, thus supporting the critical role of the bottom electrode heater. Also, the maximum temperature increases as the CF size decreases, thanks to the better current/heat confinement. This is further supported by the results in Fig. 7, reporting the T profile along the cylindrical axis for increasing ϕ (a) and the maximum temperature as a function of ϕ (b)

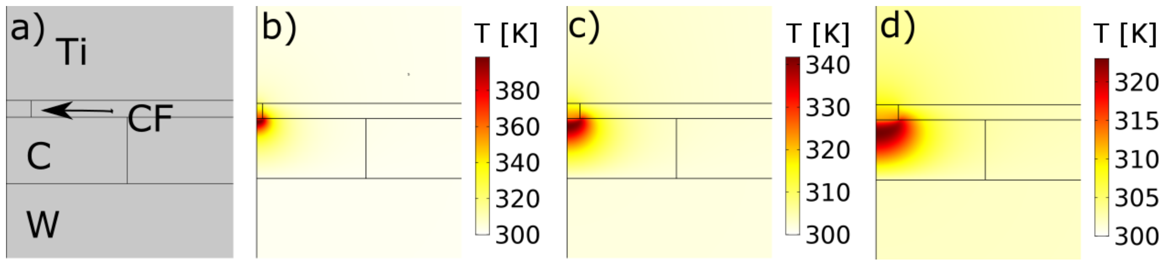

Fig. 6. Simulated temperature map of the carbon heater and CF for different sizes (a) 4 nm, (b) 8.6 nm, (c) 15 nm with the same power bias of 10 μW

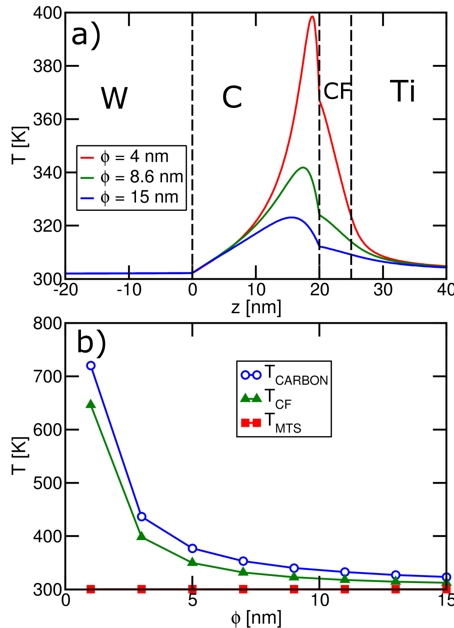

Fig. 7. (a) Simulated temperature profile along the z-axis for different sizes and (b) maximum temperature simulated inside the device depending on filament size with the same power bias of 10 μW

D. Reset Voltage

The model also allows to evaluate the condition for reset transition in the RRAM device. Fig. 8 shows the measured reset voltage V_{RESET} (note that V'_{RESET} in Fig. 2 is increasing with the compliance current because of the transistor voltage drop), at the onset of the reset transition, as a function of I_C. The figure also reports the calculated voltage for which a maximum temperature of 600 K is reached within the CF. The results show that V_{RESET} is almost independent of I_C, and can be viewed as the voltage needed to induce a given critical temperature in the CF to initiate ionic migration, hence reset transition. These results support the MTS technique to provide further insight on the RRAM fundamental switching mechanisms.

IV. Conclusion

We have shown a novel technique to directly study Joule heating in RRAM devices by an integrated MTS structure. Our results show that Joule heating is controlled by the power $V \times I$, and that the bottom electrode plays a crucial role as heater in our RRAM device. The reset operation is shown to

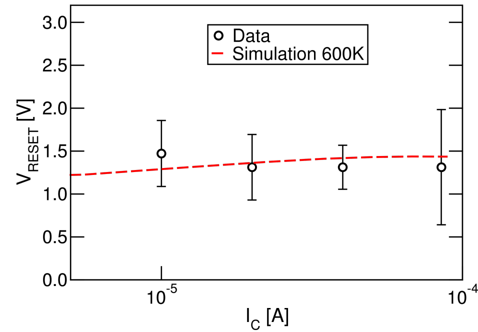

Fig. 8. Experimental median reset voltage for devices after set with different compliance currents and simulated constant temperature condition.

be controlled by the maximum temperature in the CF. These results highlight the importance of a careful thermal design for energy efficient RRAMs.

References

[1] C. Chou *et al.*, in *ISSCC*, Feb 2018, pp. 478–480.
[2] P. Jain *et al.*, in *ISSCC*, Feb 2019, pp. 212–214.
[3] P. Yao *et al.*, *Nat. Commun.*, vol. 8, p. 15199, 2017.
[4] C. Li *et al.*, *Nat. Commun.*, vol. 9, no. 1, p. 2385, 2018.
[5] G. Pedretti *et al.*, *Sci. Rep.*, vol. 7, no. 1, p. 5288, 2017.
[6] M. Ueki *et al.*, in *VLSI Technology*, June 2015, pp. T108–T109.
[7] D. Ielmini and H.-S. P. Wong, *Nat. Electron.*, vol. 1, no. 6, p. 333, 2018.
[8] S. Ambrogio *et al.*, *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2912–2919, Aug 2014.
[9] ——, *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2920–2927, Aug 2014.
[10] W. Wang *et al.*, *Science Advances*, vol. 4, no. 9, 2018.
[11] D. Ielmini *et al.*, *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2049–2056, Aug 2012.
[12] Q. Liu *et al.*, *Adv. Mater.*, vol. 24, no. 14, pp. 1844–1849, 2012.
[13] Y. Ma *et al.*, *ACS Appl. Mater. Interfaces*, vol. 10, no. 27, pp. 23 187–23 197, 2018.
[14] C. Walczyk *et al.*, *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3124–3131, Sep. 2011.
[15] D. Ielmini, *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4309–4317, Dec 2011.
[16] S. W. Fong *et al.*, in *Fourteenth ITherm*, May 2014, pp. 744–749.
[17] R. Jeyasingh *et al.*, *Nano Lett.*, vol. 14, no. 6, pp. 3419–3426, 2014.
[18] Z. Jiang *et al.*, in *2016 IEDM*, Dec 2016, pp. 21.3.1–21.3.4.
[19] A. Bricalli *et al.*, *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 115–121, Jan 2018.
[20] E. Ambrosi *et al.*, *Faraday discussions*, vol. 213, pp. 87–98, 2019.
[21] D. Ielmini *et al.*, *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3246–3253, Oct 2011.
[22] S. Larentis *et al.*, *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2468–2475, Sep. 2012.
[23] D. Ielmini *et al.*, *Nanotechnology*, vol. 22, no. 25, p. 254022, May 2011.