Patterning metal contacts on monolayer MoS_2 with vanishing Schottky barriers using thermal nanolithography

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Two-dimensional semiconductors, such as molybdenum disulfide (MoS_2), exhibit a variety of properties that could be useful in the development of novel electronic devices. However, nanopatterning metal electrodes on such atomic layers, which is typically achieved using electron beam lithography, is currently problematic, leading to non-ohmic contacts and high Schottky barriers. Here, we show that thermal scanning probe lithography can be used to pattern metal electrodes with high reproducibility, sub-10 nm resolution, and high throughput (10^5 μm^2/h per single probe). The approach, which offers simultaneous in situ imaging and patterning, does not require a vacuum, high energy, or charged beams, in contrast to electron beam lithography. Using this technique, we pattern metal electrodes in direct contact with monolayer MoS_2 for top-gate and back-gate field-effect transistors. These devices exhibit vanishing Schottky barrier heights (around 0 meV), on/off ratios of 10^{10}, no hysteresis, and subthreshold swings as low as 64 mV/dec without using negative capacitors or hetero-stacks.

41 As conventional electronic devices reach their limits of performance, a search is underway in the
42 microelectronics industry to find new materials[1], fabrication methods[2], and architectures[3].
43 Conventional lithographic techniques are, in particular, problematic in terms of resolution
44 (optical lithography), operational costs (electron beam lithography, EBL), and their ability to
45 pattern novel electronic materials and architectures. Among various novel materials being
46 considered, two-dimensional molybdenum disulfide (MoS_2) is of particular interest due to its
47 large band gap, low dielectric constant, and heavy carrier effective mass[3-6]. Currently, a key issue
48 in creating high performing field-effect transistors (FETs) based on MoS_2 and other transition
49 metal dichalcogenides (TMDC) films is the poor quality of the metal contacts fabricated on these
50 atomic layers, which gives rise to non-ohmic contacts, high Schottky barriers and large contact
51 resistances[1,7]. Several approaches have been proposed to address these problems[8], including
52 trying different metallic alloys and doping[9,10], using a metallic phase of MoS_2[11] or a h-BN layer
53 as interface between the metal contact and the semiconducting MoS_2 layer[12], and exploiting
54 graphene as contact[13-15]. However, all these strategies are either non-scalable or have not yet
55 been fully developed. They also all rely on conventional fabrication methods, typically EBL, for
56 metal contact patterning.

57

58 EBL is currently the most widespread and reliable nanomanufacturing method for metal
59 electrode patterning when nanoscale dimensions are required. The technique requires ultra-high
60 vacuum (UHV) and does not allow in situ imaging. Its scalability is also limited by the costs and
61 complexity of a multi-beam systems. Furthermore, primary and secondary electrons in EBL, as
62 well as ultraviolet (UV) exposure in optical lithography, can damage 2D materials, from
63 graphene to TMDC films[16-20]. Moreover, resist contamination on the surface of the 2D material
64 is a major impediment for the fabrication of high performing electronic devices[21-27]. Among
65 other nanopatterning methods, laser direct writing is a promising technique that offers far-field
66 three-dimensional, maskless and cost-effective optical beam lithography with high throughput,
67 even if the diffraction-limit is a barrier for achieving nanoscale resolution. Laser direct writing
68 has, for example, been shown to be effective in patterning electrodes by direct laser sintering of
69 metal nanoparticle inks deposited on a substrate[25].

70

71 In this Article, we report a strategy to fabricate metal contacts on 2D materials with high
72 reproducibility. Our approach is based on a double polymer stack chemical etching/lift off
73 process combined with thermal scanning probe lithography (t-SPL). Using a commercial system
74 based on t-SPL[2,28-31], top-gated and back-gated monolayer (a single atomic layer, 1L) MoS_2
75 FETs are fabricated with different metals as direct contacts on the MoS_2. The approach does not
76 require vacuum, allows for in situ simultaneous patterning and imaging of a monolayer of MoS_2,
77 can achieve sub-10 nm resolution, gives rise to no resist contamination, and completely
78 eliminates damage from either electrons or photons. As a result, the t-SPL fabricated FETs
79 exhibit on/off ratios up to 10^{10}, Schottky barrier heights (SBH) close to 0 mV, and sub threshold
80 swings as low as 64 mV/dec without using negative capacitors or hetero-stacks, outperforming
81 EBL results in the literature[4,32-36]. Applications to other TMDCs are also reported. The technique,

82 which currently runs with a single scanning probe, has a throughput similar to EBL and can
83 readily be implemented in a cost-effective manner to multiple probes to increase throughput.

84

85 **MoS_2 FETs fabrication by t-SPL**

86 Our approach to patterning metal contacts uses a two-layer polymer stack (Fig. 1), uniformly
87 spin coated on MoS_2 films. The top polymer layer is locally thermally decomposed/evaporated in
88 less than 1 μs using a heated nano-probe[28-31] in t-SPL (see Supplementary Information, and
89 Supplementary Figure 1, Supplementary Fig. 2, and Supplementary Video 1), while the removal
90 and optimal undercut profile of the exposed bottom polymer layer is obtained by selective
91 chemical etching and prebake conditions (see Methods). Polyphthalaldehyde (PPA)[29] serves as
92 the top layer resist (20 nm thick) due to its remarkable thermal sensitivity, while
93 polymethylglutarimide (PMGI) is used as the sacrificial bottom layer (210 nm thick) for the high
94 yield and high resolution metal lift-off process. Before starting the electrode patterning, the 1L
95 MoS_2 structure is imaged *in situ* underneath the polymer stack via thermal nanoimaging (see Fig.
96 1a, Supplementary Information, and Supplementary Fig. 1). Single-digit nanometer patterns in
97 PPA, with lateral resolution of less than 10 nm and vertical resolution of 1 nm, can be
98 reproducibly achieved[2,37,38] (see Supplementary Fig. 2). Moreover, the PPA thermally
99 decomposed products evaporate immediately without re-deposition on the substrate or
100 contaminating the nanoprobes, facilitating a complete residual-free and clean patterning process.
101 The patterned PPA does not require any chemical development and can readily be used as an
102 etching mask with high mechanical stability. After t-SPL patterning of PPA (Fig. 1b), the PMGI
103 layer is locally exposed without PPA residuals, and the patterned area can be directly imaged for
104 checking the correct alignment of the pattern (Fig. 1c) before initiating the PMGI chemical
105 etching (Fig. 1d). After PMGI selective removal, the patterned MoS_2 contact region is exposed
106 and ready for metal deposition. The final step consists in the evaporation of the metal electrodes
107 (Fig. 1e) and lift-off (Fig. 1f) (see also Methods). Figures 1g-i show optical images of different
108 examples of t-SPL fabricated FETs on 1L CVD and exfoliated MoS_2 flakes, illustrating that both
109 large pads (Fig. 1g) and fine electrodes (Fig. 1h) can be fabricated by t-SPL.

110

111 Imaging by atomic force microscopy (AFM) (see Fig. 1j) indicates that the patterned MoS_2
112 contact region is completely free of any resist residue, whereas the contact region after the
113 conventional EBL process shows considerable resist residues. Extensive AFM characterization
114 of different locations on MoS_2 flakes after t-SPL and EBL fabrication shows in the case of the
115 EBL process damage of the flakes' edges and presence of residuals (see the Supplementary
116 Section 3 and Fig. S4-S6). Furthermore, X-Ray Photoemission spectroscopy (XPS) indicates that
117 these residuals are indeed residues of the PMMA resist used during the EBL process (see
118 Supplementary Section 4 and Supplementary Fig. 7). Figure 1k shows the Raman spectroscopy
119 characterization of a typical exfoliated 1L MoS_2 flake used for FET fabrication, confirming that
120 the E^1_{2g} and A_{1g} modes are separated by 19 cm^{-1}, characteristic of monolayer flakes[39-41]. The
121 exfoliated[42] and CVD MoS_2 flakes used in this work have been all characterized by Raman
122 spectroscopy to confirm their monolayer nature (see Supplementary Section 6 and Fig. 10).

123 Representative AFM images of monolayer exfoliated and CVD flakes used in this work are
124 shown in Supplementary Fig. 11. The t-SPL fabricated 1L MoS_2 FETs channel region is also
125 characterized by Raman spectroscopy after fabrication (see Supplementary Section 5 and
126 Supplementary Fig. 9), confirming that the t-SPL process does not damage MoS_2. We remark
127 that, differently from t-SPL, it has been shown that, during EBL, electron beam irradiation can
128 cause damage in 2D materials[43,44].

129

130 The bottom device layer, in this case monolayer MoS_2, is not heated ($T < 50°C$) during the t-SPL
131 patterning process, as verified by thermal flow finite element simulations (see Supplementary
132 Fig. 3). Moreover, after each writing line, the non-heated nano-probe reads the written line
133 allowing for *in situ* correction, closed-loop patterning, and self-alignment. t-SPL also allows for
134 imaging the surface before patterning using the same, non-heated probe used for t-SPL, for
135 localizing the area where the patterns need to be fabricated and aligning features with nanometric
136 precision, without the necessity of additional markers. The versatility of t-SPL allows the
137 fabrication on a wide range of materials, as shown in Fig. 1i, where we display the optical image
138 of an aligned top-gate (TG) fabricated by t-SPL on an exfoliated h-BN flake (see discussion of
139 Fig. 2), in the SI we also report on monolayer WSe_2 FETs. Finally, the t-SPL throughput can be
140 scaled up by multiplexing the nanoprobe arrays[30] (see Supplementary Fig. 1e), in contrast to
141 EBL in which multiplexing is complex and costly.

142

143 **t-SPL 1L MoS_2 FETs electrical characterization**

144 In order to demonstrate the capabilities of t-SPL, we fabricate dual-gate 1L MoS_2 FETs with
145 aligned patterned top-gate. First, Pd/Au source and drain contacts are fabricated as shown in Fig.
146 1. Then, a 15-20 nm insulating h-BN flake is aligned and transferred on the FET as gate
147 dielectric. After the coating of the PMGI/PPA layers stack, the topography of the system was
148 acquired *in situ* via thermal nanoimaging. This process allows to directly visualize with
149 nanometric precision the source/drain contacts underneath the resist as well as the h-BN flake,
150 and precisely align the top-gate with no need for additional markers (see Supplementary Fig. 12).

151

152 Figure 2a shows a schematic of the cross section of a top-gate 1L MoS_2 FET, with the electrical
153 connections used in the measurements. In Fig. 2b, the optical image of the FET is shown. The
154 regular geometry of the rectangular 1L MoS_2 flake (red dashed line in Fig. 2b, see
155 Supplementary Fig. 13 for the optical image of the pristine flake) allows the precise
156 measurement of the channel length $L = 1.9$ μm and width $W = 3.5$ μm. Figure 2c reports on the
157 room temperature transfer curve of the FET for a drain voltage $V_{ds} = 2$ V, measured by recording
158 the drain current I_d as a function of the top-gate voltage V_{tg}. It features a nearly-ideal 64 mV/dec
159 subthreshold swing, combined with the highest on/off ratio reported in literature for a 1L MoS_2
160 FET of $I_{on}/I_{off} = 5 \cdot 10^9$. In the inset, the top-gate transfer curves are presented as a function of the
161 back-gate voltage ranging from $V_{bg} = -20$ V (yellow curve) to $V_{bg} = +20$ V (blue curve),
162 demonstrating the full functionality of the dual-gate t-SPL patterned FET. The high quality of the

163 t-SPL contacts is demonstrated also in Fig. 2d, where the output curves of the FET for small V_{ds}
164 are presented. The curves, acquired by recording the drain current I_d as a function of the drain
165 voltage V_{ds}, are linear, demonstrating the ohmic character of the contacts.

166

167 For evaluating the performance of the device in terms of on-current I_{on}, we performed additional
168 measurements at higher V_{ds} and V_{tg} after keeping the device in vacuum for 1 week. In Fig. 2e, we
169 report the I_d as a function of the V_{ds} up to 4 V, for different top-gate voltages ranging from V_{tg} = -
170 2.5 V (orange curve) up to V_{tg} = 10 V (black curve). The device features an extremely high
171 I_{on}=154 µA, which gives rise to the normalized value of $I_{on}\cdot L/W$= 84 µA, which is among the
172 highest values reported for monolayer MoS_2 FETs (see discussion of Fig. 5). We remark that the
173 corresponding transfer curve, reported in the inset, features a very low off current I_{off}, leading to
174 the record-high I_{on}/I_{off} = $2\cdot10^{10}$. The equivalency of the source and drain currents, acquired
175 throughout the whole measurements (see Supplementary Fig. 14), confirms the high quality of
176 the h-BN gate dielectric and fabrication process. Fig. 2f reports the forward and reverse transfer
177 curve at V_{ds} = 2 V, plotted both in the logarithmic and linear scale. Importantly, it demonstrates a
178 hysteresis-free transfer curve across the whole range of V_{tg}, due to the absence of defects and
179 trapped charges at the dielectric interface. This provides an additional compelling demonstration
180 that t-SPL enables a residue-free and defect-free fabrication process, which in turn preserves an
181 extremely high quality of the materials and interfaces.

182

183 The electrical characterization of two back-gate exfoliated 1L MoS_2 FETs with Pd/Au contacts
184 fabricated by t-SPL is shown in Fig. 3. The corresponding optical images of the devices are
185 shown in the insets. The devices feature a channel length and width of L = 0.6 µm, W = 1 µm
186 (Fig. 3a) and L = 1.9 µm, W = 3.5 µm (Fig. 3b). Room temperature transfer characteristics (drain
187 current I_d as a function of the back-gate voltage V_{bg}) are measured by sweeping V_{bg} up to +60 V
188 with drain voltage V_{ds} = 2 V. Both FETs show a considerably large on-current of 132 µA and 112
189 µA, which leads to normalized on-current values $I_{on}\cdot L/W$ of 84 µA and 62 µA respectively,
190 combined with extremely high I_{on}/I_{off} of $3.5\cdot10^8$ and $3.4\cdot10^9$, respectively. The subthreshold
191 swing is 500 mV/dec and 400 mV/dec respectively, which is remarkably low for a thick global
192 SiO_2 back-gate[45]. The insets show the corresponding room temperature output curves, featuring a
193 linear I_d (V_{ds}) behavior at all V_{bg}, from -60 V to +60 V, and even at low temperatures (see inset of
194 Fig. 4a), indicating an ohmic contact between the t-SPL patterned electrodes and MoS_2. We
195 remark that, as reported in the detailed comparison with literature of Fig. 5, these back-gate
196 devices feature state-of-the-art on-current combined with record-high I_{on}/I_{off}.

197

198 In a direct metal-MoS_2 contact there are two main components contributing to the contact
199 resistance, the tunneling barrier between the metal and MoS_2 due to the Van der Waals gap and
200 the Schottky barrier between the contact and the channel region. Schottky Barrier Height values
201 vary from 370-38 meV[33-36] for metals in direct contact with 1L MoS_2, to 16 meV when using h-
202 BN/MoS_2 stacks[36]. Values obtained between multilayer MoS_2 and contact metals vary between

50 meV with Ti and 30 meV with Sc[46], larger SBH have been found for monolayer MoS_2 with Ti, precisely 350 meV, in part because of its smaller electron affinity (4.2 eV)[42]. The SBH is related to many factors and it is a complex phenomenon[1] which accounts for the work function difference between metal and MoS_2, diffusion and doping of the metal atoms in the MoS_2 layer[42,47], presence of defects[48], and presence of adsorbates of various origin including resist residuals[1,49]. To evaluate the SBH of the t-SPL patterned electrodes, temperature dependent transfer characteristics are collected on exfoliated 1L MoS_2 FETs with different metal contacts.

First, the transfer curves of the t-SPL patterned FETs with Pd/Au electrodes (as reported in Fig. 3) are obtained at different temperatures at V_{ds} = 0.1 V, as shown in Fig. 4a. For positive gate voltages, the drain current decreases with increasing temperature, indicating a metallic behavior, whereas for negative biases this temperature dependence is reversed, giving rise to insulating characteristics. This transition manifests as a crossing-over at $V_{bg} \sim 10$ V in Fig. 4a, and it is known as metal-insulator transition (MIT)[50-52]. The corresponding output curves at 48 K are plotted in the inset of Fig. 4a, showing a linear behavior even at low temperatures. Together, the metallic temperature dependence shown in Fig. 4a, and the linearity of the I-V curves at all temperatures (see Fig. 3 and inset of Fig. 4a) indicate a vanishing SBH (also confirmed by the Arrhenius plots as a function of V_{bg} as described below here) and an ohmic behavior of the t-SPL patterned FET with Pd/Au electrodes.

Moreover, Al/Au contacts are patterned by t-SPL on 1L exfoliated MoS_2 flake. The temperature dependent transfer curves obtained at V_{ds} = 2 V are shown in the inset of Fig. 4b. To evaluate the SBH, the variations of the current through the device as a function of V_{bg} under different temperatures are used to generate the Arrhenius plots reported in the Supplementary Fig. 15. It is well known that in a FET the current mainly depends on the thermionic emission and the thermally assisted tunneling, and when V_{bg} is below the flat-band voltage, I_d can be written as[1,9,12,34]:

$$I_d = A^*_{2d}\ T^{3/2} \exp\left(-\frac{q\Phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_B T}\right)\right] \qquad (1)$$

where A^*_{2d} is the 2D equivalent Richardson constant, Φ_B is the SBH, T is the absolute temperature, k_B is the Boltzmann constant, and q is the electronic charge. Since we are considering $q \cdot V_{ds} >> k_B T$, Eq. (1) can be simplified to obtain a linear relationship between $\ln(I_d/T^{3/2})$ and $1/T$. In particular, the SBH is determined from the slope of the Arrhenius plots and plotted as a function of V_{bg} in Fig. 4b. It can be clearly seen that the thermionic emission current dominates when V_{bg} is lower than the flat-band voltage, which corresponds to the voltage at which the activation energy stops to depend linearly on V_{bg}. Therefore, the flat-band Schottky barrier height for t-SPL patterned Al/Au contacts can be readily determined from Fig. 4b to be merely 12.5 meV.

To the best of our knowledge, 12.5 meV and the vanishingly small barrier observed in Pd/Au devices are the smallest SBH ever demonstrated in any EBL patterned direct metal contact on MoS_2 back-gated FETs[1,33-35,42,53,54]. The best value reported for 1L exfoliated MoS_2 direct contacts is 38 meV[36] and for multi-layer MoS_2 is 30 meV[46]. We notice that Al/Au contacts give larger SBH than Pd/Au in our t-SPL patterned FETs. The factors that could potentially influence the contact resistance and the SBH in a given metal contact include[42,47 48 33,55] variations in surface contamination, defect and surface states concentration in the material, field emission, metal/semiconductor wave function overlap (predicted for metals on graphene to result in an effective lowering of the metal work function that may also apply to MoS_2), metal-induced gap states (MIGS), defect dominated Schottky barrier height, interface dipole formation, metal−semiconductor interaction induced gap states. Also, complex mechanisms which are metal specifics, have been highlighted as important factors in studying the metal/MoS_2 monolayer interface, for example s-electron metals such as Ag, Al, and Au have fully occupied d-orbitals and interact with MoS_2 weakly, whereas the d-electron metals such as Pd interact with MoS_2 strongly. We argue that the observed absence of damage at the edges and the residual-free surfaces observed for the t-SPL process as opposed to EBL (see Supplementary Fig. 4-7) may be the underlying reason for the observed vanishingly small SBH in the t-SPL 1L-MoS_2-FETs. It is indeed possible that by freeing the metal-MoS_2 interface from polymer residuals, we may change the nature itself of the interface, e.g. by increasing the metal/MoS_2 interaction and the metal-induced-gap-states. Further experiments are required to understand the microscopic origin of the different contact behavior for different metals and for the t-SPL and EBL processes.

Comparison of t-SPL FETs with literature results

To quantitatively characterize the quality of the t-SPL electrodes and compare them with state-of-the-art electrodes patterned with conventional methods, we have derived the contact resistance (R_c) of the different t-SPL fabricated contacts on 1L MoS_2. Since the contact resistance depends mainly on the quality of the contact interface and on the resistivity of the MoS_2 film itself, a reliable comparison should involve MoS_2 films having similar sheet resistance to separate the effect of the contact from the effect of the material properties[1]. Accordingly, in Fig. 5a we plot the contact resistance of t-SPL fabricated electrodes as a function of the sheet resistance ($R_{\square}$) for both top-gate and back-gate devices shown in Fig. 2, Fig. 3 (see also Supplementary Fig. 16a and Fig. 17), Fig. 4 and Supplementary Fig. 19 (blue lines and symbols), and compare these values with the EBL results reported in literature[42,56,57] (red-yellow lines and symbols). We remark that the sheet resistance of a MoS_2 film can be modulated by changing the gate voltage in the corresponding FET.

In general, the contact resistance is expected to decrease with the sheet resistance. For example, the international technology roadmap for semiconductors (ITRS) 22-nm-node requirement for low-standby-power silicon-on-insulator FETs[1], plotted in Fig. 5a (green dashed line), shows that the goal in terms of contacts formation is to reduce the intercept of the linear R_c vs. $R_{\square}$ curves, i.e. to obtain contacts with lower contact resistance for samples having the same sheet resistance.

282 When analyzing the data related to EBL electrodes on MoS_2, we notice that the R_c vs. $R_□$ data
283 points for 1L exfoliated flakes follow the same curve, suggesting comparable contact quality (see
284 the shaded stripe in red, as guide to eyes).

285

286 Here, by using t-SPL to fabricate the electrodes, we show that we are able to dramatically lower
287 the R_c vs. $R_□$ curves for direct metal contacts on 1L MoS_2 in both top-gate and back-gate
288 configuration. This is clearly demonstrated from the blue symbols reported in Fig. 5a. Data are
289 extracted from transport measurements on transfer length measurement (TLM) structures
290 fabricated on chemical vapor deposited (CVD) 1L MoS_2 (see Supplementary Section 11 and
291 Supplementary Fig. 19 and 20), and using the Y-function method to analyze the data from the
292 electrical measurements on top-gate and back-gate exfoliated 1L MoS_2 FETs as reported in Fig.
293 2, Fig. 3 and Fig. 4 (for the Y-function method, see the Supplementary Section 12 and
294 Supplementary Fig. 21). It is evident that the t-SPL patterned contacts show one order of
295 magnitude smaller contact resistance compared to EBL patterned electrodes for MoS_2 samples
296 having the same sheet resistance. The lowest contact resistance obtained for a t-SPL FET with
297 CVD 1L MoS_2 is ~ 20 kΩ·μm[56] while, as expected, the t-SPL FETs with exfoliated flakes show
298 much smaller sheet resistance than CVD MoS_2 with a minimum contact resistance of only 3
299 kΩ·μm at V_{ds} = 2 V, for the device in Fig. 3a. This is one of the lowest values ever reported for
300 direct metal MoS_2 monolayer contact[1,33,42,56,58] at this V_{ds}. For example, Liu *et. al.* demonstrated a
301 contact resistance of 3 kΩ·μm at V_{ds} = 2 V[42]. We notice that the dependence of the contact
302 resistance on the sheet resistance of the exfoliated MoS_2 t-SPL FETs follows the same line as for
303 CVD MoS_2 t-SPL FETs, indicating that the improvement in contact quality is independent of
304 material source or quality. While these curves represent the present benchmark of the t-SPL
305 patterned electrodes, they can certainly be further improved by using additional strategies
306 recently proposed in literature for improving contacts, such as the use of a dielectric tunneling
307 layer[36], 1T phase engineering[11], and the use of graphene for the contacts[15].

308

309 Figure 5b shows the detailed comparison of the on-current $I_{on}·L/W$ and off-current I_{off}/W of the t-
310 SPL 1L MoS_2 FETs, with the best values found in literature. In order to compare effectively the
311 contact quality in FETs with different geometries, the normalization to the channel width and
312 length is crucial. In Fig. 5b red-yellow symbols and lines report the data for EBL 1L MoS_2
313 FETs[3,4,56,59-64], while blue lines and symbols represent t-SPL 1L MoS_2 FETs presented in this
314 work. Noteworthy, the great majority of the EBL FETs are characterized by relatively low
315 normalized I_{on} below 10 μA, and the FETs characterized by higher on-current feature a
316 correspondingly larger off-current, leading to a significant reduction of the I_{on}/I_{off}. Remarkably,
317 t-SPL FETs feature a normalized I_{on} current which is the among the best reported, combined with
318 an extremely low I_{off} current leading to record-high I_{on}/I_{off} between 10^9-10^{10} for 1L MoS_2 FETs in
319 both the top-gate and back-gate configuration.

320

321 In Figure 5c we report the comparison of the performance of t-SPL devices with the best results
322 in literature concerning on-off ratio I_{on}/I_{off}, subthreshold swing SS and normalized on-current

323 I_{on}[4,58,60,62,64,65]. We remark that, here, the comparison is extended to multilayer MoS_2 FETs,
324 which are usually characterized by higher on-currents, and to different strategies for improving
325 the FETs performances, such as the use of negative capacitor gate dielectrics. Moreover, the
326 comparison between FETs fabricated by t-SPL and the best EBL results in literature[4,33-36,42,58,64]
327 for only direct metal contacts on monolayer MoS_2 is summarized, as shown in Table 1. Finally,
328 as an additional test, the back-gate t-SPL devices based on exfoliated 1L MoS_2 is compared with
329 equivalent EBL devices fabricated in our laboratory, with the same contact metals and device
330 geometry. The obtained results confirm the superior performance of the t-SPL devices and are
331 shown in Section 9 (Supplementary Fig. 16-18) and Supplementary Table 1 of the
332 Supplementary Information. Noteworthy, the results of this work, obtained by simple metal
333 patterning via t-SPL, show remarkably better performances in terms of combination of 10^9-10^{10}
334 on-off ratio, nearly ideal subthreshold swing of 64 mV, high normalized I_{on} and zero hysteresis.
335 We anticipate that by combining the t-SPL metal patterning approach with the aforementioned
336 methods, even higher performance MoS_2 FETs can be envisioned.

337

338 To demonstrate the generality of the approach also for other 2D semiconductors, back-gated
339 FETs are fabricated via t-SPL on monolayer WSe_2 exfoliated on Si/SiO_2 substrates. The results
340 are reported in the SI, in Supplementary Fig. 24. Along with these results we also include Table
341 S3 where we compare the performances of a back gated monolayer WSe_2 FET fabricated by t-
342 SPL with data from literature on FETs based on the same type of material. In particular, for a
343 meaningful comparison, we compare the previously published transfer characteristics
344 performances of n-FET WSe_2 with our data, by reporting both maximum on current and on/off
345 ratio for monolayer and few-layer (< 5) n-FET WSe_2. As clear from this Table, t-SPL can
346 produce FETs with transfer characteristics having the highest on/off ratio and on current among
347 n-type monolayer or few-layer WSe_2 FETs.

348

349 Conclusions

350 We have shown that thermal scanning probe lithography can be used to fabricate high-quality
351 metal contacts on 2D materials with high reproducibility. Electron beam lithography is typically
352 used for metal nanopatterning when high resolution is needed, but the need for ultra-high
353 vacuum and high-energy electrons limits its wider application. Compared to EBL, our approach
354 offers advantages in terms of device performance and capabilities, including not requiring a
355 vacuum, even for 14 nm-length channels, and simultaneous in situ imaging and patterning with
356 an overlay accuracy better than 5 nm. We have used our t-SPL-based scheme to fabricate top-
357 gated and back-gated FETs on 1L MoS_2 and 1L WSe_2. By eliminating resist contamination, and
358 damage from either electrons or photons, our MoS_2 FETs show linear I-V curves even at low
359 temperatures, record low Schottky barrier heights (~0 mV), record high on/off ratios (10^9-10^{10}),
360 and exceptionally low SS (64 mV/dec). t-SPL is compatible with standard etching procedures
361 and could potentially be pushed to single-digit-nm spatial resolution, and, by multiplexing with
362 thermal nanoprobe arrays[30,66], to higher throughput. The approach could thus lead to low-cost,
363 no-vacuum, one-step industrial metal nanomanufacturing.

364

365 # METHODS

366 ## Materials

367 We use monolayer exfoliated MoS_2 flakes (from bulk MoS_2, SPI) and monolayer
368 monocrystalline CVD MoS_2 triangular structures (from 2Dlayer) on highly doped Silicon
369 substrate covered with 285 nm of thermally grown Silicon Oxide. Exfoliated MoS_2 samples are
370 dipped for 2 h in Acetone to remove tape residuals, and then rinsed with Isopropyl alcohol
371 (IPrOH) before starting the fabrication. For the top-gated FETs, we use as top-gate dielectric h-
372 BN flakes mechanically exfoliated on SiO_2/Si, which are annealed (300°C, 2h), and then
373 transferred onto the target 1L MoS_2 FET (back-gated) with a dry stamp-assisted pick-and-place
374 process. The thickness of the h-BN flake for the FET shown in Fig. 2 is 15 nm, as measured by
375 AFM. The t-SPL patterning scheme is then used to image and pattern *in situ* the top-gate without
376 markers.

377 ## Device fabrication by t-SPL

378 All MoS_2 samples are kept in contact with HMDS vapors for 90 s to promote polymer adhesion.
379 First, a solution of pure PMGI (Polymethylglutarimide, Sigma) is spin-coated on the samples
380 surface (2000 rpm, 35 s) followed by a quick baking. For device fabrication this step is repeated
381 three times; then, a PPA (Polyphthalaldehyde, Sigma) solution (1.3 wt % in Anisole) is spin-
382 coated on PMGI (conditions: 2000 rpm at 500 rpm/s for 4 s and then 3000 rpm at 500 rpm/s for
383 35 s) followed by a quick baking. With these conditions, a 20 nm thick PPA film on top of a 210
384 nm thick PMGI film is deposited on the samples surface. Patterning of PPA is performed using a
385 commercial NanoFrazor t-SPL tool (SwissLitho AG), which uses hot probes to locally heat a
386 resist[37] with nanoscopic resolution (more details are reported in the SI). During the lithographic
387 writing the tip is heated to reach about 200°C at the PPA surface. Finite element simulations of
388 the heat flow from the hot tip through PMGI, after all PPA is evaporated, have been performed
389 with the FEniCS platform to evaluate the heat temperature underneath PMGI on the MoS_2 layer,
390 as reported in the Supplementary Section 2 and Supplementary Fig. S3. Patterns are performed
391 with a pixel time in the range of 30-70 µs. For patterning large pads (size: 100 x 100 μm^2) the
392 overlay and stitching routine is used[66]. For the chemical etching of PMGI after patterning,
393 samples are immersed in a solution of TMAH in deionized water (Tetramethylammonium
394 hydroxide AZ726 MIF, MicroChemicals) (0.17 mol/L) for 400 s, then rinsed with deionized
395 water (30 s), IPrOH (30 s) and finally dried with N_2. Metal deposition is performed using an AJA
396 Orion 8E e-beam evaporator (Pressure ~10^{-8} torr, evaporation rate: 1 Å/s). Finally, metal/resist
397 lift-off is performed by dipping samples in Remover PG (MicroChem) for a few hours, then
398 rinsing (IPrOH) and drying (N_2). The back-gate t-SPL FETs presented in this paper have been
399 fabricated using different metals: Pd/Au (10 nm/10 nm), Pd/Au (10 nm/20 nm), Al/Au (10 nm/10
400 nm), and Pt/Au (10 nm/10 nm) for exfoliated MoS_2 (see Fig. 3, 4, Supplementary Fig. 15, 16, 17,
401 18, 21 and Supplementary Table 1), and Cr/Au for CVD MoS_2 (10 nm/20 nm) (see
402 Supplementary Fig. 19 and 20). Cr/Au (10 nm/20 nm) is used as metal for the top-gate.

403 ## Electrical measurements

404 Electrical characterization of CVD monolayer MoS_2 is carried out using a parameter analyzer
405 and a home built shielded probe station working in vacuum (10^{-4} Torr) with micro-manipulated
406 probes. A 7651 Agilent DC source, a Keithley KE2400 source-meter and a 34401A Agilent
407 Multimeter are used respectively for applying the gate voltage, the source-drain voltage and to
408 read the drain current. Electrical measurements on exfoliated flakes are carried out following the
409 standard routines for FETs by either using an Agilent 4155C semiconductor parameter analyzer
410 in a vacuum probe station at a pressure of 10^{-3} Torr, or a Keithley 4200-scs semiconductor
411 characterization system in a Lakeshore probe station at a pressure of 10^{-5} Torr. To avoid the
412 capacitive coupling between the back and top-gates during the measurements of the top-gate
413 devices, the back-gate is either grounded or biased.

414 **Samples characterization**

415 Tapping mode AFM images are collected in different areas of CVD monolayer MoS_2 flakes after
416 EBL and t-SPL fabrication and resist removal, in order to systematically investigate the
417 cleanliness of the samples and the presence of residuals from fabrication. The results are shown
418 in the Supplementary Section 3 and in the Supplementary Fig. 4-6. Tapping mode AFM images
419 are also collected to verify the monolayer nature of the CVD and exfoliated MoS_2 samples used
420 in this work (see Supplementary Fig. 11), and before and after electrodes deposition in t-SPL
421 fabrication to assess the resolution of the t-SPL technique (see Supplementary Fig. 2). Images are
422 collected using a Multimode 8 AFM (Bruker) and PPP-NCH tips (Nanosensors).

423 Raman spectroscopy is used to establish the monolayer nature of all the exfoliated and CVD
424 MoS_2 flakes used for t-SPL fabrication (see the Supplementary Section 6 and Fig. 110) and to
425 investigate the contact and channel region for the t-SPL and EBL fabrication (see Supplementary
426 Fig. 8 and 9). Raman spectra are collected using a Horiba LabRAM HR800 system coupled with
427 an Olympus BX41 inverted optical microscope, and using a laser source with excitation
428 wavelength of 532 nm. Laser power is adjusted to avoid sample damage, or any sample
429 modification, as observed by optical microscopy. Spectra are acquired between 100-900 cm^{-1}
430 with 1s exposure time and as an average of 10 different measurements. The peak at 520.7 cm^{-1}
431 from the Silicon substrate is used as a reference for the position of the MoS_2 peaks. Reported
432 spectra in Fig. S8, S9 and S10 are normalized with respect to the MoS_2 A_{1g} peak.

433 XPS spectroscopy is used to investigate the residuals from EBL fabrication, as reported in
434 Supplementary Section 4 and Fig. S7. XPS measurements are performed with a Physical
435 Electronics VersaProbe II system (UHV pressure < 10^{-6} Pa) and using Al Kα radiation (1486.6
436 eV). The sample is mounted on a steel sample holder and grounded. The following conditions
437 are used: analyzer acceptance angle = 20°; take-off angle = 45°; beam size = 200 µm; pass
438 energy = 11.75 eV (C1s); integration time = 200 ms/step; step size = 0.05 eV/step.

439

440 **DATA AVAILABILITY STATEMENT**

441 The data that support the plots within this paper and other findings of this study are available
442 from the corresponding author upon reasonable request

443

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589 AUTHOR CONTRIBUTION STATEMENT

590 X.Z., A.C., E.A., and X.L. patterned the metal electrodes by t-SPL. A.S.M.A. performed the
591 electronic measurements on the t-SPL FETs. X.Z., E.A., X.L., A.S.M.A., D.S. and E.R. designed
592 the electronic experiments and analysed the data on the t-SPL FETs. G.A., and X.L. fabricated
593 and measured the EBL FETs. X.Z., M.S., and E.R. developed the two-polymer stack t-SPL
594 method. W.J.Y. and J.H. designed and analysed the EBL data. T.T. and K.W. provided the h-BN
595 samples. C.A. analysed the XPS data. A.C. and A.K. provided the WSe_2 samples and contributed
596 to corresponding data analysis. B.S.L. and M.L. deposited Pd electrodes on t-SPL FETs. E.R.
597 conceived and analysed all the experiments on t-SPL FETs. X.Z., A.C., E.A., G.A., J.H., D.S.
598 and E.R. contributed to write the article.

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600 FINANCIAL AND NON-FINANCIAL COMPETING INTEREST STATEMENT

601 The authors declare no competing financial interests.

602 ADDITIONAL INFORMATION

603 Supplementary information is available for this paper at https://

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608 **Figure 1. The t-SPL fabrication process**. **a.** *In situ* thermal nanoimaging of the sample
609 topography (see also Supplementary Section 1). Image of a monolayer MoS_2 flake underneath the
610 PMGI/PPA polymer stack (230 nm). Scale bar: 4 µm. **b.** The PPA polymer film is locally
611 evaporated by scanning a heated scanning probe on its surface at a throughput of 10^5 μm^2/h. **c.** *In*
612 *situ* thermal nanoimaging of the t-SPL pattern on PPA. Scale bar: 4 µm. **d.** Chemical etching of
613 the now exposed PMGI polymer film, which uncovers selected areas of the MoS_2 surface. **e.** Metal
614 contacts are deposited via evaporation. **f.** The PMGI and PPA films are removed via a lift- off
615 process. **g, h.** Optical images of final devices fabricated on exfoliated and CVD monolayer MoS_2,
616 respectively. Scale bars: 50 µm (**g**) and 5 µm (**h**). **i.** Optical image of a top-gate contact fabricated
617 on exfoliated h-BN flakes. Scale bar: 4 µm. **j.** Comparison between the exposed contact region
618 after the chemical etching step and before metal deposition in t-SPL (left panels) and EBL (right
619 panels) fabricated FETs on monolayer CVD MoS_2, acquired inside (top panels) and at the
620 boundaries (bottom panels) of monolayer CVD MoS_2. Scale bars: 500 nm. **k.** Typical Raman
621 spectra of monolayer exfoliated MoS_2 used for the fabrication of FETs via t-SPL.
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625 **Figure 2. Aligned top-gate FETs on exfoliated 1L MoS_2 flakes patterned by t-SPL. a.**
626 Schematic cross-section and electrical connections of a top-gate FET. Both the source-drain
627 contacts and the aligned top-gate are patterned via t-SPL. The structure comprises the degenerately
628 doped Si substrate as global back-gate, a 285 nm thermal SiO_2 as back-gate dielectric, and a 15
629 nm h-BN layer as top-gate dielectric. **b.** Optical image of the 1L MoS_2 FET, showing the source-
630 drain Pd/Au electrodes (S-D) fabricated on the 1L MoS_2 (red dashed line) and the aligned top-gate
631 Cr/Au contact (TG) fabricated on the h-BN dielectric. Channel length L
632 = 1.9 µm, channel width W = 3.5 µm. Scale bar: 5 µm. **c.** Room temperature transfer curve of the
633 top-gate FET measured at V_{ds} = 2 V. Subthreshold swing = 64 mV/dec, $I_{on}/I_{off} = 5\cdot 10^9$. In the inset,
634 transfer curves at different back-gate voltages ranging from V_{bg} = -20 V (yellow curve) to V_{bg} = 20
635 V (blue curve). **d.** Small voltage I_d (V_{ds}) curves at different top-gate voltages showing ohmic
636 behavior of the contacts. **e.** I_d as a function of V_{ds} up to 4 V, at different top-gate voltages ranging
637 from V_{tg} = -2.5 V (orange curve) up to V_{tg} = 10 V (black curve), showing a maximum I_{on}
638 = 154 µA. In the inset, transfer curve at V_{ds} = 4 V, features an $I_{on}/I_{off} = 2\cdot 10^{10}$. **f.** Forward (blue
639 dashed line) and reverse (orange line) transfer curves in logarithmic and linear scales. The curves
640 are hysteresis-free in the whole top-gate voltage range.

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645 **Figure 3. Back-gate FETs fabricated via t-SPL on exfoliated 1L MoS_2 flakes. a-b.** Room 648 temperature transfer curves at V_{ds} = 2 V of FETs with Pd/Au electrodes, fabricated on exfoliated 649 1L MoS_2. The Si/SiO_2 285 nm substrate was used as global back-gate and gate dielectric, 650 respectively. The devices feature I_{on} up to 132 μA (**a**) and $I_{on}/I_{off} > 3\cdot10^9$ (**b**). Scale bars: 2 μm 651 (panel **a**), 5 μm (panel **b**). Insets: corresponding room temperature output curves at different 652 back-gate voltages V_{bg}.

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655 **Figure 4. Schottky barrier height (SBH) characterization of t-SPL FETs on exfoliated 1L** 656 **MoS_2. a.** Temperature dependent transfer curves of the t-SPL FET with Pd/Au electrodes 657 reported in Fig. 3a (V_{ds} = 0.1 V). Inset: corresponding output curves of the same FET at 48 K. **b.** 658 Gate voltage dependence of the barrier height for a t-SPL patterned FET on 1L exfoliated MoS_2 659 with Al/Au electrodes, at V_{ds} = 2 V. The deviation from the linear response at low V_{bg} (dashed 660 red line) defines the flat band voltage and the SBH. Inset: corresponding temperature dependent 661 transfer curves at V_{ds} = 2 V.

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666 **Figure 5. Comparison of t-SPL MoS_2 FET performances with literature. a.** Contact 667 resistance R_c of the electrodes as a function of the sheet resistance R_Υ of 1L MoS_2 FETs. The red, 668 orange and yellow lines and symbols represent values extracted from literature for FETs 669 fabricated by EBL. The blue lines and symbols show the results of t-SPL fabricated FETs which 670 are extracted (right to left) from three back-gated FETs fabricated on 1L CVD (see 671 Supplementary Fig. 19), 1L exfoliated MoS_2 flakes (as shown in Fig. 3 and Fig. 4), and a top- 672 gate FET fabricated on 1L exfoliated MoS_2 flake (as shown in Fig. 2). The shaded stripes show 673 the range of data corresponding to EBL data from literature (red) and t-SPL data from this work 674 (blue). The green dashed line represents the ITRS 22-nm-node requirement for low-standby- 675 power silicon-on-insulator FETs with the contact resistance down to 20% of the total resistance. 676 **b.** On-current normalized to the channel width W and length ($I_{on}\cdot L/W$), as a function of the I_{off}/W, 677 for 1L MoS_2 FETs. The red-yellow symbols and lines represent EBL data extracted from 678 literature. The blue symbols and lines show the t-SPL results presented in this work for 1L MoS_2 679 FETs in the back-gate (Fig. 3) and top-gate (Fig. 2) configurations. **c.** In-depth comparison of the 680 performances of the best MoS_2 FETs presented in literature with the t-SPL results presented in 681 this work.

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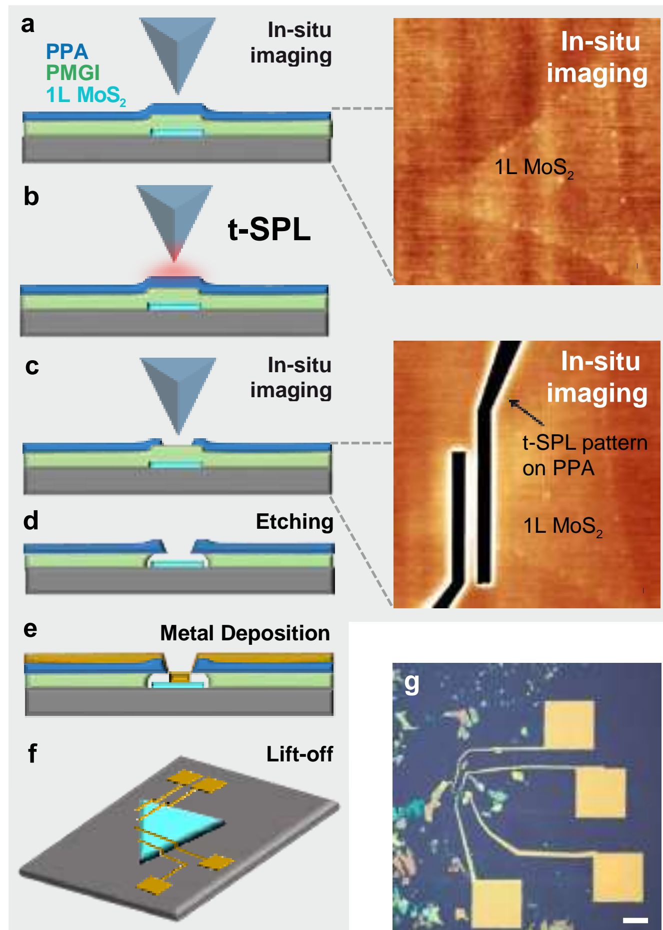
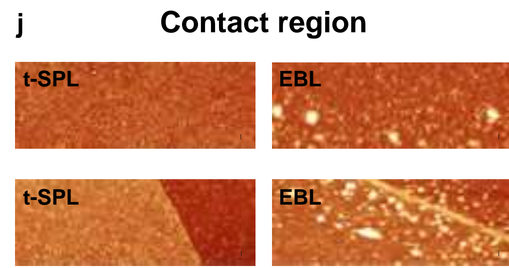
	SBH	Rc	I_{ON} / I_{OFF}	SS	Requires UHV	Simultaneous imaging/ patterning	Throughput	Resolution
t-SPL	~ 0 meV	3-6 kW mm (Back gate) 10 kW mm (Top gate)	10^{10}	64 mV/dec	NO	YES	10^5 μm^2/h	~ 10 nm
EBL in literature	38 meV [36] 55 meV [35] 60 meV [34] 110 meV [33]	3 kW mm (UHV) [58] 7 kW mm [33]	10^7 [33] 10^8 [4]	74 mV/dec [4] 178 mV/dec [64] 410 mV/dec [42]	YES	NO	10^5 μm^2/h	~ 10 nm

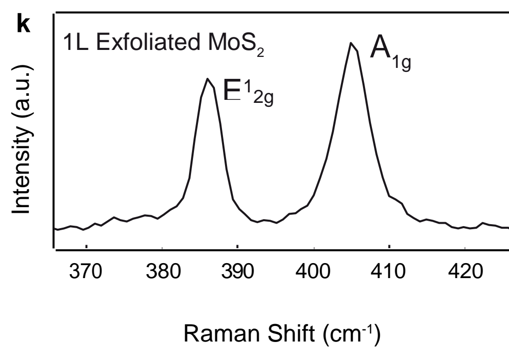
Table 1. Comparison of FETs based on monolayer MoS_2 with metal electrodes in direct contact with MoS_2 (no graphene contacts, h-BN tunneling layers or NC dielectrics).



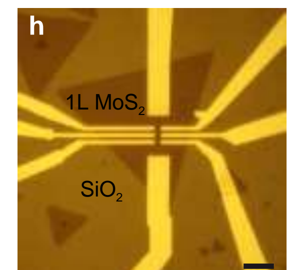
a
PPA
PMGI
1L MoS2
In-situ imaging
In-situ imaging
1L MoS2
b
t-SPL
c
In-situ imaging
In-situ imaging
t-SPL pattern on PPA
1L MoS2
d
Etching
e
Metal Deposition
f
Lift-off
g



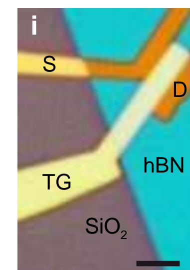
j
Contact region
t-SPL
EBL
t-SPL
EBL



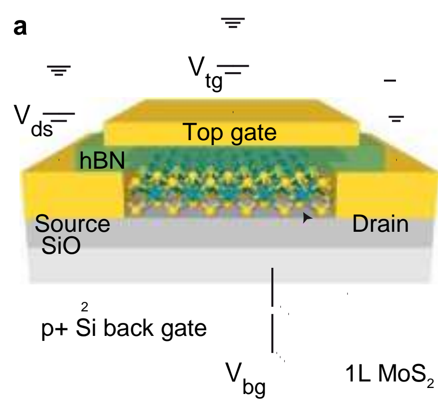
k
1L Exfoliated MoS2
E12g
A1g
Intensity (a.u.)
370
380
390
400
410
420
Raman Shift (cm-1)

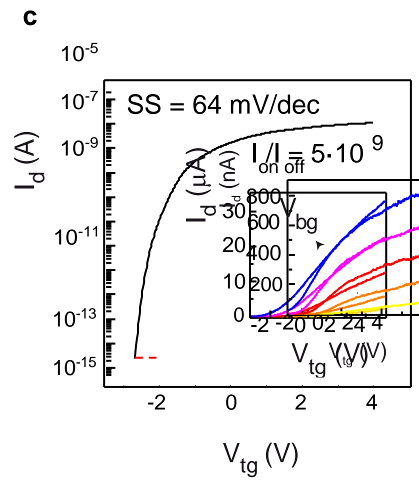


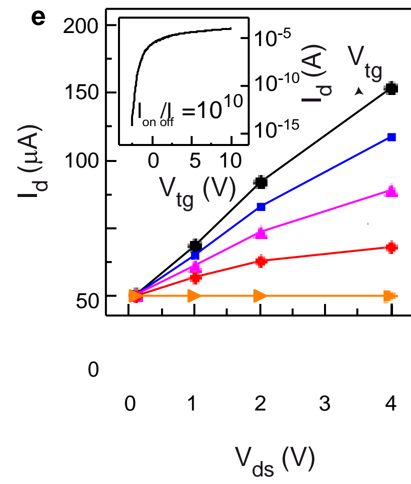
h
1L MoS2
SiO2

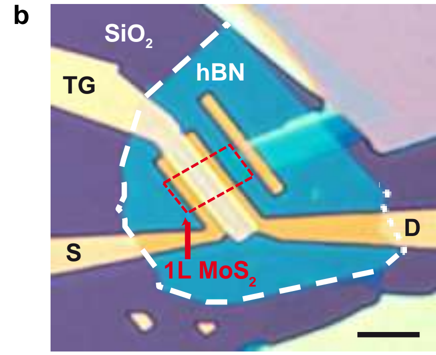


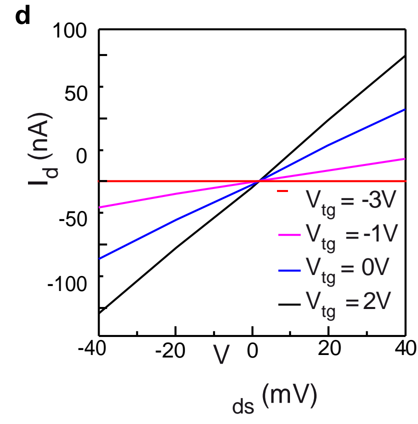
i
S
D
hBN
TG
SiO2

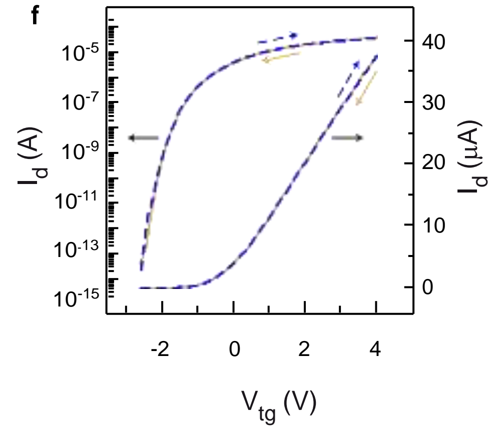

a
V_{tg}
V_{ds}
Top gate
hBN
Source
Drain
SiO_2
p+ Si back gate
V_{bg}
1L MoS_2

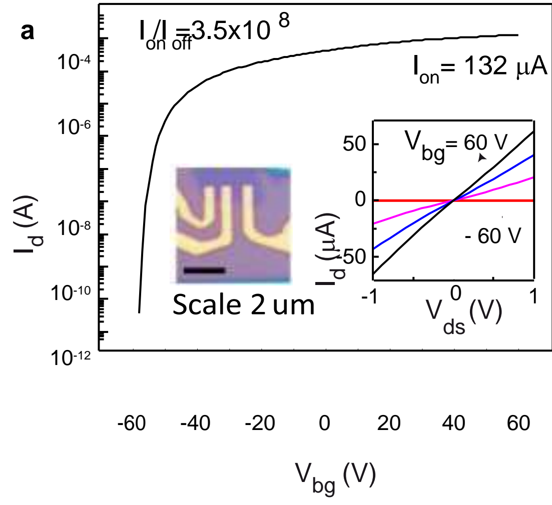

c
SS = 64 mV/dec
$I_{on}/I_{off} = 5\cdot10^9$
I_d (A)
I_d (μA)
I_d (nA)
V_{bg}
V_{tg} (V)


e
$I_{on}/I_{off} = 10^{10}$
I_d (A)
V_{tg}
V_{tg} (V)
I_d (μA)
V_{ds} (V)

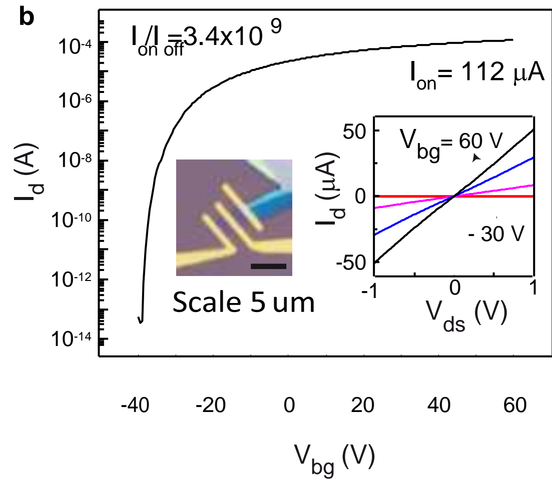

b
SiO_2
hBN
TG
S
D
1L MoS_2


d
I_d (nA)
V_{tg} = -3V
V_{tg} = -1V
V_{tg} = 0V
V_{tg} = 2V
V_{ds} (mV)

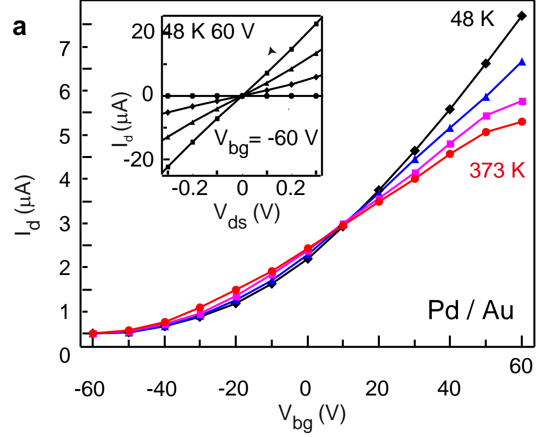

f
I_d (A)
I_d (μA)
V_{tg} (V)



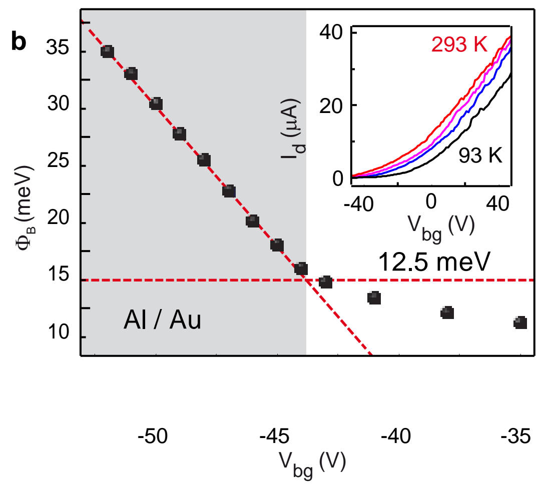
Vds = 2V
W = 1um
L = 0.637 um



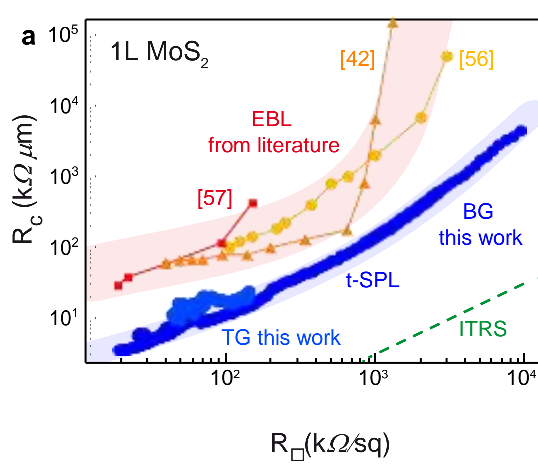
Vds = 2V
W = 3.4 um
L = 1.9 um

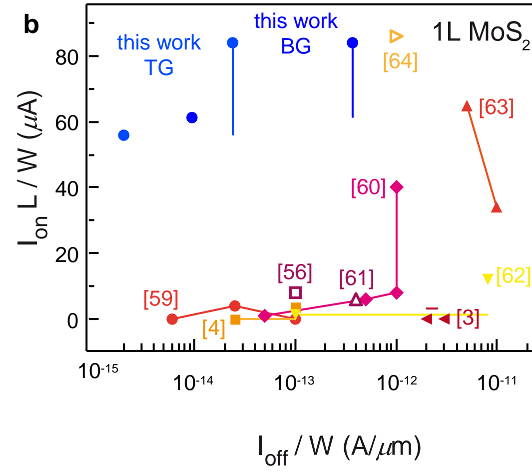


Vds = 2V
W = 1um
L = 0.637 um



Vds = 2V
W = 3.4 um
L = 1.9 um





c

Layers	Configuration	I_{on}/I_{off}, S (mV/dec)	$I_{on} \cdot L / W$ (μA)	Ref.
Multilayer	Bottom Gate Negative Capacitor	10^6 - 10^7, < 60	50	[60]
Multilayer	Bottom Gate (SiO_2) UHV Contacts	N.A.	45	[58]
1L	Top Gate	10^6, 500	11	[65]
1L	Aligned Bottom Gate (Graphene contact)	10^7, 64	1.5	[62]
1L	Top Gate	10^8, 74	3.75	[4]
1L	Top Gate	10^8, 178	86	[64]
1L	Top Gate	10^9 - 10^{10}, 64	84	This work
1L	Bottom Gate (SiO_2)	10^9, 400	62 - 84	This work