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ABSTRACT

A new digital instrument for timing of events is presented. It is based on a reconfigurable, high-performance, 16-channel time-to-digital converter implemented in a Xilinx 7 Series 28-nm field programmable gate array device. Each channel provides timestamps with a least significant bit of 2 ps that states the resolution, whereas instead the single-shot precision is below 12.5 ps rms with the possibility of multihit measures at the maximum rate of 20 MHz. The default width of the full-scale range is 157 μs that can be extended at users choosing up to 15 days by means of proper time tagging procedures made available. The instrument achieves performance in terms of precision, resolution, and full-scale range of measurement at the state-of-art of existing solutions. The novelty is that besides performance, the presented instrument is totally reconfigurable by the user both in the hardware and in the firmware parts. Moreover, novel techniques of event acquisition (e.g., level-zero trigger) are introduced. These further features are not present in any other instrument available nor in the literature or in commerce and constitute a difference with respect to all referenced instruments.

I. INTRODUCTION

The time-to-digital converter (TDC) processing core is based on Tapped Delay-Line (TDL) and instantiated as IP-core module compatible with Xilinx's Field Programmable Gate Arrays (FPGAs) and Systems on Chips (SoCs) of last generation.

The instrument structure is composed of hardware, firmware, and software parts. Three acquisition ways are available for managing properly the timestamps, which fit at best with the philosophy of the applications the TDCs are devoted to. The Level-Zero Trigger (LZT) is a novel technique that allows collecting only the events that follow a user defined pattern. For guaranteeing a continuous acquisition of absolute timestamps with a large range (up to 15 days), a Time-Tagging Mode (TTM) is available. Furthermore, a lite version of the TTM called MultiHits Acquisition (MHA) is integrated; in this sense, it is possible to acquire absolute time measures of several events into a dynamic range of 157 μs with respect to a trigger signal provided by the user.

The instrument can be reconfigured by the final user both in firmware and hardware parts. In particular, the firmware and the software associated with the hardware are modularly structured so that the processing is optimized by partitioning the computing tasks in parallel segments.

All characteristics of the instruments have been experimentally validated. In Sec. IV, we do not describe experiments in detail, in order to limit the length of the manuscript. In fact, we favor the discussion of the results of the experiments with the instruments under comparison.

The extremely wide evidence of applications, where the timing of signals is a fundamental request both as single and especially multiple simultaneous measures, is continuously promoting the development of innovative techniques and the design of devices for their implementation.[1]

The process of measurement consists in recognizing events and providing their timestamp, i.e., the representation of the time they occur. Since this timestamp is always referred to a reference instant, in practice, the measurement consists in calculating the time interval between a couple of "start" and "stop" instants. Furthermore, the timing measures are not used only for direct evaluations, indeed there are many physical phenomena observed in an indirect way.

So, a time interval can represent a space distance in Time-of-Flight (ToF) applications[2] or can be used for extracting the spectrum of a material in Time-Correlated Single Photon Counting (TCSPC)[3,4] and in Time-of-Flight Mass-Spectroscopy (ToF-MS)[5] or for getting the fluorescence of a substance by means of Fluorescence Spectroscopy (FS).[6] Moreover, the concept of ToF can be extended in bi- and tri-dimensional imaging. Time-of-Fly Laser-Raging (ToF-LR)[7] and Time-of-Fly Positron Emission Tomography (ToF-PET)[8] are the most significant examples.

For completeness, we have to say that a new generation of electronic devices, such as Analog-to-Digital Converters (ADCs)[9] and Phase-Locked Loops (PLLs),[10] have been redesigned using the "time-mode" approach. Here, developing new time-interval-meters with higher and higher performance allows us to increase the quality of the measures so improving the result of the application in which they are used. Historically, the well-established method for high-accuracy measurement of time intervals is the Time-to-Amplitude Conversion (TAC).[11,12] However, nowadays in the digital era, the timing information can be converted directly in a digit without using any analog circuit. These systems, called Time-to-Digital Converters (TDCs), are the landmark for determining the time instants at which digital events take place. Nowadays, TDCs are the building blocks of "time-mode" circuits.[13] These circuits code of information by measuring the time instants at which the electrical signals (voltage and current) cross reference values, which is exactly the opposite of what happens in voltage and current mode circuits. Therefore, time measurement is at the basis of this new philosophy of processing. The key point is that time-mode circuits benefit at most from technology scaling.[14–16] In fact, the switching characteristics of MOS transistors are improved to such an extent that the time resolution of digital circuits decisively surpasses the resolution of analog ones implemented in active devices scaled in the nanometer range. Moreover, it is important to mention that the analog circuits implemented by such small devices usually have quite poor performance. Moreover, since fully digital, TDCs offer features that are not possessed by either voltage-mode or current-mode options.[17] Among them, full programmability, tunable characteristics, easiness of portability, low-power consumption, high-speed operation, lower migration cost from one generation of technology to another, less sensitivity to interferences such as cross talk, switching noise, and substrate coupling are of primary importance, which have a detrimental impact on the performance of either voltage and current-mode circuits.

Since a few years, digital programmable logic devices have made feasible the implementation of synchronous and low-performance TDC architectures.[18] Today, the last generation of FPGAs and SoCs are characterized by lower and lower propagation delays that make feasible the realization of high-resolution and high-rate asynchronous TDCs. Moreover, the abundance of logic resources allows the implementation of more and more complex and effective calibration algorithms that allow achieving performance such as precision, accuracy, and temperature stability comparable with Application Specific Integrated Circuit (ASIC) realizations at similar technological nodes.[19–21] In this way, all the well-known advantages of using programmable devices are exploited, such as reduced time-to-market and easier migration of processing architectures among devices, just to name a few in addition to the general advantages of the digital systems mentioned above. In particular, the implementation of multichannel architectures becomes straightforward while keeping on foreground the functional performance.[22–24] This leads to a new generation of tunable Hardware Description Language (HDL) TDCs where the user can easily customize the system inside some range of choices, maintaining at the same time the portability between different programmable devices.[25,26]

As important as the architecture and the relative performance is the management of the timestamps produced by the TDC that needs different acquisition modes tailored on specific application targets. Well-known examples in the literature are the "time-tagging" mode that allows us to get measures at a relative low rate for long time[27] and several multihit solutions that permit to acquire relative few events at a high rate.[28]

Generally, in a physical experiment based on high-performance time measures, after the data collection (e.g., "time-tagging," multihit) all timestamps are elaborated in the postprocessing mode. In this way, a huge amount of memory and bandwidth to store and route the information is mandatory due to the necessity of all timestamps to have a high-rate and large number of bits (high-resolution over a wide dynamic-range) for guaranteeing high-performance. However, only a restricted number of these timestamps are correlated and represent the observed event, while the main part of them is due to random events. For this reason, a novel technique called Level-Zero Trigger (LZT) is proposed. With respect to the "time-tagging" and multihit solutions, the LZT allows filtering at the firmware level all the timestamps in real-time, acquiring only those that follow a user defined pattern that models the time response of the physical event. In this way, it is possible to discard useless data with important memory and bandwidth saving.[29,30]

This work deals with the design and realization of a full programmable and multichannel instrument for timing of signals, which is based on a recent TDC architecture tailored for the last generation FPGA devices as IP-core. The instrument structure is a hardware, firmware, and software bundle for high-performance time measures in experiments where very fine time resolving is a primary request. The synergy of firmware and software maximizes the performance of the instrument also in real-time applications in terms of high-resolution and high-precision over a wide full-scale range, but also includes features like high full-scale range, high acquisition rate, thermal stability, real-time processing, flexibility, modularity, portability, low time-to-market, and at last controlled implementation costs.[31–33]

II. TDC IP-CORE

Programmable logic devices, especially FPGA and SoC, allow us to implement TDCs with different kinds of structures. Looking into the literature, we can roughly divide these architectures between TDCs based on feedback (FB) circuits,[34,35] e.g., ring-oscillators, and feedforward (FF) ones based on delay-lines.[34–36]

The high difference of propagation delay values among combinatorial logic elements, mainly due to the scaling down of technology, favors the implementation of feedforward solutions with respect to the feedback ones. To confirm this, we can consider the worsening in resolution from 5 ps to 63.3 ps shown by two TDCs based on a ring-oscillator implemented in 28-nm[34] and 90-nm[35] technology, respectively. Differently, a TDC based on delay-line offers a resolution of 75 ps in 130-nm,[36] 50 ps in 90-nm,[37] and

TABLE I. Comparison of the resolution of the proposed TDC IP-core with respect to architectures present in the literature of TDCs implemented in FPGA. FB and FF stand for "feedback" and "feedforward," respectively.

	Resolution (LSB) (ps)	Architecture	Technology (nm)	Subinterpolation
Reference 34	5	FB	90	No
Reference 35	63.3	FB	28	No
Reference 36	75	FF	130	No
Reference 39	10	FF	130	(Average)
Reference 37	50	FF	90	No
Reference 38	30	FF	65	No
Proposed TDC	2	FF	28	Yes

30 ps in 65-nm[38] technology. Moreover, to overcome the limit of resolution due to the minimum propagation delay of the logic, further mechanisms of averaging and calibration are inserted into delay-line TDC architectures, lowering the resolution down to 10 ps in a 130-nm FPGA device.[39]

The different propagation times of signals through the cascaded bins constituting a delay-line implemented in a FPGA device causes not uniform quantization.[40] These differences, in the case of averaging, have a negative impact on resolution and precision and severely limit the linearity. The slowest bins, called ultrabins, are main responsible for this. As a consequence, subinterpolation algorithms and dynamic calibration procedures are mandatory, for reducing the effect of ultrabins and improving the linearity. These evidence are summarized in Table I.

Precisely, the subinterpolation consists in merging different measurements coming from several TDLs composed of "real bins." In this way, it is possible to obtain a Virtual Tapped Delay-Line (V-TDL) composed of "virtual bins" characterized by a faster propagation delay. Different from a standard average process on a not uniform quantization, if one of the measures falls in the ultrabin, this does not limit the resolution.[41] Furthermore, the dynamic calibration allows compensating both the nonlinearity of the delay-line and its thermal drift.

The implemented TDC IP-core is a user friendly and multiplatform module. It has 16 channels and provides high-resolution and high-precision by means of the Super Wave Union (SuperWU) subinterpolation[39,42,43] of each channel, whereas the Nutt interpolation allows a wide full-scale range and a multichannel structure.

The measurement of the time interval limited by start event i and stop event j, T_{ji}, is calculated as the difference between the timestamps T_i and T_j as shown in Fig. 1,

$$T_{ji} = T_j - T_i. \tag{1}$$

According to the Nutt technique of interpolation, the generic timestamp T_i is composed of a "coarse" (T_i^{COARSE}) and a "fine" (T_i^{FINE}) contribution (Fig. 1), i.e.,

$$T_i = T_i^{COARSE} - T_i^{FINE}. \tag{2}$$

For doing this, the IP-core implements two different types of TDCs (Fig. 2). A synchronous Coarse-Counter (CC) returns the coarse part T_i^{COARSE} of the timestamp by counting the number of clock periods between i and the reference zero time, i.e., the output of

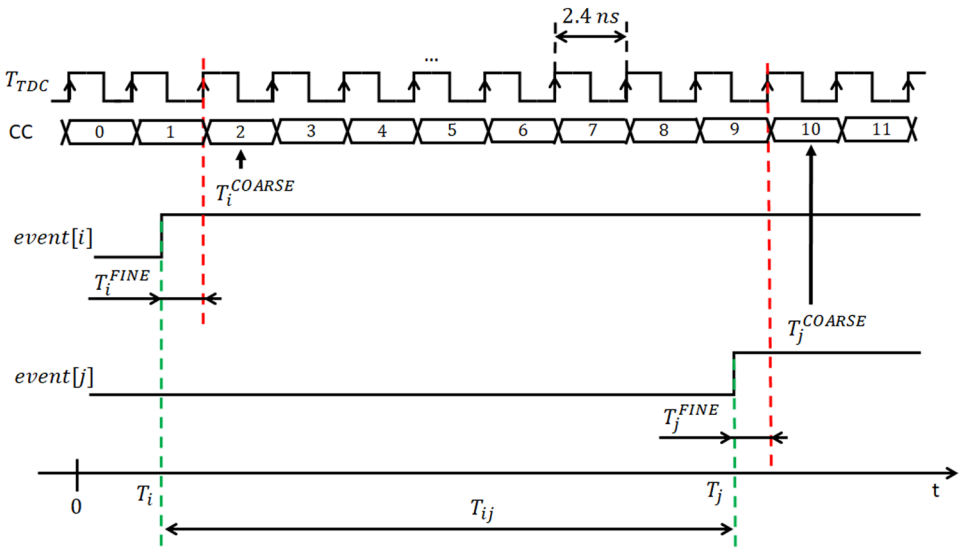

FIG. 1. Timing diagram of the calculation procedure of the timestamps T_i and T_j of the events i and j using the Nutt technique of interpolation.

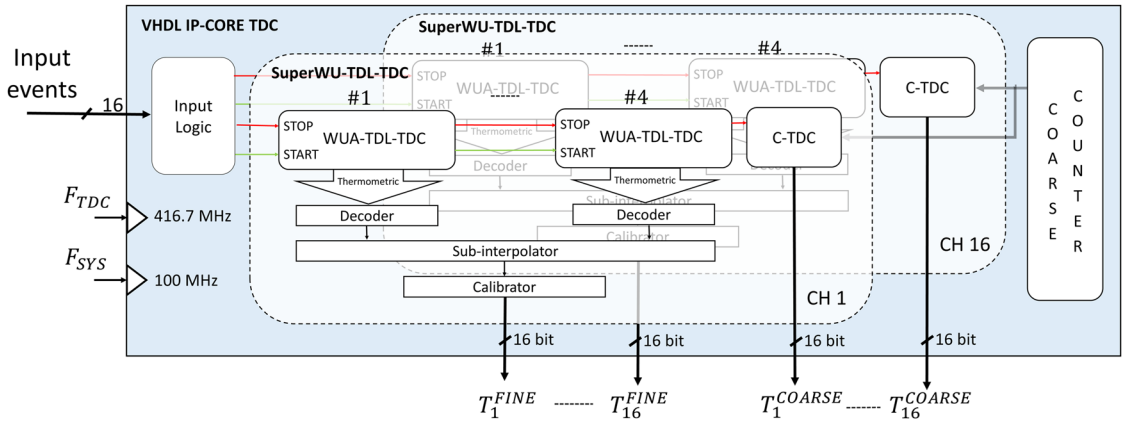

FIG. 2. Block diagram of the TDC IP-core, where the two types of TDCs implemented, C-TDC and TDL-TDC, are put in evidence. In the TDL-TDC block, the implemented subinterpolation method, in this case wave union A, is also specified.

the Counter-TDC (C-TDC). The fine part of the timestamp T_i^{FINE} is measured by a subinterpolated Tapped Delay-Line TDC (TDL-TDC) as the difference between the distance of the event i from the following clock edge.[32] The number of bits of the coarse-counter determines the full-scale range of the instrument.

So, the fine contribution is provided by a Super Wave Union Tapped Delay-Line TDC (SuperWU-TDL-TDC)[43] synchronized with the C-TDC. The SuperWU-TDL-TDC implements the subinterpolation of 4 Wave Union A Tapped Delay-Line TDCs (WUA-TDL-TDC)[19] that performs 2 measurements in parallel for a total of 8 fine measurements for each single event on the relative channel.[41]

The implemented subinterpolation algorithm speeds up the TDL, thanks to the parallel structure that makes it equivalent to a Virtual Tapped Delay-Line (V-TDL) composed of 1200 virtual bins instead of 150 real ones, which are, in average, 8 times faster. As negative by-side effect, this procedure adds a further jitter component called equivalent-time noise,[43] which increases with the subinterpolation order and is caused by the mechanism of generation of the replicas for the multiple measures performed. In this case, an improvement of a factor 8 is enough to achieve a resolution [least significant bit (LSB)] of 2 ps while keeping negligible the equivalent-time noise. This guarantees single channel precision (σ_{TDC}) below 9.5 ps rms. This characterization has been performed using a pure digital signal, with a negligible jitter, at the input of the TDC-IP.

TABLE II. Comparison of the most relevant figures of merit of the proposed TDC IP-core with respect to TDCs at the state-of-the-art implemented in FPGA proposed in the literature.

	Resolution (LSB) (ps)	Precision (ps rms)	INL (ps)	IP-core organization
Proposed TDC	2	9.7	4.2	Yes
Reference 42	N.A.	8.7	N.A.	No
Reference 56	2.93	4.2	11.7	No
Reference 57	3.29	4.2	6.58	No
Reference 58	2.5	6.7	7.5	No

The synchronous parts of the TDC logic, such as dynamic "bin-by-bin" calibration,[19,20] decoding,[44] and ancillary finite-state machines, run at the system clock (f_{CLK}) of 100 MHz. Each single channel achieves a maximum rate of measure of 20 MHz with power consumption below 13.8 mW, using 3975 flip-flops (FFs), 3684 Look-Up Tables (LUTs), 1 DSP, and 54-kbit BRAM, which is in the first approximation an occupancy below 1% of the available resources in the considered device.

As Table II shows, the proposed HDL module achieves performance comparable to the state-of-the-art of ASIC and FPGA solutions. Furthermore, the organization of the firmware as an IP-core allows easily the migration of the TDC among all last generation Xilinx FPGAs and SoCs, that is, Series-7, UltraSCALE and UltraSCALE+.

III. INSTRUMENT STRUCTURE

The instrument is composed of the analog front-end for discriminating time events, which allows the simultaneous acquisition of up to 16 events carried in by single-ended signals, the processing section programmed with the custom firmware that allows different acquisition modes, various communication modules (e.g., USB 3.0 and Ethernet links), and the software running on a generic computer (Fig. 3).

A. Analog-to-digital conversion of events

The role of the analog front-end is to convert into digital pulses the time events present in input analog signals. The discriminator of events is an ultrafast and low-jitter comparator (Analog Devices ADCMP607BCPZ[45]), whose output is a logic level in the Low-Voltage Differential Signal (LVDS) format. The user can set the threshold of the comparator with a resolution of 50 μV by means of two 16-bit and 8-channel I^{2}C-programmable DACs (Analog Devices AD5675R[46]). Moreover, the user can switch from DC to AC coupling through a tunable high-pass filter if the rejection of a bias is requested.

The analog section is designed for minimizing any effect of cross talk by means of proper routing rules based on fully

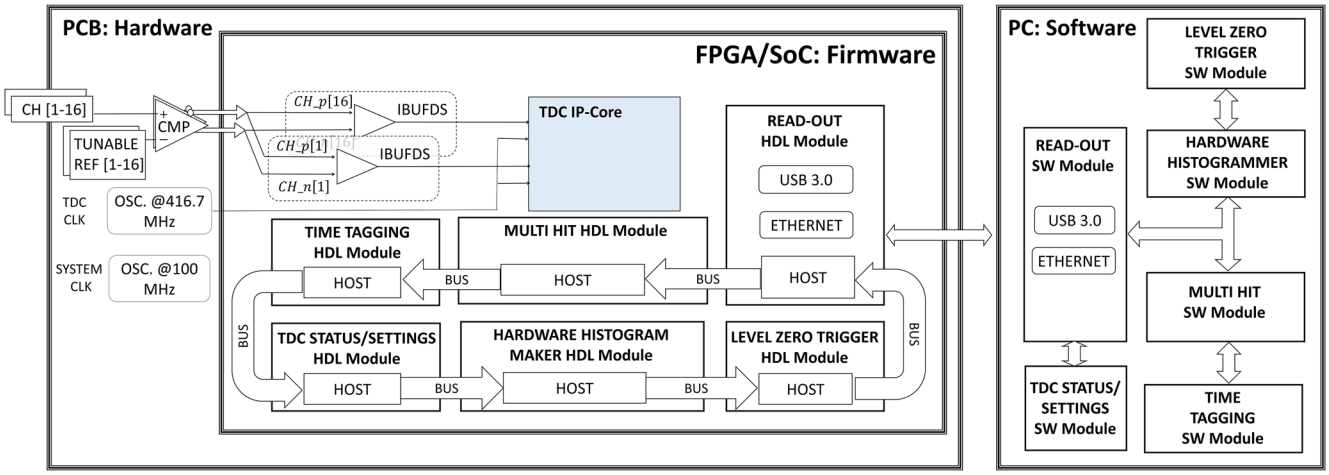

FIG. 3. Schematic overview of the complete structure of the instrument. The shaded region highlights the position of the TDC IP-core.

differential connections, isolation among traces, and impedance matching. Decoupling between analog and digital sections guarantees very low ground bounce that minimizes the threshold jitter during the operation of comparison. This allows us to achieve a contribution of timing jitter (σ_J) lower than 7 ps rms, which has been calculated by subtracting the precision obtained with a pure digital signal (σ_{TDC}) to the precision of the measurement achieved by a weak analog signal with 10 ns rising edge and 200 mV maximum amplitude,

$$\sigma_J = \sqrt{\sigma_{CH}^2 - \sigma_{TDC}^2}. \tag{3}$$

B. Processing unit and firmware

In order to offer the maximum versatility of the system, the processing section of the instrument has been designed as a carrier of replaceable micromodules equipped with different Xilinx FPGAs and SoCs.[48] In this way, the migration of the custom modular firmware is feasible through all Xilinx 7 Series, UltraScale and UltraScale+ FPGAs and SoCs.

Therefore, the proposed instrument is reconfigurable in a sense of both of firmware and hardware.

The instrument configuration here considered (Fig. 4) is equipped with the module TE0712-02-200-2C by Trenz Electronics[47] that hosts an industrial 28-nm programmable Xilinx Artix®-7 XC7A200T-1 FPGA (33 650 SLICEs, 13 140-kbit BRAM, 740 DSPs) in package of area 19 × 19 mm^2.

In the following, we focus on the most relevant features of the firmware highlighting the factors that primarily influence the performance of the instrument and are under user's control.

The firmware is organized as a daisy chain bus with a high grade of modularity, where the TDC IP-core calculates the timestamps and other ancillary modules perform their real-time processing (Fig. 3). The read-out module, which is the default master of the bus, implements USB 3.0 and Ethernet interfaces. Timestamps from the TDC IP-core are sent to one or more acquisition modules, which have custom packagers that send data to the host PC. Packagers and read-out stage communicate using the daisy chain bus at the rate of 80 MB/s. Also, the user's settings are sent from the host PC to the processing unit through the daisy chain bus.

One of the most significant degrees of freedom at user's availability is the set of ways of acquisition of the timestamps, i.e., Level-Zero Trigger (LZT), Time-Tagging Mode (TTM), and MultiHits Acquisition (MHA). Each one of these ways has been developed for maximizing the "acquisition efficiency." In this sense, the LZT allows filtering in FPGA and acquiring in software only the timestamps that follow a specified pattern; the TTM acquires all the timestamps extending the dynamic range up to some days without the impact on the resolution; the MHA permits to work at the maximum possible rate acquiring timestamps with the best resolution inside the dynamic range.

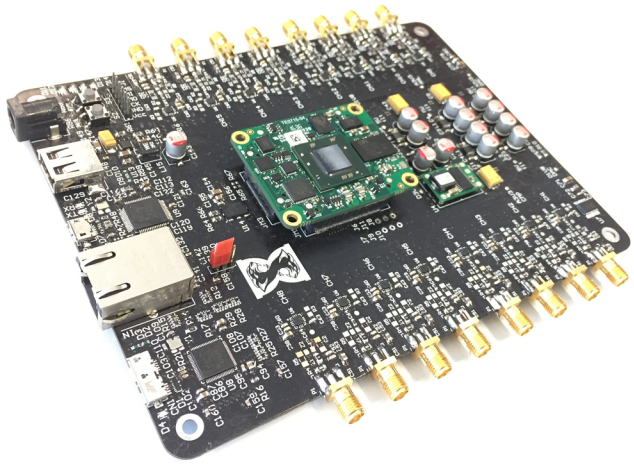

FIG. 4. Picture of the instrument with the piggyback processing micromodule mounted in the middle through connectors. Changing this module allows also the hardware reconfiguration of the instrument.

The level-zero trigger module is devoted to collect only the measures of events whose sequences of start and stop instants follow a programmable pattern in a defined time window. In run-time and via software, the user can set all start and stop conditions and the acquisition windows with a resolution of 10 ns. Therefore, it is possible to discard inside the FPGA the events that are not compliant with the specified pattern. For instance, this technique is suited for discriminating real events from dark counts, thus improving the efficiency.[30]

In this way, the bandwidth of the interconnection between TDC and PC and the storage memory are only occupied by those timestamps that are filtered by the firmware.

The user can set in run-time all the start and stop conditions, by means of the so-called AND-mask and OR-mask (Fig. 5), and the maximum measure interval between them. The timestamps filtered by the level-zero trigger are sent to the PC at a maximum rate of 10 Mmeasures/s shared between the 16 channels. In the LZT, the concept of "acquisition efficiency" consists in minimizing

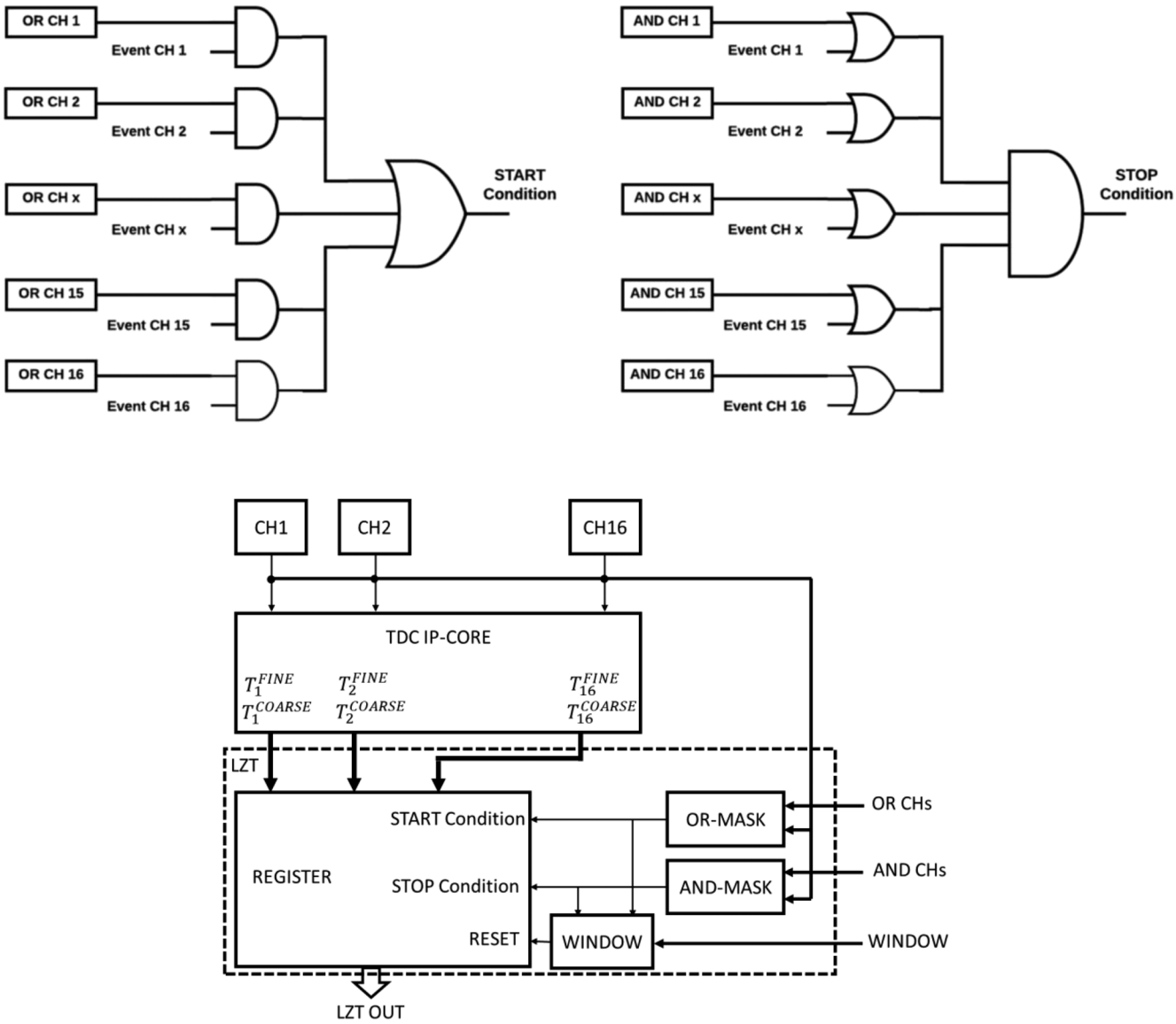

FIG. 5. If an event at the generic *x* input can start a measurement, its corresponding position in the OR-mask (OR CH*x*) is set equal to "1" (top left). This is sent to a 2-input-AND gate together with the *x* input signal. When the AND condition is true, the output of the OR gate, collecting all AND-gate outputs, goes high and the LZT starts to store timestamps (bottom). If the generic *x* input has to be present for the validity of the measurement, its corresponding position in the AND-mask (AND CH*x*) is set equal to "0" (top right). This is sent to a 2-input-OR gate together with the real *x* input signal. The collected timestamps are considered valid if all events having "0" in the AND-mask arrived before the end of the window (bottom).

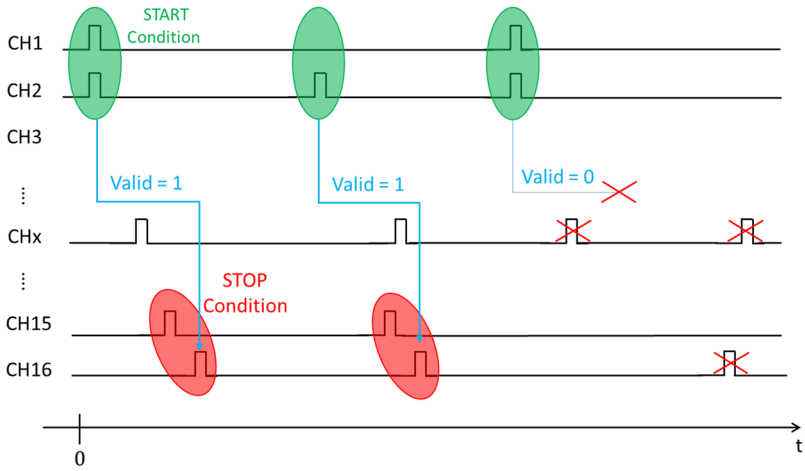

FIG. 6. Timing diagram of the acquisition with level-zero trigger. Channels 1 and 2 (CH1, CH2) are in OR-mask, whereas channels 15 and 16 (CH15, CH16) are in AND-mask defining START and STOP conditions, respectively.

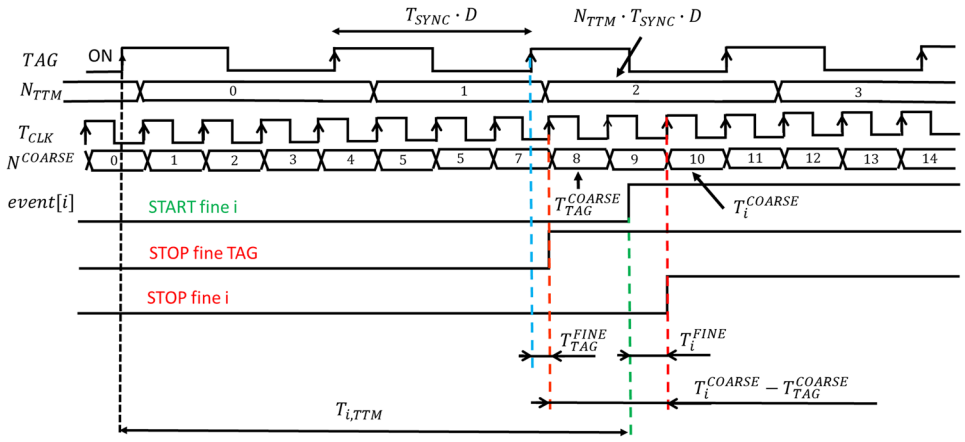

FIG. 7. Timing diagram of the calculation of the absolute time-tag $T_{i,TTM}$ of the *i*th event.

the filtering effort processing only the class of timestamps required (Fig. 6).

Thanks to software flexibility, the Time-Tagging read-out Mode (TTM)[48,27] extends the hardware full-scale range until several days at the maximum measuring rate of 1 MHz. In this module, the "acquisition efficiency" consists in getting the maximum dynamic range possible at the maximum resolution available. For doing this, an extra periodic signal called *SYNC*, at frequency f_{SYNC}, correlated with the input events, is introduced.

Generally, the *SYNC* is a very fast signal obtained, for instance, from the optical pulse train of a laser and is the absolute time reference of the events under measurement. Instead, the other input events are obtained by detection of the photons inside the optical pulses.

Since f_{SYNC} is fixed by an external source, the *SYNC* can be decimated of a tunable integer factor D to get the *TAG* signal,

$$f_{TAG} = f_{SYNC}/D. \tag{4}$$

The edges of the *TAG* signal increment a 48-bit counter N_{TTM} synchronous with T_{CLK}. Since it is impossible to lock in phase with

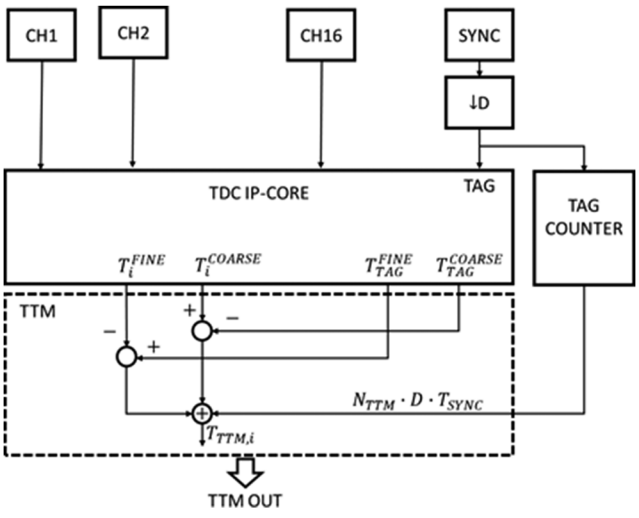

FIG. 8. Block diagram of TTM firmware.

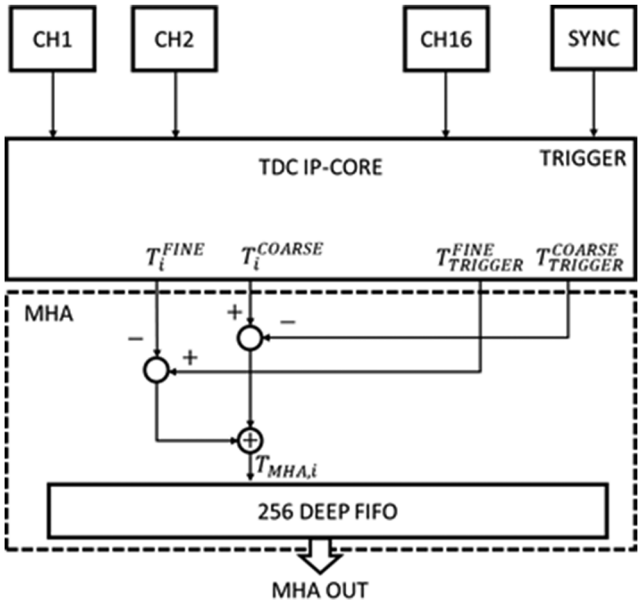

FIG. 9. Block diagram of MHA firmware.

the necessary precision the *SYNC* with the clock of TDC IP-core (T_{CLK}), an ancillary channel of measure is requested. It measures the time position ($T_{TAG}{}^{COARSE}$ and $T_{TAG}{}^{FINE}$) from the rising edge of the TAG (i.e., the decimated *SYNC*) with respect to the rising edge of T_{CLK} (Fig. 7). Consequently, the components of the timestamp of the *i*th event ($T_i{}^{COARSE}$ and $T_i{}^{FINE}$) are corrected by the measurement of the reference *TAG* edge ($T_{TAG}{}^{COARSE}$ and $T_{TAG}{}^{FINE}$), and the absolute time-tag ($T_{TTM,i}$) is

$$T_{TTM,i} = N_{TTM} \cdot T_{SYNC} \cdot D + \left(T_i^{COARSE} - T_{TAG}^{COARSE}\right) + \left(T_{TAG}^{FINE} - T_i^{FINE}\right). \quad (5)$$

Figure 8 shows the block diagram of the TTM. The timestamps produced by the TDC IP-core are managed as reported in Eq. (5). For maximizing the performance, arithmetic operations are implemented in DSP block resources. The TTM is necessary when the not filtered acquisition of all the timestamps generated over an acquisition time bigger than the full-scale range is requested. Furthermore, the TTM is fundamental for the identification of very complex patterns that cannot be detected by the LZT. The huge amount of data sent and stored to the PC limits the transfer rate to 1 Mmeasures/s.

The third option is the MultiHits Acquisition (MHA), which has the same structure of TTM, except for the absence of N_{TTM} (Fig. 9). The MHA acquires at the maximum rate of 20 MHz per channel all the timestamps in a user-defined window smaller than the full-scale range of the TDC IP-core (157 μs) after a trigger that substitutes the *TAG* (Fig. 10). Consequently, for performing the measurement, the components of the timestamp of the *i*th event (T_i^{COARSE} and T_i^{FINE}) are corrected by those of the trigger ($T_{TRIGGER}{}^{COARSE}$ and $T_{TRIGGER}{}^{FINE}$), i.e.,

$$T_{MHA,i} = \left(T_i^{COARSE} - T_{TRIGGER}^{COARSE}\right) + \left(T_{TRIGGER}^{FINE} - T_i^{FINE}\right). \quad (6)$$

In order to sustain the maximum rate, measures are temporarily saved in a BRAM inside the FPGA capable to store 256 values of them and transferred to the host PC after the acquisition is completed.

The MHA is a lite and faster version of the TTM used when a higher acquisition rate and a lower full-scale range are required. In this context, "acquisition efficiency" is the maximization of measuring rate and resolution. In fact, the MHA allows us to record all the timestamps produced in FPGA without transmitting them to the PC. Moreover, the use of the MHA is necessary instead of the TTM if the *SYNC* signal that stimulated the generation of the events is not perfectly periodic or correlated with the input events. However, only the time distances inside the full-scale range of the TDC are measurable.

C. Software

The software is a Windows application developed in Visual Studio and performs the storage and processing of measures from

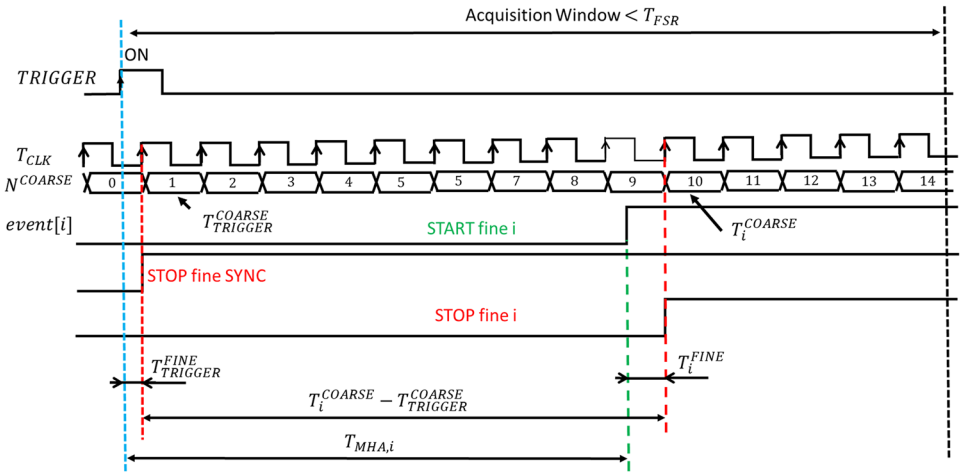

FIG. 10. Timing diagram of the MultiHit Acquisition $T_{MHA,i}$ of the *i*th event.

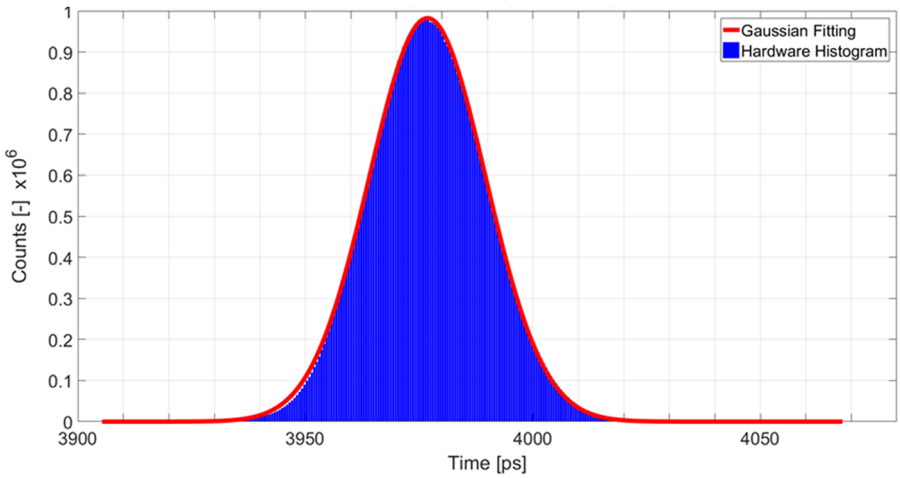

FIG. 11. Timing histogram calculated by the Hardware Histogram-Maker Module. The histogram is computed over 10^8 measures with a bin width of 2 ps (resolution, LSB). The shape of the timing statistics is Gaussian with very high confidence (R2 < 0.9996), featuring a standard deviation of 12.8 ps rms that means a channel precision of 9.1 ps rms (precision).

the FPGA. Moreover, the same application allows programming the setting of the firmware and controlling the calibration procedure.

The software is structured in the same modular way as the firmware and allows monitoring in real-time data from level-zero trigger, time-tagging module, and multihit acquisition modules and storing the selected timestamps.

Of particular relevance is the hardware histogram-maker module that calculates the histogram of timestamps in FPGA (Fig. 11). The module accepts and manages measures in the pipeline mode up to 20 Mmeasures/s, computing the corresponding histogram with a tunable bin width.

Thanks to an intuitive graphic interface, the application makes the instrument very user-friendly.

IV. SYSTEM CHARACTERIZATION

The characterization of the instrument has been carried out not only in laboratory but also in the fieldwork of several research projects.

TABLE III. Features and performance of the considered version of the instrument.

Feature	Value
Number of channels	16
TDC clock period	2.4 ns
System frequency	100 MHz
Interpolation technique	SuperWU
Device occupation per channel	3738 FFs, 7010 LUTs, 54 kbit BRAM, 1DSP48
Channel processing latency	110 ns
Maximum channel rate of measuring	20 MHz/channel
Total channel resolution (LSB)	2 ps
Total channel precision	<12.5 ps rms
Full scale range	157 μs
Maximum nonlinearity error	<4.2 ps
Power supply	5 V, 2 A
Voltage drift influence	Not detectable
Temperature drift influence	286 fs/°C without the Peltier cell
Channels cross talk	No evidence both on idle and active channels
Precision cross talk influence	<3 ps rms only on active channels
Max. timestamp transfer rate LZT	10 Mmeasures/s
Max. timestamp transfer rate TTM	1 Mmeasures/s
Time-tagging full scale-range	15 days
Max. measurements MHA	256
Input signal amplitude range	[0; 3.3] V
Minimum input pulse width	3 ns

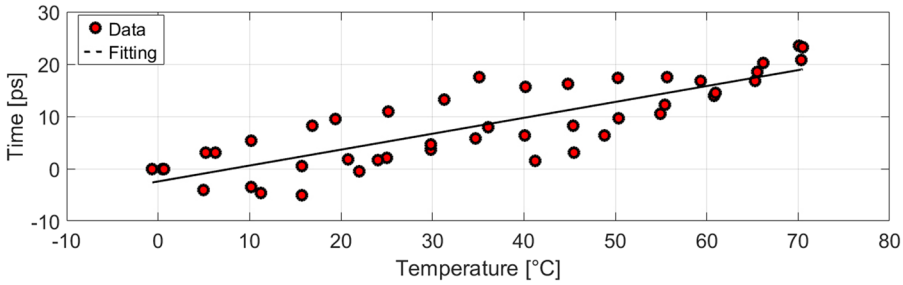

FIG. 12. Dependence on the temperature of mean values of measures of the same interval.

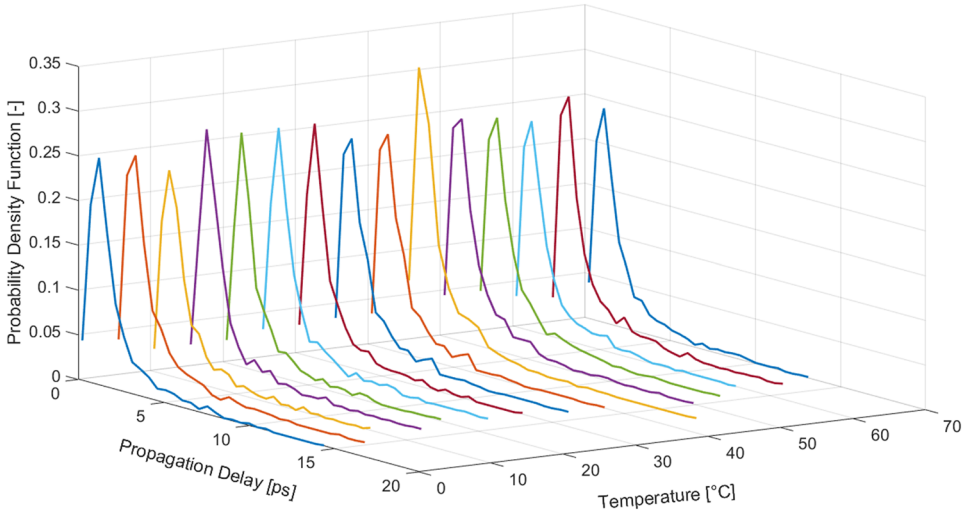

FIG. 13. Dependence on the temperature of the dispersion of the propagation delays of the bins of the V-TDL, implementing the subinterpolation based on the SuperWU algorithm.

As mentioned above, the instrument considered for this presentation is equipped with a Xilinx Artix®-7 XC7A200T-1 FPGA (33 650 SLICEs, 13 140-kbit BRAM, 740 DSPs) in the package of area 19 × 19 mm^2.[49,47]

A. Performance

Table III gives a synoptic view of the main features of the instrument from the functional point of view.

B. Temperature effects

We have specifically investigated the dependence on temperature without any thermostatic action of precision and mean value of the measures, in an extended operative range between 0 °C and 70 °C.

Over the whole range, the drift of the measurement values of the same intervals was 20 ps (286 fs/°C), which is comparable with the system precision (Fig. 12). This means that in a reasonable operative range of ±10 °C around room temperature, the thermal drift of measures is reduced to about ±2.86 ps that is negligible with respect to the system precision (<12.5 ps rms).

Experiments have put in evidence that also other characteristic parameters of the implemented subinterpolated SuperWU V-TDL are not significantly affected by temperature variations. Figure 13 shows the probability density function that describes the dispersion of the propagation delay of the 1200 virtual bins that comprise the subinterpolated SuperWU V-TDL as functions of the temperature in a range from 0 °C to 70 °C.

C. Linearity

We have experimentally verified that the worst case of integral nonlinearity of the instrument is always below 4.2 ps over 35 ns of full-scale range.

Figure 14 shows the integral nonlinearity error as a function of the time interval measured. The curve was obtained by the

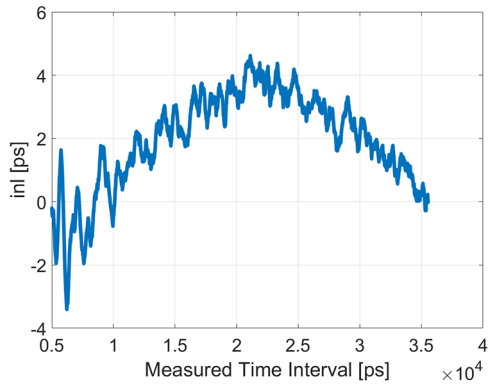

FIG. 14. Measurement of integral nonlinearity.

TABLE IV. Comparison of the most relevant figures of merit of the proposed instrument with respect to two significant ASIC solutions.

Feature	Proposed instrument	Reference 53	Reference 54
TDC channel resolution (LSB) (ps)	2	5.5	10
TDC channel precision (psrms)	<12.5	<4.95	<21.3
Full-scale range (s)	157 μs	90.1 ns	160 μs
Maximum channel rate (MHz)	20	N.A.	6.7
Number of channels	16	1	3
Technological node (nm)	28	40	350
Reconfigurability	Yes	No	

TABLE V. Comparison of the most relevant figures of merit of the proposed instrument with respect to reference commercial solutions.

Feature	Proposed	HydraHarp 400 (PicoQuant)	TimeHarp 260 PICO (PicoQuant)
Discriminator	Threshold prog. (50 μV)	CFD	CFD
Input signal amplitude (V)	[0; 3.3]	[0; 1]	[0; 1.2]
TDC channel resolution (LSB) (ps)	2	1	2
TDC channel precision (ps rms)	<12.5	<12	<20
Full-scale range (s)	157 μs	2.9	17.1
Maximum channel rate (MHz)	20	12.5	40
Number of channels	16	8	25
Channel processing latency (ns)	110	4	2
Total power consumption (W)	<10	<100	<15
Reconfigurability	Yes	No	No

integration and equalization of a density code histogram composed of 1.5×10^{10} counts normalized in picoseconds. The 1.5×10^{10} start and stop events were obtained, respectively, by a 3.33 MHz square wave and a completely uncorrelated single photon avalanche diode (SPAD) operating at the rate of 100 kHz. The low rate of the SPAD with respect to the frequency of the stop events and the big value of the counts guarantee a uniform investigation of the code density.

D. Comparison with ASIC solutions

The performance of the proposed instrument and of customized solutions implemented in specific integrated digital circuits is pretty much the same. The main advantage in our case is that the instrument is fully programmable.

Table IV compares the proposed instrument to a couple of particularly significant ASIC solutions of TDCs for different target applications, i.e., PLL[50] and measurement.[51]

Table V compares the proposed instrument to very well-known instruments at the state-of-the-art, whose TDC processing cores are implemented in ASICs.

V. APPLICATIONS

The applications for debugging, testing, and engineering the instrument in many research projects have also highlighted its extreme flexibility and reconfigurability in the most different experimental conditions.

Just to name a few of these applications, high-resolution/precision and multichannel features were fundamental in the characterization of the timing jitter of array of detectors such as Super Nanowire Simple Photon Detectors (SNSPDs),[52] Single Photon Avalanche Diode (SPAD), and Silicon Photo Multipliers (SiPMs).[53] Moreover, the high full-scale range made the instrument suitable for several kinds of experiments based on time-of-fly measures in the LHCb collaboration[54] and for electron beam tracking measures.[55] At last, an achievable high channel rate was essential in photon statistic experiments.[30]

Fundamental in several of these applications was the availability of different acquisition modes, thus fulfilling requirements of different experimental conditions and detectors used.

VI. CONCLUSIONS

A fully configurable high-performance time-resolving instrument based on subinterpolated SuperWU has been realized and tested.

The system can be configured with up to 16 channels operating in parallel with a resolution of 2 ps (intended as LSB of the timestamps), precision below 12.5 ps r.m.s, over a hardware full-scale-range of 157 μs.

The possibility of using different acquisition modes (LZT, TTM, and MHA) allows us to manage in different ways the timestamps provided by the TDC IP-core without reducing resolution and precision.

In particular, the level-zero trigger module makes possible to filter all the timestamps in real-time, sustaining a total transfer rate of 10 Mmeasures/s shared among the channels. Thanks to a time-tagging module, the extension of the full-scale range to some days is feasible simply operating via software. Moreover, a MultiHit Acquisition module allows storing 256 measures at the maximum rate of 20 MHz per each channel.

The firmware and the software of the instrument are modularly structured, meaning that each module has firmware and software images that split the processing in parallel and temporal segments.

By changing the plugged-in processing module, the instrument can be reconfigured also in its hardware structure.

The instrument has been characterized in temperature without any thermostatic action in an operative range from 0 °C to 70 °C, showing only a drift of 286 fs/°C of the mean value of the measures. At last, the instrument guarantees linearity error below 4.2 ps over 35 ns of dynamic range.

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