Multilayered Ge/SiGe Material in Microfabricated Thermoelectric Modules

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INTRODUCTION

The efficiency of a thermoelectric material is evaluated by measuring the figure of merit $ZT = \alpha^2\sigma T/\kappa$, where α is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature and κ is the thermal conductivity. Commercial thermoelectric modules are still dominated by bulk bismuth telluride (Bi_2Te_3) alloys below 100°C and lead telluride (PbTe) is still one of the best performance thermoelectrics for applications between 200°C and 500°C.[1] Tellurium, however, is rare and unsustainable and lead has been banned from consumer devices due to its toxicity. Hence, there is substantial interest in finding suitable alternatives for these materials.

The thermoelectric properties of the main commercial microelectronic semiconductors such as Si, Ge and $Si_{1-x}Ge_x$ are poor close to room temperature compared to Bi_2Te_3 generators and Peltier coolers.[1] $Si_{1-x}Ge_x$ alloys have been used for radioisotope thermoelectric generators by NASA due to the high ZTs at temperatures above 500°C.[1] However, the presence of low dimensional structure, such as quantum wells, quantum wires or quantum dots, can improve the thermoelectric performances of a material at room temperature.[2,3] This is due to enhancements of both α, through larger asymmetry in the density of states around the chemical potential,[4,5] and σ, from reduced ionised impurity scattering.[3] κ is reduced as result of higher phonon scattering rates at heterointerfaces.[1] Mature Si/SiGe and Ge/SiGe heteroepitaxial growth technology potentially allows engineered thermoelectric materials[6] that would be compatible and integrable with CMOS and Si photonics circuits.[7]

We have previously demonstrated lateral Hall bar devices with integrated heaters and thermometers that can measure the value of ZT for lateral transport in heterostructures, and additional test structures to estimate the contribution of any thermal parasitic channel.[8,9] In this paper, we demonstrate a set of test structures with a similar type of

approach to allow ZT to be obtained for vertical transport in heterostructure, i.e. where the electrical and thermal transport is perpendicular to the heterostructure interfaces.

SAMPLE PREPARATION

Four-micrometer Ge/SiGe superlattice structures have been grown by low-energy plasma-enhanced chemical vapour deposition (LEPECVD)[10] on 100-mm-diameter Si wafers. p-type superlattices doped with boron at $2.0 \times 10^{18}\,\mathrm{cm}^{-2}$ with 922 repeats of $2.85 \pm 0.85\,\mathrm{nm}$ Ge quantum wells (QWs) with $1.12 \pm 0.14\,\mathrm{nm}$ $Si_{0.5}Ge_{0.5}$ barriers were grown strain symmetrised to $Si_{0.7}Ge_{0.3}$ virtual substrates.[6] High resolution x-ray diffraction (XRD) and scanning transmission electron microscopy (STEM) were used to characterise both the Si and Ge content inside the superlattice and to precisely measure the layer thickness of each barrier and QW.[8,10] Both techniques agreed with a difference of less than 3%. This difference is within the error of measurement and inside the specification of growth. Such deviation is not expected to create any impact on the final value of the calculated ZT. Figure 1 shows a STEM image of one of the analysed sample.

The Ge/SiGe test structures were patterned using conventional photolithography and low damage reactive ion etch methods.[11] To characterise the cross-plane electrical conductivity, we used an approach similar to the one reported in,[12–14] but implemented with circular TLM structures[15,16] (Fig. 2) to increase the accuracy of the measurements.[17] Lift off of Ni and a successive annealing at 340°C allowed the formation of NiGe Ohmic contacts.[15] The values of the four-terminal resistances shown in Fig. 2b were measured for different etching depths and gap spacing. The total measured resistance (R_{TOT}) is the contribution of the contact resistance (R_c), the vertical superlattice resistance (R_{SL}) and the lateral superlattice contribution (R_L), its value is equal to: $R_{TOT} = 2R_c + 2R_{SL} + R_L$. For a zero gap spacing the contribution of the lateral conduction is zero: $R_{TOT} = 2R_c + 2R_{SL}$. By plotting these calculated values versus the etch depth, it is possible to extract both the value of R_c, as the intercept of the fitted line with the vertical axis in Fig. 2c, and the value of electrical conductivity as the gradient of the fitted line scaled by the geometrical dimensions of the device. This process has been implemented in the analysis of several designs.[16] A value for σ of $8630 \pm 910\,\mathrm{S/m}$ was obtained for a 3.48 nm p-Ge quantum well and 1.5 nm p-SiGe barrier shown in Fig. 2c. The second test structure to measure α and κ involved a mesa structure with thermometers consisting of a metal bilayer of Ti/Pd (20/80 nm) patterned at the top and bottom of the structure and a NiCr heater 33 nm thick patterned on the top surface (Fig. 3). Silicon nitride layers, 50 nm thick, deposited by plasma-enhanced chemical vapour deposition (PECVD), were used to provide electrical insulation between the heater, the thermometer and the Ohmic contacts. No electrical and thermal connections are present between the top and the bottom of the mesa structure, to prevent heat and current leakage. Moreover, to minimise errors due to the lateral contributions, self-aligned techniques were used for both thermometers and electrical contact pads.

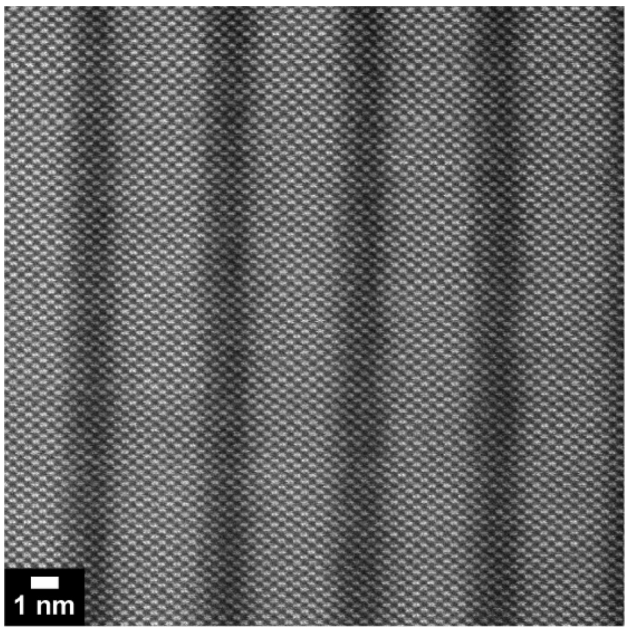

Fig. 1. A STEM image of a $3.43 \pm 0.12\,\mathrm{nm}$ p-Ge QW (XRD 3.54 nm) and $1.12 \pm 0.14\,\mathrm{nm}$ (XRD 1.66 nm) of p-$Si_{0.5}Ge_{0.5}$ barrier. Both measurements are within the specification of design. By analysing the electrical, thermal and Seebeck measurements for different structures, it is possible to correlate the impact of the QW and barrier thicknesses on the figure of merit ZT, as further illustrated in.[16]

SAMPLE CHARACTERISATION

The sample was mounted on a metal plate to create a heat sink on the back of the wafer. When a DC voltage was applied to the NiCr heater, a temperature gradient was established across the heterostructure. The calibrated Ti/Pd thermometers[18] were used to measure the relative temperature difference across the superlattice for a range of applied powers.

Thermal measurements are problematic because any physical connection to the required thermometers and heaters produces parasitic heat channels that impair the accuracy of the measurements. Even assuming a unidimensional heat conduction (the ratio of the heater width and material thickness being 10:1), due to the large thermal conductivity of the metal layers and the lateral thermal conductivity of the superlattices,[8] lateral heat spreading is present in the structure as depicted in Fig. 4c. A second test structure was developed to measure this contribution and modelling was then used to subtract this contribution to improve the estimation of κ[8,18] Fig. 4b.

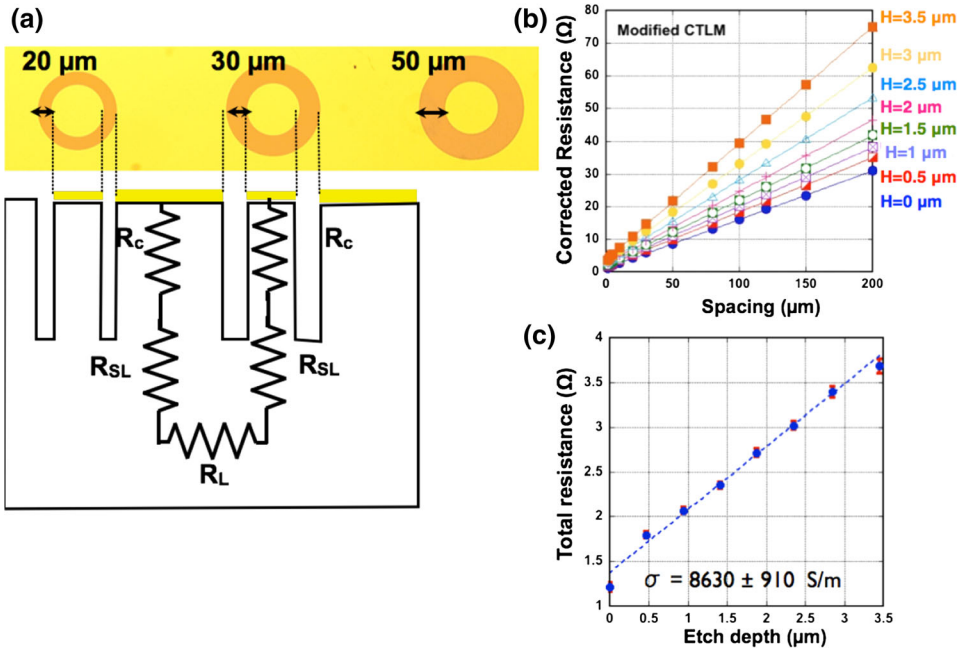

Fig. 2. (a) An optical picture of the device test structure used to characterise cross plane electrical conductivity of the superlattice material under test. (b) Measured resistance for different gap spacing. (c) Superlattice resistance versus the etching depth.

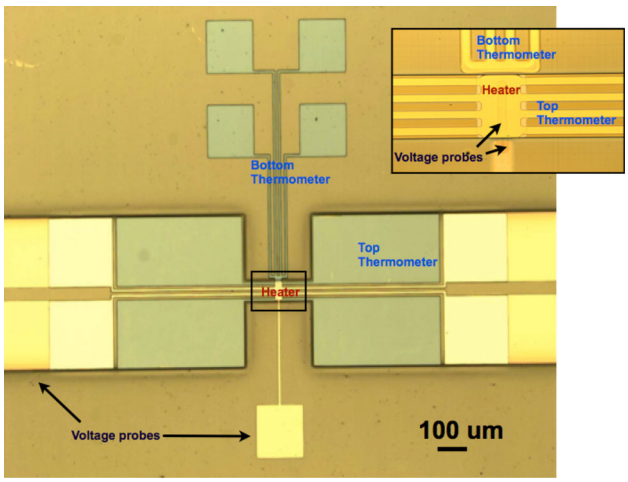

Fig. 3. An optical picture of the device test structure used to characterise α and κ of the superlattice material under test. The inset presents a detailed picture of the two thermometers with the heater and voltage probes used to measure α.

The second test structure consisted of a geometry similar to the full structure but with electrical interconnects and the superlattice material on only half the structure. The difference in the measured temperature profiles between these two structures for the same level of applied power gives information on the lateral thermal conduction and the parasitic heat flow. Twice the parasitic thermal contribution must be subtracted to obtain the correct cross-plane (vertical) value of κ. The accuracy of this technique was evaluated by measuring the thermal conductivity of reference samples made of PECVD SiO_2 and Si_3N_4 along with bulk Si and comparing the extracted data with literature values. Measured mean values were within 10% of literature values.[16]

Figure 5 provides the experimental data of the measurements of temperature for the full and half devices as a function of the heater power. The temperatures detected from the bottom thermometers are the same for the full device (cyan triangles) and half device (blue circles). This suggests a thermal equilibrium regime due to the heat sink provided by the substrate. When analysing the temperature of the top thermometer for the full (red squares) and the half structure (orange diamonds), it can be observed that for the same level of power, the local temperature of the half structure is higher. This is due to the reduction of the parasitic heat leakage through the lateral superlattice but predominantly from the metal interconnects to the heater and thermometer on the top of the device. From a linear fit to the data, it was found that only 41% of the total applied power is able to conduct vertically inside the vertical superlattice structure. The rest is loss by conduction through the metal contacts and lateral conduction along the superlattice QWs. To extract the value of κ, Eq. 1 is used, where P_{eff} is the effective power inside the structure, t is the superlattice thickness and A is the effective area of the heat flux.

$$\kappa = \frac{P_{\text{eff}} t}{A \Delta T} \tag{1}$$

To calculate the Seebeck coefficient of the material $(\Delta V/\Delta T)$, the voltage was measured across the

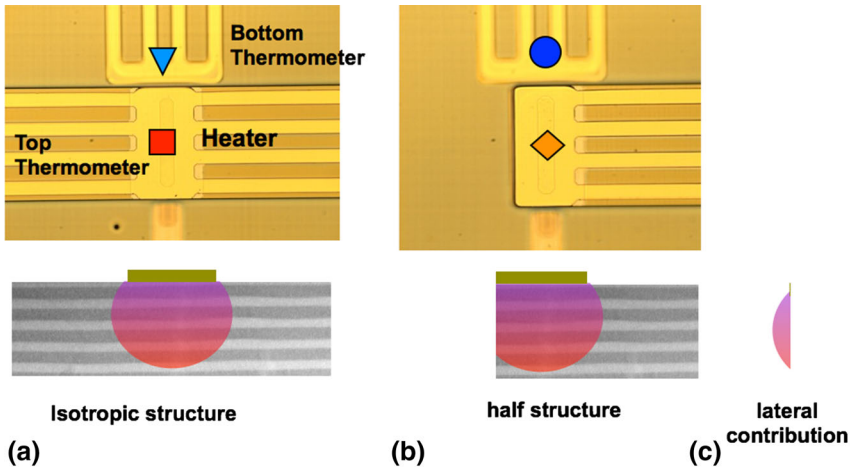

Fig. 4. The thermometers on the top and bottom of the full (a) and half devices (b) and the parasitic lateral contribution (c). A differential method has been developed to estimated the power lost through the parasitic channels and to estimate the effective heat flux travelling inside the structure.

superlattice, at the same time the temperatures were monitored at the thermometer sections for different applied powers to the heater. The gradient of the curve in Fig. 5 was used to obtain the relative Seebeck coefficient. The absolute value of the Seebeck coefficient for the p-Ge/SiGe material under analysis was obtained by removing the Ni (-15μV/K) contribution for each of the contacts. Additionally, finite element simulations were used to investigate the error in the estimation of the Seebeck coefficient when measuring the temperature at the thermometer sections 50 nm from the voltage probes section. Even if a drop of temperature is present, this value is negligible and within the measurement errors quoted.

A value of κ of 5.1 ± 0.4 W/mK and α of $394 \pm 6\mu$V/K were measured for the p-Ge/SiGe cross-plane device under analysis. To reduce the uncertainty, each of the measurements were acquired with lock-in amplifiers. Each point in Fig. 5 is the mean of 100 repetitions of the measured data for a fixed applied power. A ZT of 0.08 ± 0.011 and a PF of 1.34 ± 0.15 m Wm^{-1}K^{-2} at 300 K was extracted for the material under analysis. Results obtained for structures with different quantum well widths are reported in.[16]

MODULE DEVICE

For a complete thermoelectric module, n- and p-type legs connected electrically in series and thermally in parallel are required (Fig. 6a). The output power of a generator with N legs of area A and length L is:

$$P = \frac{\alpha^2 \sigma A N \Delta T}{2(\rho_c \sigma + L)\left(1 + 2\frac{\kappa l_c}{\kappa_c L}\right)^2} \qquad (2)$$

where the specific contact resistivity of the electrical contacts is ρ_c, the thermal conductivity of the contacts is κ_c and the length of the contacts is l_c. Similar to the Micropelt approach,[19] the final generator was assembled by indium bump bonding with a flip chip bonding process of two individually microfabricated p- and n-type samples. Each sample consisted in series of interdigitated legs μ m thick and an area of 500×500 square as shown in Fig. 6b. The measured specific contact resistivity of the NiGe contacts was low, with R_c values below $10^{-8}\Omega$ cm^2.[15] This is one order of magnitude smaller than what is currently available for Bi_2Te_3 contacts, which constitute a reduction of the losses in Eq. 2. Figure 6d demonstrates the preliminary results of a power extracted from the device by applying a temperature gradient between the hot and the cold side.

Figure 6c presents the measurement setup where the temperatures at the hot and the cold sections were controlled by standard thermocouples. The measured output power is still relatively low and some optimisation is required to enhance these values. Firstly, to reduce the thermal losses inside the substrate, the wafers need to be thinned. Secondly, the presence of a silicon dioxide buffer layer under the thermoelectric material under test would eliminate any leakage currents in the system. Moreover, the performance of the entire system is also affected from the thermal and electrical impedance matching between the n- and p-type leg as well as the load. The physical area dimension for the p-type and n-type legs must be scaled according to Eq. 3 in order to balance the current inside the circuit and remove any Peltier effect at the thermocouple junctions.[20] To obtain a maximum output power, the module requires the following design parameters to be met:

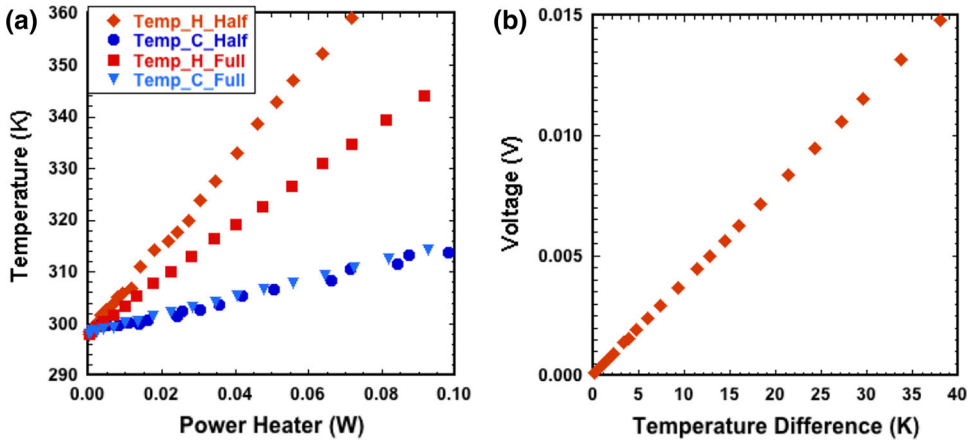

Fig. 5. (a) The temperature dependance versus heater power for a full and half device. The difference of power required for a defined temperature between the hot thermometers allows the parasitic power loss to be estimated. (b) The thermal generated voltage as a function of the temperature difference for the hot and cold sides for the full device structure. The gradient of this curve is the relative Seebeck coefficient.

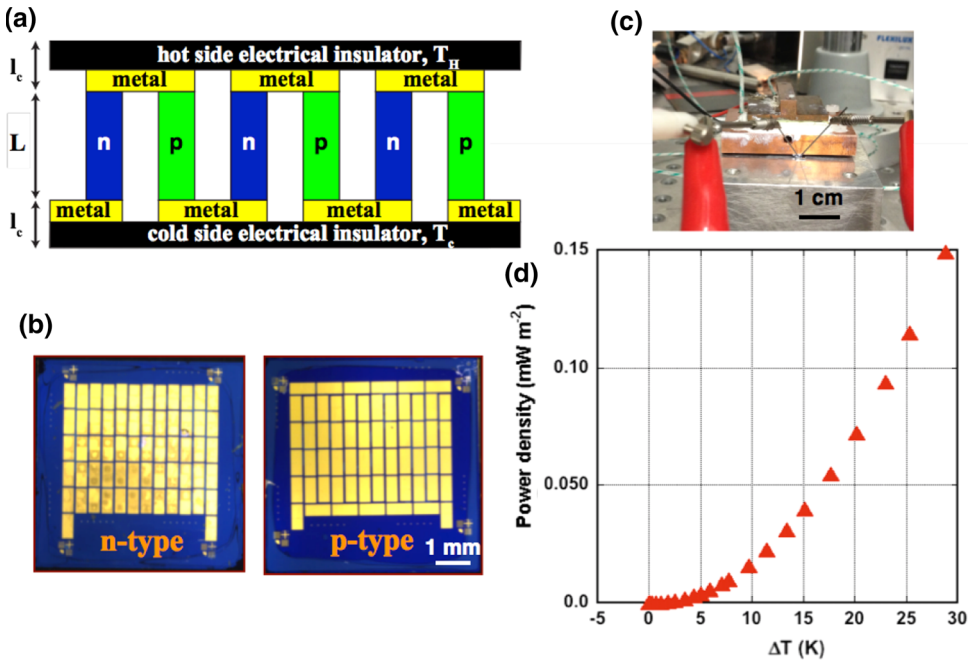

Fig. 6. (a) A schematic diagram of the *n*- and *p*-type legs after bonding. (b) *n*- and *p*-type samples with interdigitated legs before the bonding process. (c) The characterisation setup for the determination of the power output. (d) The output power obtained for an initial un-optimised module.

$$\frac{L_{\mathrm{n}}A_p}{L_{\mathrm{p}}A_{\mathrm{n}}} = \sqrt{\frac{\sigma_{\mathrm{n}}\kappa_{\mathrm{n}}}{\sigma_{\mathrm{p}}\kappa_{\mathrm{p}}}} \qquad (3)$$

By applying all these optimisations, improved performance is predicted.

CONCLUSIONS

Ge quantum well superlattices have been designed and characterised producing a ZT of 0.08 ± 0.011 and PF of $1.34 \pm 0.15\,\mathrm{mWm^{-1}K^{-2}}$ at 300 K. A bump-bonding process has been developed to allow *n*- and *p*-type microfabricated legs to be flip chip bonded together to produce complete microfabricated Ge/SiGe thermoelectric generators. The initial results have suffered from electrical leakage and poor thermal impedance matching but routes to improvement including electrical isolation from the substrate, balancing the current by scaling the leg areas and thinning the substrates to improve the thermal contacting are proposed.

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