Voltage Regulators Design Through Advanced Mixed-Mode Circuit Simulation

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I. Introduction

DESIGNERS of switching power suppliers typically *approximate* their behavior by subdividing one working cycle in various sequential phases/subtopologies and apply *specific* and *simplified* techniques to each phase to grasp the main features of the overall dynamics. This approach is justified by the fact that often MOSFETs and diodes are the unique nonlinear elements and the original nonlinear circuit reduces to a linear time varying one by modeling them as ideal switches. Subdivision is reasonable if the converter has a simple schematic/structure and the control strategy can be described by a limited number of combinatorial functions and state machines. Each linear subtopology is thus solved by pen and paper. In these cases, the entire system can be modeled by a differential algebraic equation (DAE) with switching vector field and/or algebraic constraints and with possibly discontinuous (digital) state variables. As shown in previous works (see for example [1]–[4] and references therein), this approach allows to describe a complete working cycle of the converter (and study its stability) by exploiting the product of constant fundamental matrices, one for each subtopology that the converter assumes.

We present here a *general* and fully automatic simulation method, based on an extension of the state transition matrix, allowing 1) to accurately and efficiently compute the periodic steady-state solution of switching power suppliers described by complex topologies (*without substituting nonlinear elements with simplified linear ones*) through the shooting (SH) method, 2) to study the stability of the steady state, 3) to determine time-varying transfer functions (e.g., the input/output one) through the periodic linear phasor (PAC) analysis, and 4) to evaluate the performances of the chosen controller.[1]

To describe the proposed approach, the design of a voltage regulator module (VRM) supplying modern computers is used as a test vehicle. This peculiar choice is driven by the extremely large market of computers, and thus of VRMs, triggering a large interest in finding new solutions lowering cost.

The increasing integration of transistors in a chip directly impacts on the supply current that can be greater than 100 A with peaks above 150 A. In nowadays microprocessors, the extremely low value of supply voltage (about 1.0 V), makes very narrow (about 130 mV) the interval inside which this voltage is allowed to vary when there is a fast step in the requested power. The large supply current heavily burdens the transient response since load current swings of 100 A (with slew rates of 300 $A\mu s^{-1}$) must be correctly handled [7]. These targets can be reached by using a very large output capacitance but this increases size and cost. Given a control strategy, our design target is to select the minimum capacitance value that ensures the desired performance and obviously the stability of the VRM. To achieve this goal, the adaptive voltage position (AVP) approach [8] is exploited. If the transient dynamics is characterized by the absence of spikes and oscillations, the AVP design is optimal. The AVP can be accomplished in a straightforward way when the VRM acts as an independent voltage source connected in series to a resistor. The constant resistive output impedance design for the VRM thus leads to an optimal solution for load transients [9]. PAC analysis is a promising tool to this kind of design and its extension to switching power suppliers is extremely valuable.

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[1] In the following, we refer to the conventional shooting (SH) and periodic linear phasor (PAC) analyses providing no details on them since they are widely discussed in the literature (e.g., [5], [6]).

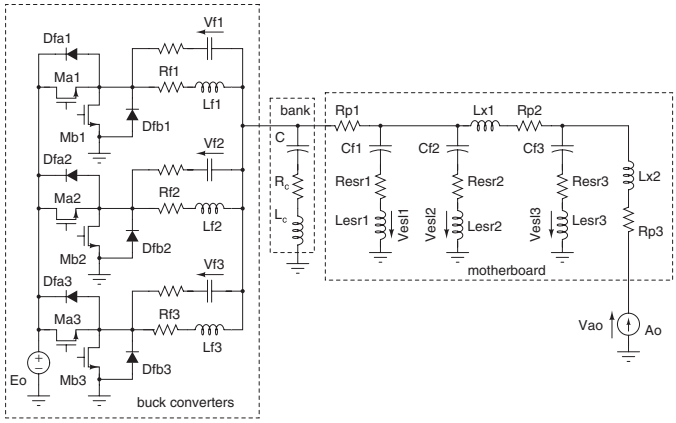

Fig. 1. Schematic of the VRM and the lumped model of the motherboard. $L_{f\,1} = L_{f\,2} = L_{f\,3} = 280$ nH, $R_{f\,1} = R_{f\,2} = R_{f\,3} = 1$ mΩ. The equivalent CR_cL_c series circuit represents a bank of B identical capacitors connected in parallel (each capacitor of 470 μF has 5 mΩ equivalent series resistance (ESR) and a series inductance of 2 nH). The values of the components enclosed in the motherboard block are reported in [7]. The switching frequency is 200 kHz.

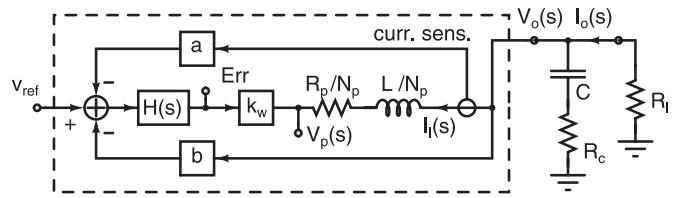

Fig. 2. Simplified linear block schematic of the dc/dc converter. The PI controller is described by $H(s) = k_i/s + k_p$ being k_i and k_p real constant parameters. The a, b, and k_w blocks model the gain in sensing the $I_l(s)$ current flowing in the L inductor, the $V_o(s)$ output voltage across the load and the gain of the PWM modulator whose output voltage is $V_p(s)$. The v_{ref} input voltage sets the value of the VRM output voltage.

II. VRM Control Loop Design

The schematic of a buck converter implementing a version of a VRM and a lumped model of the motherboard [7][2] is shown in Fig. 1. We chose the N_p number of phases equal to 3; it depends on the load current requirements and is a tradeoff between cost and performances.

As a gross simplification helping in first dimensioning the elements of the VRM, the block schematic circuit reported in Fig. 2 implements the equivalent linear time-invariant model of the main voltage section of the controller that acts on the circuit shown in Fig. 1. The controller includes also a current sharing block not shown in Fig. 2. The limit of the validity of this approximation will be verified by exploiting the proposed simulation approach. The analytical approach to obtain a purely real R_l impedance "seen" by the load considers the parallel connection of the impedances of the converter and of the output bank of capacitors. These capacitors are connected in parallel and are modeled for simplicity by C in Fig. 2; the corresponding overall equivalent series resistance (ESR) is modeled

[2]Lumped model of the motherboard is characterized by the $L_{x\,1}$, $L_{x\,2}$, and $L_{\mathrm{esr}\,3}$ cutset of inductors leading to and index 2-DAE. This causes troubles to the modified nodal analysis formulation used in almost all circuit simulators. The cutset can be removed by substituting, for example, L_{x2} by a proper voltage-controlled voltage generator.

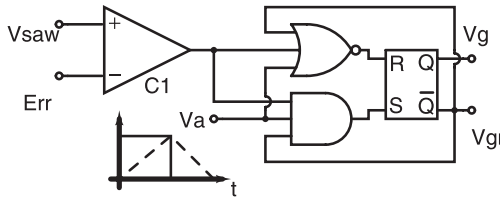

Fig. 3. Schematic of the circuit generating the gate signal of the switching MOSFETs of a single phase of the VRM. The E_{rr} input terminal reads the signal at the output of the PI block shown in Fig. 2, i.e., across the CPU; the V_{saw} sawtooth waveform (dashed line) is compared with E_{rr} by the C_1 comparator that generates a square wave with a proper duty cycle. The V_a input reads the 50% duty-cycle square waveform (solid line) synchronous with the sawtooth one. The V_g gate signal is triggered when E_{rr} becomes lower than V_{saw} with V_a high and reset when both V_a and the comparator output are low. The FLIP-FLOP limits the generation of one and only one V_g gate triggering signal per working cycle of the VRM. The V_{saw} waveform and the corresponding square waveform are shifted by $T_{\mathrm{saw}}/3$ among the three phases of the VRM.

by R_c and the L_c parasitic equivalent inductance is neglected. By choosing $R_c = R_l$ (i.e., the desired impedance will match that of the capacitors bank), the relation governing the constant output impedance is

$$\underbrace{\frac{sC}{1+sCR_l}}_{G_b(s)} + \underbrace{\frac{I_l(s)}{V_o(s)}}_{G_c(s)} = \frac{1}{R_l} = \frac{I_o(s)}{V_o(s)} \tag{1}$$

where $G_b(s)$ and $G_c(s)$ represent the admittance of the board capacitors and of the converter, respectively. By exploiting the relations among the electrical variables involved in the linear time-invariant model shown in Fig. 2, we have

$$\begin{aligned} I_l(s)(sL + R_p)N_p^{-1} &= V_o(s) - V_p(s) \\ V_p(s) &= -H(s)\left(I_l(s)a + bV_o(s)\right)k_w \end{aligned} \tag{2}$$

and one can derive

$$G_c(s) = \frac{1}{R_l}\frac{1 + s\dfrac{1 + k_p k_w b}{k_i k_w b}}{s^2\dfrac{L}{k_w R_l k_i N_p b} + s\dfrac{R_p - N_p k_w k_p a}{N_p k_w R_l k_i b} - \dfrac{a}{R_l b}}. \tag{3}$$

It is then possible to obtain a constant output impedance of the VRM by choosing

$$a = -R_l, b = 1, k_p = \frac{L - CR_l^2 N_p}{k_w CR_l^2 N_p}, k_i = \frac{R_p - R_l N_p}{k_w CR_l^2 N_p} \tag{4}$$

determining thus the controller parameters yielding the AVP. It is worth noting that the controller admittance is far from (3) also because of sampling effect, limited slew rate of the inductor current, and possible nonlinearities of control block (such as for example saturations).

The design is completed by the schematic of the digital circuit generating the driving signals of a single phase of the VRM (see Fig. 3). The three instances of this circuit are modeled as digital blocks through the VERILOG-RTL hardware description language and constitute the *digital part* of the converter model.

III. Proposed Method

The general model of a converter can be written as[3]

$$\begin{cases} \dot{x} + f(x, y, r, w, t) = 0 \\ \dot{r} = 0 \\ g(x, y) = 0 \\ c(w, r) = 0 \end{cases} \tag{5}$$

where $x(t) : \mathbb{R} \to \mathbb{R}^N$ and $y(t) : \mathbb{R} \to \mathbb{R}^M$ represent the time evolution of differential and algebraic variables, respectively, linked by $g(x, y) : \mathbb{R}^{N+M} \to \mathbb{R}^M$, $r(t) : \mathbb{R} \to \{0, 1\}^R$ represent single bits stored in digital state variables (R binary registers) linked to the $w(t) : \mathbb{R} \to \{0, 1\}^C$ combinatorial digital variables by $c(w, r) : \{0, 1\}^{R+C} \to \{0, 1\}^C$, $f(x, y, r, w, t) : \mathbb{R}^{N+M+R+C+1} \to \mathbb{R}^N$ is the vector field switching according to the values assumed by r, w, and possibly y.

From (5), the digital state variables seem to be static and this is in general true a part from a finite set of time instants where the r variables abruptly change their values. These *digital* events can be monitored by a proper set of H $(N + M)$-dimensional manifolds $h(x, y, t) = 0$, where $h(x, y, t) : \mathbb{R}^{N+M+1} \to \mathbb{R}^H$. When a trajectory in the state space hits one of the H manifolds [say $h_j(x, y, t) = 0$] at $t = t_1$, $r_-(t_1)$ (i.e., $r(t_1)$ immediately before the event) is instantaneously mapped in $r_+(t_1) = B_j(x(t_1), y(t_1), r_-(t_1), w_-(t_1))$, where B_j (for $j = 1, \ldots, H$) are reset functions.

In our case, by referring to Fig. 3, we can identify three manifolds introduced by the three C_1 comparators (one per phase). These manifolds are *automatically* defined by considering the VERILOG-RTL description of the digital circuit[4] and are selected according to the state of the FLIP-FLOP.

If we want to efficiently compute the steady-state solution of (5) by the SH method and then perform a PAC analysis to derive any periodic time varying transfer function of the VRM, the system fundamental matrix must be accurately computed [10]–[12]. This can be done in a conventional way between to subsequent *digital* events, but it is not straightforward at discontinuities of the digital variables inducing switching in the f vector field.

A. Variational Model

To evaluate the fundamental matrix of a hybrid dynamical system as (5), exhibiting discontinuities in the vector field and/or in the state variables, the *saltation matrix* operator must be used [13]. To understand how this linear operator is defined and how it must be used, in the following we assume that (5) reduces to an ordinary differential equation and that no combinatorial variables are involved.[5]

[3] In (5), the initial conditions are not specified.

[4] One can adopt also more accurate descriptions of this class of analog/digital (A2D) circuits. We assumed that $V_{\rm saw}$, E_{rr}, and V_a are analog but one can resort to A2D converters to properly quantize these voltages. Of course this implies larger H. Nevertheless, even in this case, we have expanded the VERILOGA language and exploited the fact that the A2D converters linking the analog and digital parts of the circuit change their output codes any time the input voltages cross predefined thresholds which define the manifolds.

[5] Complete description of the DAE case can be found in [10].

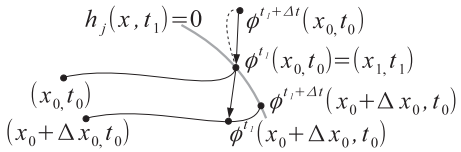

Fig. 4. Example of a trajectory hitting a manifold.

Consider the reference trajectory shown in Fig. 4 that, starting from x_0 at $t = t_0$, hits the $h_j(x, t) = 0$ time-varying manifold at x_1 for $t = t_1$. This manifold divides the state space in two regions where the dynamics is ruled by two different vector fields, say $f(x, r_-)$ and $f(x, r_+)$ on the left and on the right of the manifold, respectively. By perturbing the initial point by Δx_0, the perturbed trajectory hits the manifold at $\phi^{t_1+\Delta t}(x_0 + \Delta x_0, t_0)$ with the Δt time delay. In Δt, the reference trajectory evolves from x_1 to $\phi^{t_1+\Delta t}(x_0, t_0)$. We are interested in deriving the $\mathbf{S} \in \mathbb{R}^{N\times N}$ matrix such that, at first order $\phi^{t_1+\Delta t}(x_0 + \Delta x_0, t_0) - \phi^{t_1+\Delta t}(x_0, t_0) = \Delta x_+ = \mathbf{S}\Delta x_- = \mathbf{S}\left[\phi^{t_1}(x_0 + \Delta x_0, t_0) - (x_1, t_1)\right]$. In the literature, $\mathbf{S}$ is referred to as *saltation* matrix. If one is interested in evaluating the $\mathbf{\Phi}$ fundamental matrix of the system from x_0 to $\phi^{t_1+\Delta t}(x_0, t_0)$, $\mathbf{S}$ is necessary to match $\mathbf{\Phi}$ at the discontinuity boundary (where the Jacobian of the vector field is not defined), i.e., $\mathbf{\Phi}(\phi^{t_1+\Delta t}(x_0, t_0), x_0) = \mathbf{\Phi}(\phi^{t_1+\Delta t}(x_0, t_0), x_1)\mathbf{S}\mathbf{\Phi}(x_1, x_0)$. The derivation of $\mathbf{S}$ (see [13]), which is defined provided that the reference trajectory hits the manifold transversally, reads

$$\mathbf{S} = I_N + \frac{\left[f(x_1, r_+, t_1) - f(x_1, r_-, t_1)\right] {\eta_j}_x^{\mathrm{T}}}{{\eta_j}_x^{\mathrm{T}} f(x_1, r_-, t_1) + \eta_{j_t}} \tag{6}$$

where

$${\eta_j}_x^{\mathrm{T}} = \nabla_x h_j(x, t)|_{x_1, t_1} \text{ and } {\eta_j}_t^{\mathrm{T}} = \left.\frac{\partial h_j(x, t)}{\partial t}\right|_{x_1, t_1}.$$

IV. Numerical Results

We first perform a steady-state simulation with a bank composed of $B = 20$ capacitors and A_o generating a square waveform at 10 kHz $= \frac{1}{100\,\mu\mathrm{s}} = {T_o}^{-1}$ with amplitude as detailed in Section I. The frequency of $V_{\rm saw}$, i.e., of a single phase of the VRM, is 200 kHz $= \frac{1}{5\,\mu\mathrm{s}} = {T_{\rm saw}}^{-1}$, and it varies from 0 to 1 V. The main steady-state T_o-periodic waveforms are shown in Fig. 5. As it can be seen, the result is good since V_o shows an overshot of 10 mV and no undershoot. The maximum voltage swing is $V_o = 35$ mV at the VRM output and $V_{Ao} = 120$ mV across A_o (CPU land). This is coherent since the bank ESR is $250\,\mu\Omega$ and at low frequency the motherboard is characterized by $R_m = 800\,\mu\Omega$ total resistance. We remark that the output voltage of the PI block is upper limited at about 1 V and lower limited at about 0 V. During the falling fronts of the A_o current, the PI output saturates; in this condition, the gain of the block falls to 0 and this impacts on the fundamental matrix and on the Floquet multipliers. This makes also very difficult to analyze the VRM with a simplified pen-and-paper approach. We compute the $\mu_1 = 0.2637$, $\mu_2 = 0.0055 \pm 0.0099\,\mathrm{i}$ main Floquet multipliers (those with significant modulus, the order of the circuit model is well above 3) of the T_o-periodic steady-state solution; they are well inside the unit circle in the complex plane and thus the VRM is stable.

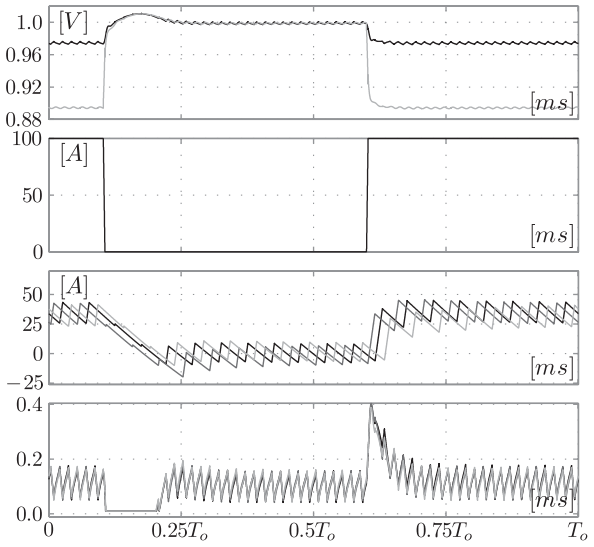

Fig. 5. T_o-periodic steady-state solution computed with a bank of $B = 20$ capacitors. From the upper panel to the lower one: the voltage across the capacitor bank (black trace) and the voltage across A_o, i.e., CPU land (gray trace); the A_o current; the currents through the L_{f1}, L_{f2}, and L_{f3} inductors (from black to light gray); the duty cycles of the three phases.

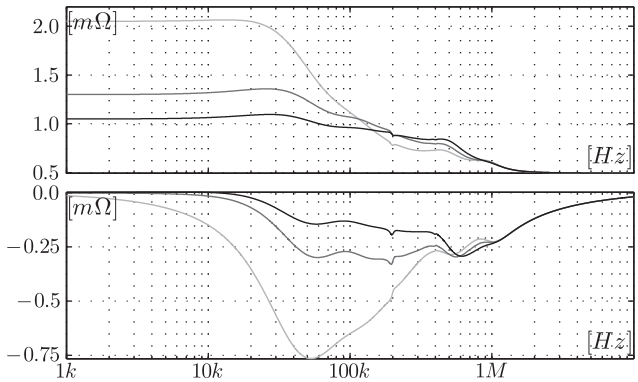

Fig. 6. Real (upper panel) and imaginary (lower panel) parts of $R_{Ao}(f) = V_{Ao}(f)/A_o(f)$. From black to light gray $B = 20, 10, 4$ (number of capacitors). Even if the VRM is stable for all of these B values, its performances reduce in term of the controller capabilities to yield the AVP.

We compute the $R_{Ao}(f)$ impedance "seen" by A_o through the PAC analysis [6], [14] according to what reported in [7]. $R_{Ao}(f)$ can be considered as the periodic time-varying transfer function between the current injected by A_o and the variation of the $\mathtt{V}_{Ao}$ voltage (CPU land). This result is shown in Fig. 6; the real part of $R_{Ao}(f)$ is almost perfectly equal to the sum of R_c and R_m till about 10 kHz; in this frequency range, the imaginary part of $R_{Ao}(f)$ is almost null.

Since the target of our design is to minimize the capacitor bank ensuring stability, we removed one by one the capacitors till one of the Floquet multipliers exits the unit circle.[6] For the considered values and number of capacitors constituting the bank, k_p and k_i are updated according to (4). This exit happens when the number of capacitors is reduced from $B = 4$ to $B = 3$ when μ_1 is equal to 1.1925 [15], i.e., the T_o-periodic steady-state solution observed for $B = 3$ is unstable. This value, i.e., the stability border of the VRM, deeply depends on the implemented digital control schema. We computed the $R_{Ao}(f)$ for $B = 4$ (see Fig. 6). We easily see that even though the VRM is stable, the quality of $R_{Ao}(f)$ is unacceptable (too high value [7]). In other words, even before reaching the stability boundary, the performances of the VRM reduce in term of the controller capabilities to yield the AVP.

[6]SH analyses were performed in tens of seconds on a DELL6600 computer running LINUX; the PAC ones were performed in ≈ 2.5 s. The circuit simulator PAN, developed by the authors, has been used and it is available at the URL: http://brambilla.ws.dei.polimi.it.

V. Conclusion

We exploited an extension to hybrid dynamical systems of both the conventional SH method and the PAC analysis to enhance the design of a VRM. We have shown that the main characteristics of the VRM such as its stability and periodic transfer functions can be directly and efficiently derived. This allowed to estimate the performances of the controller in yielding the AVP as a function of the circuit design parameters. The extended methods have general validity and in principle can be applied to any circuit modeled through a hybrid DAE.

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