Electrical Conductivity Discontinuity at Melt in Phase Change Memory

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I. Introduction

ELECTRICAL and thermal conductivities of the phase change alloy are key parameters of Phase Change Memory (PCM) cells. They directly affect joule heating efficiency and thermal confinement of PCM architectures [1] and must be properly included within modeling tools supporting device development and optimization. Their values depend on material phase and temperature [2]–[6], and feature a steep rise at melt [7], [8]. However, no clear evidence of this effect has been pointed out so far on PCM cells. In this work, through an accurate inspection of the experimental I-V curves collected on 45-nm PCM cells with *"Wall"* architecture [9] a clear conductance peak at melting is highlighted. The experimental evidence confirms the conductance discontinuity at melt and favorably compares with the results of a 3D numerical device simulator including a conductivity model tailored to match the available experimental data.

II. Experimental Evidence

Extensive wafer level characterizations were performed on 45-nm *"Wall"* devices with the structure reported on Fig. 1a. In this architecture, the phase change volume is defined by the crossover between a chalcogenide layer ($Ge_2Sb_2Te_5$, from now on referred as GST) and a vertical resistive slab, which acts as a heater. The structure is completed by bottom and top metal electrodes. Silicon nitride and silicon dioxide layers surround the heater, providing electrical and thermal confinement (Fig. 1b).

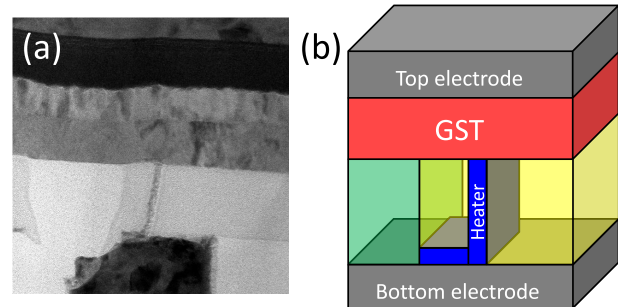

Fig. 1. (a) *"Wall"* architecture. (b) Conceptual device structure [9].

Three representative I-V curves are reported in Fig. 2a. They have been selected from a large set of measurements performed on cells with the same nominal parameters. The curves were measured by driving the device, initially set in the crystalline state, with 300 ns square pulses with increasing voltage amplitude. The current value flowing through the cell was obtained by averaging the signal read across a 50 Ω placed in series to the device. After each pulse, the low field resistance was measured by a Keithley 236 parameter analyzer, forcing 0.2 V across the device. Fig. 2b shows the measured resistance values. Around 1.0 V (200 μA) the resistance increases, thus pointing out that melting has been reached at the heater/GST interface. The devices are characterized by different high-field resistance values, namely 3.5 kΩ, 4.3 kΩ and 5.0 kΩ, respectively. To better highlight the I-V non linearities, the derivative of the three curves have been computed (Fig. 2c). The curves have been smoothed out with a 3-values moving average filter. The curves feature a peak close to the corresponding melting voltage values, namely 0.98 V, 1.10 V and 1.16 V, as indicated by the vertical dashed lines. Note that the lower the heater resistance, the higher the peak height is. As the heater resistance increases the derivative peaks fade away.

III. Models of Electrical and Thermal Conductivity

In order to account for the experimental results, a numerical model of both electrical and thermal conductivities has been developed. Most of the data available in literature refer to the electrical conductivity of polycristalline films collected during temperature ramp measurements. Symbols in Fig. 3a refer to experimental data [2], [6]. The *hcp* phase shows

Manuscript received April 11, 2014; revised April 23, 2014; accepted April 24, 2014. Date of publication May 8, 2014; date of current ver-sion June 24, 2014. The review of this letter was arranged by Editor E. A. Gutiérrez-D. L. Crespi is with the
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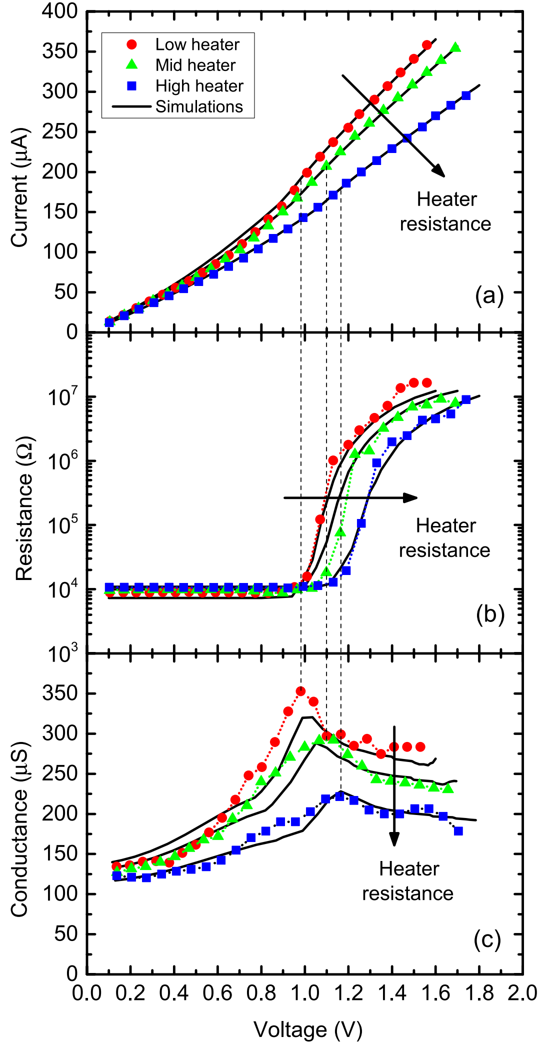

Fig. 2. Experimental data and simulation results adopting the proposed conductivity model. (a) I-V curves. (b) R-V curves. (c) Derivatives of the I-V curves. The vertical dashed lines highlight the melting points, demonstrating that the peak differential conductance occurs when the GST alloy begins to melt. Black lines represent simulation results.

a metallic behavior with a conductivity value decreasing from up to 2000 S cm^{-1} at 300 K to roughly 700 S cm^{-1} at 800 K. The other data refer to *fcc* phases [2] generated by temperature ramps reaching increasing peak temperature values, leading to a conductivity of 10–200 S cm^{-1} at 300 K. These phases show a semiconducting behavior with a temperature activation energy increasing as the conductivity decreases.

Few data are available for the electric conductivity of the molten phase, above 900 K. Some values were measured in liquid GST [7], while the other points were estimated from measurements on PCM devices with line architectures [10]–[13]. The liquid GST behaves as a liquid semiconductor, with a conductivity value increasing with temperature. A weak compositional dependence has been reported along the Sb_2Te_3-GeTe tie-line [14]. No experimental data are instead available for the 600–900 K range as well as an experimental assessment of the discontinuity at melt.

The conductivity model, represented by the solid line in Fig. 3a, was therefore built to be consistent with the above

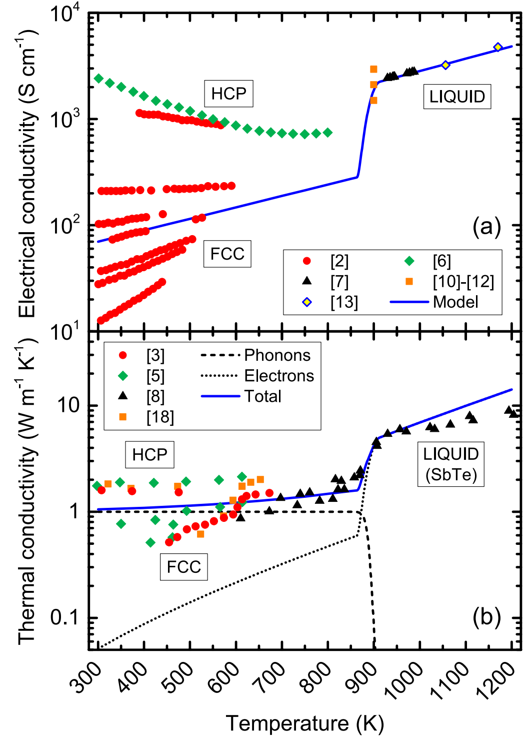

Fig. 3. (a) Electrical conductivity of GST. Solid line refers to the numerical model adopted in the simulations. Symbols refer to experimental results collected on GST phases highlighted by the close-by labels. (b) Thermal conductivity of GST, obtained by superposition of a phononic and an electronic contribution.

experimental results, and then compared with the measurements collected on the PCM cells. The model is qualitatively similar to what already shown in [15] and [16]. From a numerical standpoint, it was convenient to split the model equations in two branches with the same functional dependence:

$$\sigma(T) = \beta e^{\alpha T} \tag{1}$$

where α and β are fitting parameters. The solid-liquid transition around the melting temperature, $T_m = 888$ K, was described by setting a temperature transition range, Δ, and merging the two values at $T_m - \Delta/2$ and at $T_m + \Delta/2$ with a 3rd-order polynomial function, imposing the continuity of both the function and its first derivative. The low temperature conductivity was set to 70 S cm^{-1}, in agreement with the cell resistance in the crystalline state, thus leading to $\beta = 33.31$ S cm^{-1}. The α parameter, which sets the slope of the conductivity dependence on temperature in the solid crystalline phase, was chosen to fit the temperature activation of the device conductivity as measured on the 300–500 K temperature range, leading to $\alpha = 2.475 \times 10^{-3}$ K^{-1}. For the molten phase, instead, the conductivity at the melting temperature was set to 2000 S cm^{-1} [10]–[12], corresponding to a $\beta = 152.0$ S cm^{-1}, while $\alpha = 2.902 \times 10^{-3}$ K^{-1} was set according to [7]. The transition range Δ was set to 50 K. With steeper transitions (lower Δ values), no significant variations in the simulation results were obtained.

The thermal conductivity is linked to the electrical conductivity and plays a key role as well. Fig. 3b shows the model proposed for GST-based chalcogenides. Thermal conductivity

is computed as the superposition of a phononic and an electronic contribution [17]. The phonon contribution accounts for heat transfer mediated by lattice vibrations and it is set to 1 W m^{-1} K^{-1} up to melting. The value is compatible with the experimental data reported in [18] for an *fcc* phase. The electronic contribution accounts for heat transport mediated by carriers, and follows the Wiedemann-Franz law. The solid line reported in Fig. 3b, is the superposition of the two contributions. Following the dependence of the electrical conductivity, the thermal conductivity features a sharp transition at melt, as reported in [8] for similar chalcogenide alloys (SbTe in Fig. 3b).

To perform accurate device simulations, the conductivity model has been introduced into a 3D electro-thermal simulator framework [19], which solves the Poisson's, drift-diffusion and heat equations self consistently. Thermoelectric effects were neglected, to avoid the tailoring of additional parameters. Regarding the heater parameters, the electrical conductivity was taken constant on temperature at 500 S cm^{-1}, while the thermal conductivity follows the Wiedemann-Franz law. The same approach was adopted for the metal electrodes, using an electrical conductivity of 10^5 S cm^{-1}.

The silicon nitride and silicon dioxide thermal conductivity values were taken equal to 1.1 W m^{-1} K^{-1} and 1.4 W m^{-1} K^{-1}, respectively, not depending on temperature. Thermal boundary resistances (TBRs) were also adopted along the GST-SiO_2 interface (50 m^2 K GW^{-1}) and the GST-Si_3N_4 interface (15 m^2 K GW^{-1}), not dependent on temperature [18], [20], [21].

The black solid lines in Fig. 2 show the simulation results. The only difference was the value of the heater resistance, to match the high field slope of the I-V curves. The model well accounts for the I-V and R-V curves, also correctly describing the conductances slope inversion depicted in Fig. 2b, therefore providing a proof of its strong correlation with the conductivity discontinuity at melt.

IV. Conclusion

In this work, evidence has been provided of the discontinuity at melt of the electrical conductivity of phase change alloys. A model has been introduced, based on the experimental data available on GST. The model reliably accounts for the electrical and thermal behavior of PCM devices with *"Wall"* architecture.

Acknowledgment

The authors would like to thank A. Redaelli and E. Varesi for fruitful discussions.

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