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CMOS Impedance Analyzer for Nanosamples Investigation Operating up to 150MHz with Sub-aF Resolution

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This work addresses the emerging need for investigating micro- and nano-devices by performing Impedance Spectroscopy with high-sensitivity yet at high bandwidth. To this goal a new circuital architecture has been implemented that overcomes the limitations of the classic transimpedance topology of noise and maximum operating frequency trade-off as well as of input capacitance stability concerns. Thanks to a two channel modulation/amplification/demodulation structure embedded into a feedback loop, high loop gain at all the working frequencies is obtained. Implemented in 0.35μm CMOS, the IC works from 1kHz up to 150MHz, independently on the input capacitance value up to about 100pF. The IC shows a resolution as good as 0.4aF in the 100kHz-150MHz range (Vin=1V, BW=50Hz). The circuit directly provides two DC outputs proportional to the Real and Imaginary component of the DUT admittance so that no external lock-in structure or filter is required. The output bandwidth is adjustable from few tens of Hz up to 50kHz, thus allowing both fast impedance tracking and high resolution impedance spectroscopy.

Index terms:
Transimpedance amplifier, Impedance spectroscopy, Impedance tracking, Admittance measurement, Lock-in amplifier

I. Impedance measurements at the nanoscale

Impedance analyzers find an important role in nanoscience and in biological research as a tool to access electrical and physical parameters of the matter as well as to enhance the read-out performance in sensor applications [1]. High sensitivity is a very important requirement in these applications due to the small size of the scaled samples that implies a proportional reduction of the electrical signal to be measured. As the total input capacitance (C_{IN}) of the system sets the noise of the measurement, bench-top measuring instruments cannot be used because their input capacitance is often order of magnitudes greater than the intrinsic capacitance of the sample. Instead, high sensitivity can be achieved by developing integrated solutions and embedded setups, in which the input capacitance C_{IN} is efficiently minimized [2].

Other than noise requirements, needs are emerging to perform impedance spectroscopy on a wide frequency range. Electrical assessment of the cell metabolism, for example, requires a frequency of investigation of about 100MHz for the signal to traverse the cell membrane and to access the cytoplasm [3]. Bench-top impedance analyzers exist that cover such a wide frequency range but they are bulky, expensive and have inadequate resolution for the typical high impedance shown by many nanosamples and semi-insulating biological molecules. Recent compact analyzers based on custom CMOS chips are mainly focused on low-power solutions [4]-[6], highly multichannel applications [7], or high-sensitive implementations in the MHz range [8]. Even though the practical implementations of these solutions widely differ, the principle read-out scheme basically consists of a periodic voltage stimulus, a transimpedance amplifier and a lock-in. This topology allows to measure a generic sample ideally without being affected by its stray capacitances to ground and to reach a high sensitivity due to the very small noise bandwidth provided by the lock-in system. When the transimpedance amplifier is designed with a resistive feedback, wide bandwidth requires a small value resistor to avoid the effect of its unavoidable stray capacitance. The thermal current noise of such small value resistor becomes the limiting factor to sensitivity. By implementing a capacitive feedback, the noise of the amplifier is reduced, but the maximum measured frequency is now

dependent on the gain-bandwidth of the operational amplifier and on C_{IN}, which is strongly dependent on the sample and on the setup conditions. A further limit of the transimpedance topology is the low measurement accuracy in the high-frequency range, due to the increasingly smaller value of the loop gain as frequency increases.

The circuit presented in this paper is specifically designed to solve these problems, that is to ensure an operating bandwidth from 1kHz up to 150 MHz independently of the total input capacitance C_{IN}, with noise performances approaching the best solutions operating at much lower frequencies [8].

To reach these goals, a specifically conceived feedback architecture and new circuit solutions have been introduced, as described in the following Chapter II. The requirements will be addressed in Chapter III and a detailed analysis of the main blocks is then presented in Chapter IV. Experimental results will be finally shown in Chapter V.

II. IC working principle

Figure (1) shows the basic scheme of the implemented topology, which uses a down-conversion/amplification/up-conversion architecture inside a feedback structure. In this architecture, the feedback is properly closed when the input signal frequency f_s equals the modulation frequency f_{mod} of the forward amplifier. The incoming signal is firstly modulated to DC frequency by multiplier M1, then amplified by amplifier A with a gain G_A independent of f_s, low-pass filtered by LPF(f) to prevent $2f_s$ component and other spurious harmonics to propagate into the loop, and finally demodulated back to the input frequency by M2. Since the signal is translated into DC, two paths in parallel are required to process both the in-phase (I) and quadrature (Q) input signal components; the unity gain SUM block adds them together as they are translated back into the measurement frequency. The standard operating condition of the circuit of Fig.(1) when $f_{mod} = f_s$ is therefore to acquire the DUT input current and to provide an output V_{HF} at the measurement frequency, whose phase and amplitude are proportional to the input DUT admittance. This

basic idea is the same being used in bench-top impedance analyzers [9], here implemented in a single chip with the benefit of avoiding an additional lock-in system, as it will be further explained, as well as advantages in terms of sensitivity and compactness.

To appreciate the peculiar features of this system, let us consider the loop gain assuming ideal multipliers and perfectly matched paths:

$$G_{loop}(f) = \frac{C_F}{C_{IN} + C_F} \cdot G_{M1} G_A G_{M2} \cdot [LPF(f - f_{mod}) + LPF(f + f_{mod})] \qquad (1)$$

where G_{M1} is the conversion factor from the input to the DC output of the multiplier M1 and G_{M2} is the conversion factor from the DC input to the high frequency output of M2. The loop gain is calculated by opening the loop at the output node V_{HF} and in the case of a purely capacitive DUT (reflecting the semi-insulating characteristics of the typical samples this work is developed for). $\mathbf{C_{IN} = C_{par} + C_{DUT}}$ is the sum of all capacitances at the input node including the DUT capacitance $\mathbf{C_{DUT}}$ and the parasitics to ground C_{par}. **As explained in III.a and eq.(3),** for best noise performance C_F has been designed smaller than the minimum C_{IN}. The frequency shape of G_{loop} is determined by the low-pass filter LPF, that is the block with the most limited bandwidth into the loop.

When the modulation frequency is locked at the input frequency, $f_{mod} = f_s$, the loop gain is high, equal to $\approx \frac{C_F}{C_{IN}+C_F} \cdot G_{M1} G_{M2} G_A \cdot LPF(0)$ and constant at all frequencies f_s of operation. This feature thereby overcomes the classical bandwidth limitation related to the gain-bandwidth product of OpAmps. In our case the high-frequency limit is not determined by the attenuation due to C_{IN}, but by the technology used in the multipliers and by their phase shifts along the loop (not modeled in the first order G_{loop} analysis presented). The use of a 2P4M-0.35µm CMOS process has set the maximum frequency to around 150MHz, but in principle this technology dependent value can be consistently improved by using a scaled technology.

Another interesting aspect of the architecture of Fig.(1) is the availability of the DUT information directly at the two outputs, V_R and V_I, of the low-pass filters. In these nodes the signal is at DC frequency and the outputs are respectively proportional to $I_{dut}cos(\varphi)$ and $I_{dut}sin(\varphi)$, that is to the Real (I) and Imaginary (Q) part of the input admittance. The system therefore embeds into the loop path a lock-in structure, profitably compensating the initially perceived complexity of this realization, when compared with a traditional transimpedance followed by a two-channel lock-in system operating on the high-frequency output V_{HF}, as in bench-top analyzers. The admittance of the DUT can be recovered from the measured values of V_R and V_I by using the following:

$$Re\{Y\} = -\frac{V_R \cdot 2\pi f_{mod} C_F \cdot G_{M2}}{V_x};$$
$$Im\{Y\} = \frac{V_I \cdot 2\pi f_{mod} C_F \cdot G_{M2}}{V_x} \quad (2)$$

where V_x is the amplitude of the forcing voltage across the DUT.

III. System design specifications

Given the basic architecture of Fig.(1), the actual implementation (see Fig.(2)) is slightly more complex dictated by noise, bandwidth and dynamic range considerations. The additional circuitry is necessary to extend the state of the art sensitivity in the impedance measurement [8] up to 150MHz. The need to draw away the DC current at the input node, which would otherwise saturate the amplifier, has been also addressed by adding an additional loop at the input node, which does not interfere with the signal for frequencies greater than 700Hz.

a. Noise performance optimization

The first goal was to reduce the Flicker noise contributions of amplifier A **and of the M1 output in Fig.(1)**, that would otherwise add to the input signal and reduce sensitivity. Chopper technique [10] has been used to this purpose, implemented by two passive mixers (CH1, CH2 in Fig.(2)). In addition, a low noise differential stage B1 (of gain equal to 7) has been inserted after the input node to prevent the white noise contribution of the two multipliers M1 to be boosted by the input capacitance C_{IN}, that now is not directly seen by M1. The amplifier B1 has also the benefit to shield the virtual ground from chopper charge injection, preventing additional input current noise [11], and voltage spikes on the DUT, **sometimes critical for biological applications. Thanks to this topology, best high-frequency noise performance are obtained, anyway worsening the frequency performance below 35kHz due to the B1 flicker noise**. Given these added stages, the signal from the DUT at the exciting frequency f_s is now amplified and converted to a differential signal by B1, chopped at φ_{ch}=150kHz by passive mixer CH1, and modulated at $f_{mod} = f_s$ by the Gilbert cell multiplier M1. This results in signal information at 150kHz at the input of amplifier G1. The second passive mixer CH2, operating at φ_{ch}, brings the signal to DC for further amplification and low-pass filtering. This low-pass stage LPF(f) is implemented by the integrator stage G2 with unity-gain frequency of $1/2\pi RC \approx 10Hz$. Thanks to G2 this architecture has a very large loop gain (≈10^9 in our case) at the modulation frequency.

When looking to the equivalent input current noise $\overline{\iota_{in}^2}(f)$, it has both Flicker noise (due to G2 and M2 stages, whose terms are however attenuated thanks to their peculiar position in the loop) and white noise components (due to B1, M1 and G1). Considering the V_R and V_I outputs in the frequency range of interest, $\overline{\iota_{in}^2}(f)$ can be approximated as:

$$\overline{\iota_{in}^2}(f) \approx (2\pi f(C_{IN}+C_F))^2 \cdot \left(\overline{e_{B1}^2}(f) + \frac{\overline{e_{M1}^2}(f \pm \varphi_{ch})}{G_{B1}^2} + \frac{\overline{e_{G1}^2}(f \pm \varphi_{ch} \pm f_{mod})}{4G_{B1}^2 G_{M1}^2} + \frac{\overline{e_{G2}^2}(f \pm f_{mod})}{2G_{B1}^2 G_{M1}^2 G_{G1}^2} + G_{M2}^2 \left(\frac{C_F}{C_{IN}+C_F}\right)^2 \overline{e_{M2}^2}(f \pm f_{mod}) \right) \quad (3)$$

where $\overline{e_{B1}^2}$, $\overline{e_{M1}^2}$, $\overline{e_{G1}^2}$, $\overline{e_{G2}^2}$, $\overline{e_{M2}^2}$ are the **equivalent input** power spectral densities of B1, M1, G1, G2 and M2 respectively. The chopper modulation has been approximated by a modulation at the fundamental frequency φ_{ch} with a unitary gain to preserve the power in the case of a white noise.

Other than B1 input buffer ($1.3\,nV/\sqrt{Hz}$**, 7.2mA current consumption**) , M1 multiplier ($6.5\,nV/\sqrt{Hz}$, **0.7mA current consumption**) plays a significant role in the overall system noise, even if partially attenuated by B1 gain. The noise of G1 ($9\,nV/\sqrt{Hz}$, **0.18mA current consumption**) and LPF ($313\,nV/\sqrt{Hz}$, **0.56mA current consumption**) are strongly reduced thanks to the high gain of their previous stages in the loop ($G_{M1}=10$, $G_{G1}=10$). The contribution due to M2 ($22\,nV/\sqrt{Hz}$, **11mA current consumption**) is calculated by considering the current which **should flow into C_F to cause the noise at the V_{HF} node**: it plays instead a major role due to its position after the outputs along the feedback loop, directly adding to V_R and V_I DC outputs. Its contribution has been reduced by selecting a C_F of 100fF, twenty times smaller than the input capacitance of the chip.

b. System output bandwidth specifications

In order to achieve the highest possible resolution, the output system bandwidth should be designed as small as possible to minimize the rms output noise. In our prototype a bandwidth as low as about 50Hz can be selected. In addition to reduce the output noise, such small bandwidth effectively filters out the spurious

harmonics produced by modulators M1, CH1 and CH2. To cope also with applications in which instead high-speed measurements are desired, we made the bandwidth user-selectable by proper switches (see Par.IV.c) up to 50kHz.

To calculate the system bandwidth, we can study the G_{loop} and determine the value f^* for which $|G_{loop}(f^*)| = 1$. With reference again to Fig.(2), the G_{loop} for V_R and V_I outputs can be approximated as

$$|G_{loop}(f)| \approx \frac{1}{2\pi f C R} \frac{C_F}{C_{IN} + C_F} \cdot G_{B1} G_{M1} G_{G1} G_{M2} \tag{4}$$

The bandwidth of the low-pass outputs is therefore given by

$$f^* \cong \frac{1}{2\pi C R} \frac{C_F}{C_{IN} + C_F} G_{B1} G_{M1} G_{G1} G_{M2} \tag{5}$$

This result shows that the feedback is active only in a small frequency range around the DC signal, that can be tuned by changing the values of C and R_{equ} in the LPF (see Par. IV.c). Considering now the V_{HF} output, node at which the DC signal is up-converted to f_{mod}, it's straightforward to understand that the circuit amplifies only the frequencies in the small interval $f_{mod} \pm f^*$. This behavior can be formally obtained by studying the system real transfer function, which shows a very narrow band-pass behavior thanks to the presence of two complex conjugates poles.

c. Offset and Dynamic Range analysis

Each stage of the circuit experiences a feedback only in a very limited frequency interval. Any signal being generated outside this frequency interval would initially propagate along the loop, being amplified and multiplied, until it reaches the low pass filter G2 where it is filtered out. The main sources of these signals are the DC offsets of each stage along the loop and the harmonics produced by the multipliers, as well as

the spurious signals directly injected into the input node. All these spurious components stress the dynamic range of the full circuit. To clarify this point, let's consider for example the $2f_{mod}$ and $3f_{mod}$ harmonics due to M2 nonlinearity and mismatch: after a first attenuation $C_F/(C_F + C_{IN})$, the harmonics are amplified by a factor $G_{B1}G_{M1}G_{G1} \approx 700$ before being filtered out. Under normal circumstances, harmonics can be in the mV range, leading to signals of hundreds of mV at G2 input. **These signals are much bigger than the error signal of the feedback loop related to the DUT input current. These considerations lead to the conclusion that the design of each stage along the loop should be tuned to minimize offset and harmonic distortion** while providing a dynamic range much higher than the one which would be required for the DUT feedback signal only.

d. Input DC current feedback loop

The presence of a capacitance in the feedback requires a reset network to drive away the DC current from the input node that would otherwise saturate the impedance analyzer. To this purpose, a dedicated loop has been implemented (see Fig.(3)), based on an architecture already available in the literature [12]. This loop should be active only at frequencies around DC but not interfere with the main signal at any other frequency, in addition to not to increase the overall system noise. Referring to Fig.(3), information (the input virtual ground DC value) is taken at φ_{ch}=150kHz, after CH1, amplified by G3 ($G_{G3} = 10$), then chopped back into DC by CH3. A differential-to-single-ended converter (G4) drives the filter H(s) that provides stability (through the zero R_zC_1), a high DC gain, a limited bandwidth (max 700Hz) in the DC feedback loop. A physical resistor R_{ATT}=2MΩ, followed by an active current divider (G6 network [13]) with division factor equal to N=10, operates as an equivalent resistor of 20MΩ that closes the DC loop and collects the DC current from the input node. The DC feedback loop effectively removes the input DC current up to ±60nA. The current division device Z_{NL} is made of PMOS and NMOS in common gate configuration in parallel with a capacitor acting as a high-frequency bypass to grant loop bandwidth stability independently of the input DC current value. The added value of this solution is that, in the frequency range for which the main loop

has high loop-gain ($\mathrm{f_{mod}} - \mathrm{f}^*, \mathrm{f_{mod}} + \mathrm{f}^*$), the active current divider G6 injects a very low noise to the input node, **N² times lower than the noise of the physical resistor, equivalent to a resistor of 200MΩ [12].**

The chopped amplifier structure made of CH1, G3 and CH3 is an effective structure [10] for reducing the offset that the DC current loop introduces into the main amplifier loop. If CH1, G3 and CH3 were not present, and G4 were directly connected to the output of B1, the offset at the input of G4 would have caused CH1, M1 to generate spurious harmonics into the main loop (few mV offset are sufficient for causing harmonics of hundreds of mV at the G2 input, as mentioned in previous paragraph).

The adopted solution efficiently exploits the already existing CH1 and reduces the input offset below the mV range:

$$Vos_{DCloop_{in}} = \frac{1}{G_{G3}}\left(V_{G4_{os}} + \frac{V_{G5_{os}}}{G_{G3}G_{G4}} + \frac{V_{G6_{os}}}{G_{G3}G_{G4}H(0)}\right) \quad (6)$$

No new offset is added by the new stage G3, which instead is responsible for a reduction of a factor G_{G3} of the input DC loop offset preserving a low capacitance at the output of B1. Considering a matched current divider of factor N, the feedback loop can be approximated to

$$G_{loop,DC}(s) \cong G_{B1}G_{G3}G_{G4} \cdot \frac{1 + sC_1R_z}{sC_2R_z} \cdot \frac{1}{NR_{att}} \frac{1}{sC_{IN}} \quad (7)$$

where C_1, C_2 and R_z are the filter H(s) components. An equivalent resistance **R_z of 1TΩ obtained with four cascaded current dividers [12]** assures a feedback stable for input capacitance C_{IN} up to 100pF. The ratio $C_2/C_1 = 400$ is designed to have an effective feedback only for frequency lower than 1kHz independently of the DUT sample.

IV. Design details of the stages along the loop

a. Input buffer B1

The input buffer B1 (see Fig.(2)) has demanding requirements in terms of noise and bandwidth. A noise contribution as low as $1.2nV/\sqrt{Hz}$ with a 35kHz noise corner has been obtained by using **the single differential stage with PMOS input device and resistive load configuration shown in Fig.(4). This simple topology is biased by 7.2mA** and provides a gain of about 7, enough to significantly reduce the M1 noise contribution. A bandwidth greater than 350MHz is instead necessary to avoid phase delay along the loop all over the full frequency range not to affect the system high-frequency limit. The dynamic range of the buffer output is instead relaxed and has allowed to include a cascode structure. This solution not only increases the amplifier bandwidth, but also decouples the input MOS C_{gd} from the output nodes to reduce the chopper CH1 feed-through back to the system input node down to few mV in the worst case.

b. Down-conversion multipliers M1

The down-conversion multiplier M1 has been implemented as a double balanced Gilbert cell, chosen for its simplicity which directly reflects in a small number of noise and mismatch sources to be optimized. The modulation signal (f_{mod}) input is assigned to the upper differential pairs, while the lower pair is dedicated to the loop signal: the input capacitance has been limited to 360fF for not compromising B1 bandwidth. **This area constraint limits the maximum stage matching as well as its transconductance, causing an f_{mod} output spurious harmonic and a limited maximum stage gain. For the current implementation, Monte Carlo simulation of the expected output harmonic gives a mean amplitude of 22mV (standard deviation of 19mV).** A good matching is also required for the two upper differential couples, which would cause $2f_{mod}$ and $3f_{mod}$ harmonics and DC output offset. These sources of mismatch have been optimized to reduce the DC output offset down to 1.9mV (σ = 1.4mV). As already mentioned in III.c, these output components do not experience the feedback and propagate and amplify into the loop up to the integrator G2. **A conversion gain $G_{M1} \cong 10$ for an external differential modulation signal of 300mV has been designed to further reduce offset and noise requirements of the following stages. Concerning noise, the implemented cell has an equivalent input noise of $6.5nV/\sqrt{Hz}$ and a noise**

corner of 15kHz with a current bias of 0.7mA, contributing almost as much as the input buffer B1 to the overall system noise.

c. Integrator Filter G2

The integrator G2 is the stage that sets the system bandwidth and provides very high gain at $f_s=f_{mod}$. When selecting the lowest bandwidth (in our prototype chosen at 50Hz for $C_{IN}\cong$ 10pF) its unity-gain frequency must be as low as 10Hz. This extremely low value cannot be obtained with passive R_{equ} and C integrated components. We used an architecture (Fig.(5)) where the current from a physical resistor of R_{in}=1MΩ is divided by a factor of 10.000 (N_1xN_2), thus obtaining the desired equivalent resistor (R_{equ}) of 10GΩ, to be coupled with a C_{int} of 1.6pF. **Thanks to the global feedback, in steady state conditions no DC current is foreseen into the resistor: the two cascaded current dividing stages (G8 and G9) can be implemented by using pairs of properly matched capacitors. Differently from the current divider in [13], in which a couple of matched transistors were used, capacitors are indeed noiseless components that also grant high linearity.** This last aspect is very important because the input of the integrator stage receives not only the loop signal at around DC but also all the spurious harmonics created by the previous stages. A non-linearity of the integrator could down-convert these spurious frequencies into spurious DC components that would be integrated by capacitor C_{int} the same way as the DUT signal affecting the accuracy of the DC outputs V_R and V_I.

A DC current is required to charge C_{int} and set V_R and V_I to the values imposed by the input admittance. This DC current is provided by T1-T2, a pair of PMOS with common source and common well. **This two-port device has been preferred to the solutions proposed in [13] and [14] for symmetry reasons. A nominal symmetric I-V characteristic is assured because both positive and negative currents flow through the series of a PMOS transdiode and a parasitic well-drain n-p junction. This feature helps high voltage spurious signal to be rejected, limiting T1-T2 nonlinear effect due to**

mismatches between devices. During steady state conditions, instead, the T1-T2 path is practically off even in the worst condition of input spurious harmonics of 500mV and 10kHz, ensuring their efficient and linear cut-off through the capacitive loads. The integrator unity-gain frequency is digitally controlled by varying the dividers ratio N_1 and N_2, thus changing R_{equ} from 10GΩ to 500MΩ, 200MΩ or 10MΩ and **consequently varying the system bandwidth from 50Hz up to 50kHz (for C_{IN}=10pF) as expressed by eq.(5). Uncertainty in R_{in} and R_{equ} only affects bandwidth but not the overall gain of the system.**

In order to provide to the active resistance the required bias conditions, the integrator input nodes voltages must be set to the middle of the dynamic. This requirement prevents the scheme of Fig.(5) to be directly converted into a fully-differential solution, in which any CM loop would only be able to control the output CM. The integrator has therefore been implemented as in Fig.(6): it is made of two single-ended integrators in parallel. To recover the peculiarity of a differential architecture to dump common mode fluctuations, the two single-ended paths have been tied together by a common mode (CM) feedback loop. This loop first senses the CM outputs by using G7 amplifier ($G_{G7} = 10$) and uses this error signal to modify the CM reference of the G1 stage. Its common mode output is consequently modified thanks to the G1 CM internal feedback loop shown in Fig.(7), necessary for keeping a reliable DC working point to the stage; this solution allows to **properly set** the integrator inputs to feedback the G2 common mode output. Note that the differential chopper CH2 doesn't influence the CM signal and it can be neglected in the loop analysis. This solution exploits the optimized and easy transfer function of the complex active filter, never modifying its internal bias nodes: in this way the filter dynamics is always maximized and undesired non-linear behaviors are avoided. The CM loop bandwidth can be correspondingly calculated as

$$f_{BW} = G_{G7}/2\pi C R_{equ} \quad (8)$$

d. Up-conversion stage

Differently from the down-converter M1 described above, the design of the up-conversion stage M2 (see Fig.(8)) is much more critical since the multiplier is placed along the feedback path right after the V_R and V_I outputs and therefore its noise, linearity and offset are affecting directly the overall performance. With reference to Fig.(2), this stage first translates the DC outputs to the f_{mod} frequency through M2 multipliers and then add them together through SUM to generate the V_{HF} output. In order to achieve linearity over an extended range of V_R and V_I, multipliers M2 have a conversion factor equal to G_{M2}=1 when operated with a differential modulation signal of 300mV. They are made of a couple of four-quadrants Gilbert cells, whose current output signals are then added together by means of a series of mirrors to obtain a ±1V differential output dynamic **range of the circuit** without causing any unbalance to the Gilbert cell.

In place of the classic differential pair, the lower multiplier inputs have been replaced by the voltage-to-current converter topology in Fig.(9), which provides a ±1V differential input dynamic range. This circuit is made of a couple of input followers T_3, through which the input voltage is applied to the resistor R, generating a linear current I_R. This current signal is read by T_6 as a result of the local feedback structure (provided by T_3, RC and T_6) and mirrored by T_7 to the output. Transistors T_4 and T_5 are **required** to prevent T_6 to enter ohmic region when large input signals are applied. In the case one of the two T_6 enters ohmic region, its gate voltage increases more than expected (due to the dependence on the drain-source voltage); the output MOS T_7, still working in saturation regime, increases its current well above T_6 current, changing significantly the common mode V-to-I output current. **The ultimate effect of T_6 going ohmic is shown in the graph in Fig.(8), grey curve: M2 gain would drop, causing a non-monothonic behavior outside the linear range and therefore loop instability (G_{loop} changes its sign). To prevent this and obtain the black input-output characteristic in Fig.(8), T_4 and T_5 are designed to switch-on and stabilize the overall V-to-I converter stage outside the linear dynamic region.** The bandwidth of the multiplier is about 400MHz and is defined by the $\tau = 1k\Omega \cdot 400fF$ output node time constant.

To stress how linearity and offset are important factors in the stage design, let us recall that output spurious harmonics of stage M2 would be fed back into the loop by the capacitance partition $C_F/(C_F + C_{in})$ and amplified before reaching the Integrator filter G2, possibly causing stages saturation. Gilbert cells have therefore been sized both with high overdrive and high current to limit output harmonics: given a 1V input, $2f_{mod}$ and $3f_{mod}$ harmonics, estimated through Montecarlo simulation, have an average peak value of 6.5mV and 3.1mV, with a standard deviation of 2.1mV and 1.1mV respectively. The up-conversion stage draws alone more than half (**25mA, 11mA for each M2 stage and 3mA for SUM mirrors**) of the total system current consumption, a fee to cope with high dynamic and linearity requirements on such a low output resistance. Despite the stage complexity, **the equivalent input noise at each M2 input has been limited to $22nV/\sqrt{Hz}$, partially contributing to the equivalent input noise when weighted by $C_F/(C_{IN} + C_F)$** .

V. Experimental results

The circuit has been implemented in AMS 0.35um C35B4 technology **as shown in Fig.(10),** occupies 1.6 mm^2 and has a static current consumption of **37.5mA when biased at 3V. An optional output buffer with a current consumption of 6.5mA can be switched on for testing the high frequency output V_{HF}.** The system has been fully characterized to certify the ability of the system to perform both samples spectrum acquisition and impedance time-tracking. The IC can be considered as the core of the impedance analyzer, whose structure is completed by a **Direct Digital Synthesizer (DDS)** for input and modulation signal generation, and 24-bit ΔΣ ADCs for the conversion of the output signals. The instrument principle scheme is completed by a μC for interfacing with a computer for static control and data acquisition. A ring oscillator, implemented on-chip, generates the clock signal for chopper multipliers CH1 and CH2; the frequency can be digitally selectable between about 150kHz, 75kHz and 18.75kHz, thus avoid any possible overlapping between the chopper and the measurement frequency.

a. System characterization

Figure (11) shows the measured transfer functions between the input (V_X) and the output V_{HF}. The measurement is performed by choosing a given modulating/demodulating frequencies, f_{mod}, and spanning the frequency f_S of the injected current by means of a test capacitance $_{test} = \ _F = 100fF$. The expected bandpass shape is observed, always centered at the different f_{mod} values. The expected gain $= - \ _{test}/\ _F = -1$ at f_S=f_{mod} is reached within ±1dB over the full frequency range from 1kHz to 150MHz and within ±0.1dB in the 3kHz-130MHz range. The figure shows that the minimum bandwidth of about 50Hz can be effectively reached over the full frequency range, practically independent of the operating frequency, thus providing an efficient noise filtering when requested. The bandwidth reduction visible in the 1kHz measurement of Fig.(11) is due to the limited bandwidth of the external RF transformers used for driving the modulation signal to M1 and M2. For faster impedance measurements, the single side bandwidth can be increased by up to a factor of 1000 to about 50kHz, as shown in Fig.(12), by digitally modifying the capacitive ratio that sets the equivalent resistor of G2 (see Fig.(5)) to 10GΩ, 200MΩ or 10MΩ in the given example.

The functionality of the circuit is shown in Fig.(13), where the impedance spectrum of known components connected to the input pad of the chip is reported. Continuous line is the analytical expected curve and squares are the experimental values as extracted directly from the DC voltages V_R and V_I. Thanks to the large frequency span up to a working frequency of 150MHz, all the significant information can be retrieved: **the bypass 15pF capacitance at low frequencies, the 100kOhm resistor at the medium frequencies and the 100fF parasitic capacitance at high frequencies, showing the effectiveness of the presented scheme; as shown in Fig.(14), in the 3kHz – 150MHz interval the measurement relative error stays within 20%.**

b. Noise Performance and sensitivity

To access the sensitivity of the circuit in the measurement of the impedance, a comprehensive noise characterization has been performed. In this case no DUT has been connected to the input pad, thus expecting an intrinsic parasitic capacitance to ground of 2pF being present. In Fig.(15) we show the equivalent input current noise spectral density as measured from the system DC outputs at $f_{mod} = 1MHz$. The figure shows the two extreme cases of 50kHz and 50Hz bandwidth conditions. The 50kHz condition allows to clearly identify the white noise value of 100fA/sqrt(Hz) with a noise corner of 60Hz. In the 50Hz mode a complete filtering of the white noise is achieved, so to reach the highest sensitivity. The extremely low level of the flicker noise is granted by the 2-steps down-conversion, which avoids the 1/f noise of multiplier M1 and reduces the 1/f term of integrator G2 in a very effective way.

By measuring the noise for different f_{mod} and assuming an applied voltage of 1V, the achievable capacitance resolution has been obtained and plotted in Fig.(16). The system can meet the desired attoFarad resolution over four decades, from 20kHz to 150HMz. This level of sensitivity over such an extended frequency range surpasses the performance of available impedance analyzers. As an additional test to access the actual sensitivity of the chip, a tracking of the capacitance with time has been performed (see Fig.(17)). In this case the DUT consists of a variable capacitance, one plate being the instrument input BNC connector, the other being a copper sheet held by a micromanipulator, whose distance can be manually changed by the connector through the micromanipulator. Thanks to this fine tuning, 7aF capacitance variation is induced, steps which are clearly visible in Fig.(16) with such a sub attoFarad resolution system.

Finally, the table I summarizes the performance of the chip and compares it with the state of art. The modulation/demodulation technique presented in this work allows to achieve the wider operating frequency range. The low-noise high-value equivalent resistances combined with the chopper technique assures a high sensitivity on the full frequency range.

II. Conclusion

This paper presents an integrated system for impedance tracking or impedance spectroscopy. It is based on a forward amplifier organized as a two-channel modulation/amplification/demodulation circuit embedded into a feedback loop. The architecture features high loop gain at frequencies from 1kHz to 150MHz, ensuring stability and high linearity at all measuring frequencies. Real and Imaginary part of the input sample admittance is directly available at the DC system outputs, avoiding the need for any external lock-in filter. The noise figure of merit of the resulting impedance analyzer (about 0.4 aF in terms of capacitance resolution from 100kHz to 100MHz) is one order of magnitude better than available solutions operating over a similar frequency range. Thanks to its performance, the implemented IC can be considered the basic block for the development of embedded setups for high-sensitivity wide-bandwidth impedance measurements in different contests and applications.

[1] J. Guan, Y. Miao and Q. Zhang, “Impedimetric Biosensors” J. Bioscience and Bioengineering, vol. 97, no. 4, pp. 219–226, 2004.

[2] D. Bianchi, M. Carminati, G. Ferrari, M. Sampietro, “CMOS Current Amplifier for AFM Impedance Sensing on Chip with ZeptoFarad Resolution”, Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 61-64, Jun 2013.

[3] T. Sun and H. Morgan, “Single-cell microfluidic impedance cytometry: a review,” *Microfluidics and Nanofluidics*, Vol. 8, pp. 423–443, Mar. 2010.

[4] C. Yang, S. R. Jadhav, R. M. Worden, and A. J. Mason, “Compact Low-Power Impedance-to-Digital Converter for Sensor Array Microsystems,” *IEEE Journal of Solid-State Circuits*, Vol. 44, pp. 2844–2855, Oct. 2009.

[5] H. Jafari, L. Soleymani, and R. Genov, “16-Channel CMOS Impedance Spectroscopy DNA Analyzer With Dual-Slope Multiplying ADCs,” *IEEE Trans. on Biomedical Circuits and Systems*, Vol. 6, pp. 468–78, Oct. 2012.

[6] J. Guo, W. Ng, J. Yuan, and M. Chan, “A 51fA/Hz$^{0.5}$ low power heterodyne impedance analyzer for electrochemical impedance spectroscopy,” *IEEE VLSIC,* pp. 56–57, June 2013.

[7] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, “A CMOS electrochemical impedance spectroscopy biosensor array for label-free biomolecular detection,” *ISSCC Dig. Tech. Papers,* pp. 130–131, Feb. 2010.

[8] F. Gozzini, G. Ferrari, and M. Sampietro, “An instrument-on-chip for impedance measurements on nanobiosensors with attoFarad resoution,” *ISSCC Dig. Tech. Papers*, pp. 346–347, Feb. 2009.

[9] R. Sakiyama, “Narrow-band amplifier and impedance-measuring apparatus,” *US Patent App. 20,040/257,093*, 2004.

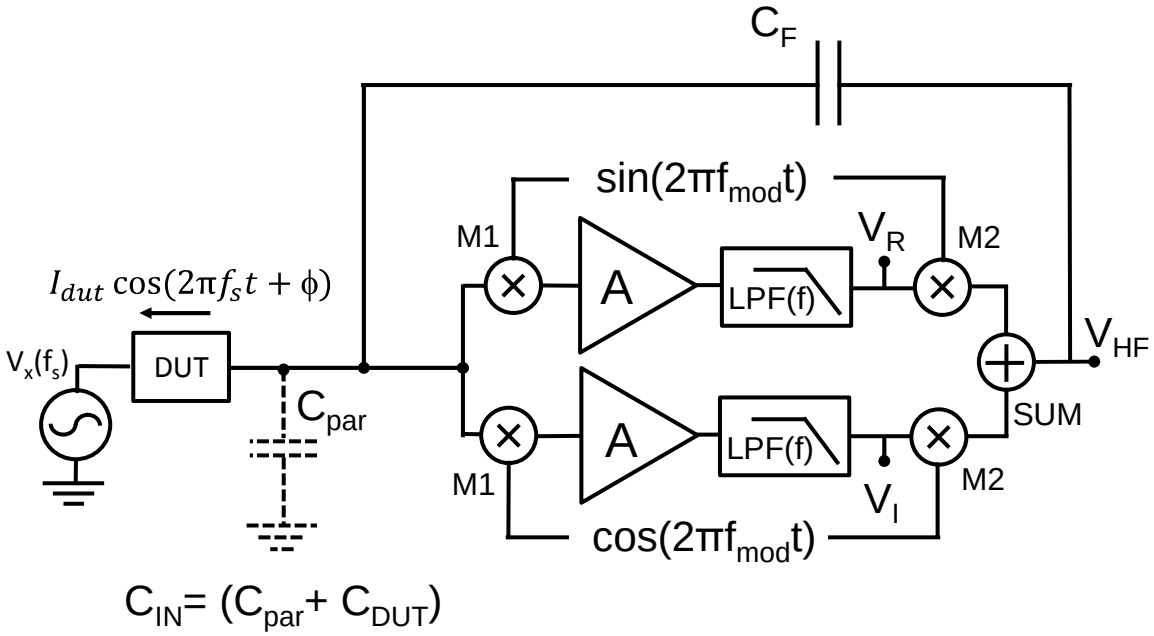
[10] C. C. Enz and G. C. Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization,” Proc. IEEE, vol. 84, no. 11, pp. 1584–1614, 1996.

[11] J.Xu, Q. Fan, J. H. Huijsing, C. Van Hoof, R. Firat Yazicioglu, K. A. A. Makinwa, “Measurement and Analysis of Current Noise in Chopper Amplifiers”, IEEE J. Solid-State Circuits, vol. 48, no. 7, pp. 1575–1584, 2013.

[12] Gozzini, A. Molari, and M. Sampietro, “Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices,” IEEE J. Solid-State Circuits, vol. 44, no. 5, pp. 1609–1616, May 2009.

[13] F. Gozzini, G. Ferrari, and M. Sampietro, “Linear transconductor with rail-to-rail input swing for very large time constant applications,” *Electron. Lett.*, vol. 42, no. 19, p. 1069, 2006.

[14] R.R. Harrison and C. Charles, “A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications,” IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 958 – 965, Jun. 2003



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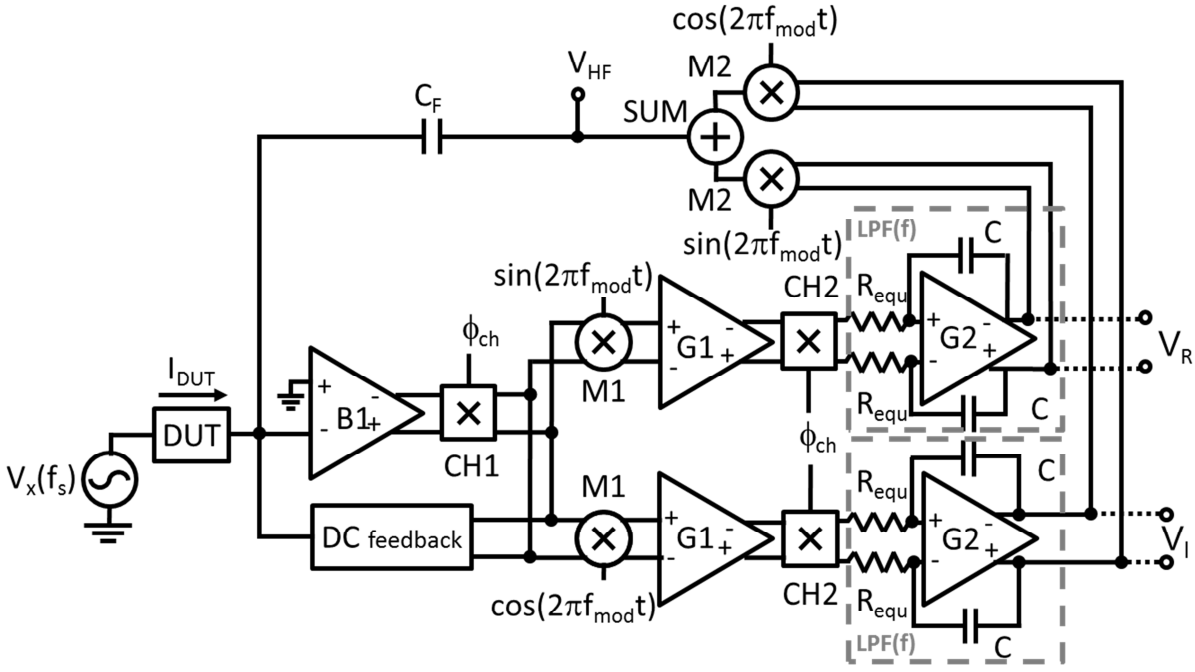

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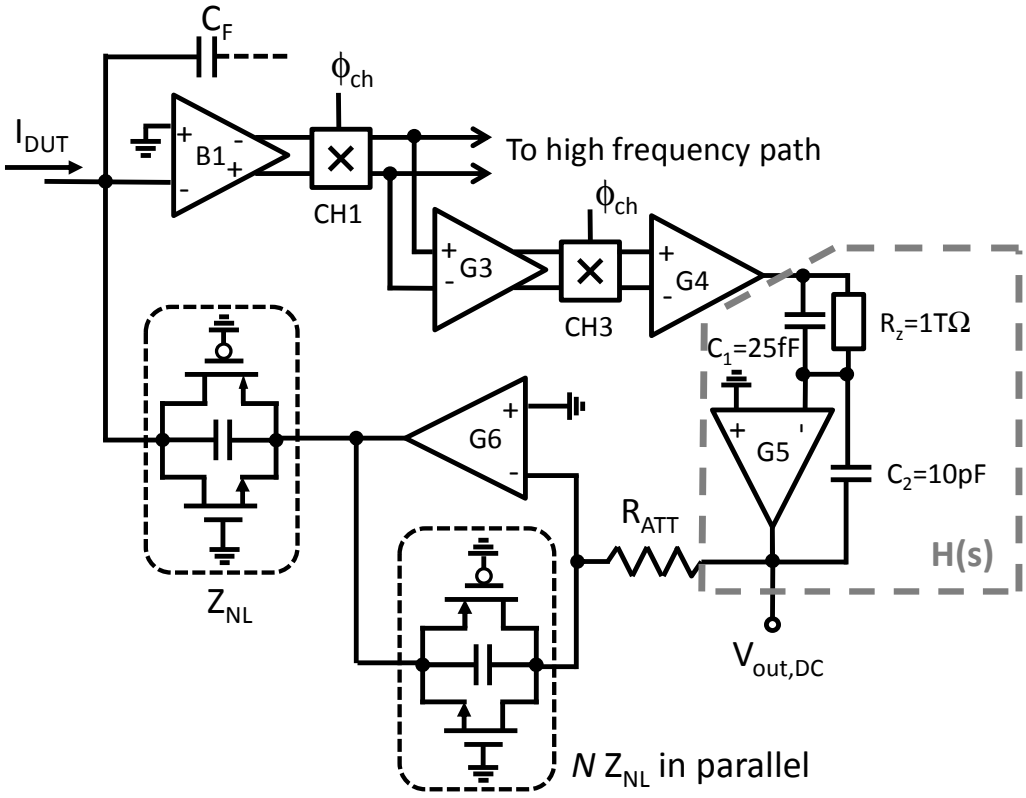

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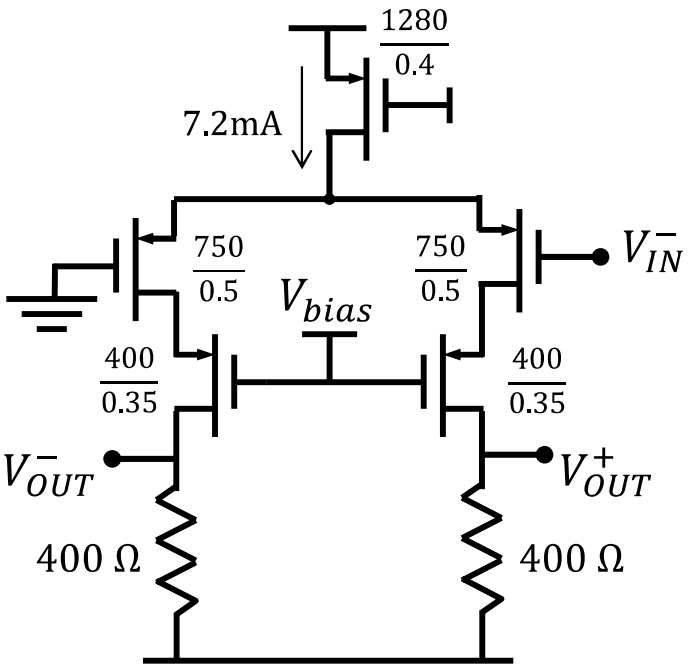

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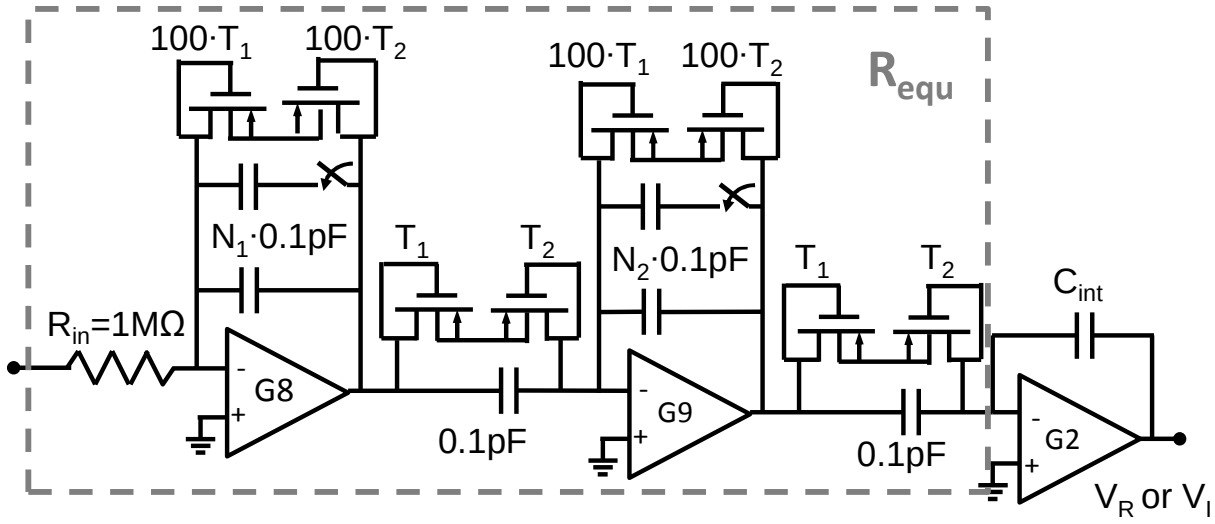

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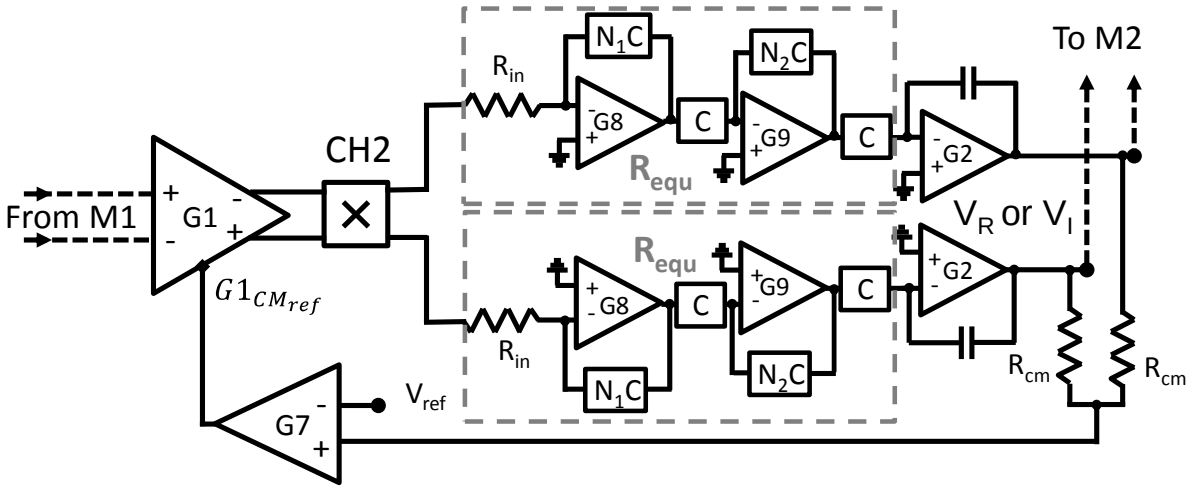

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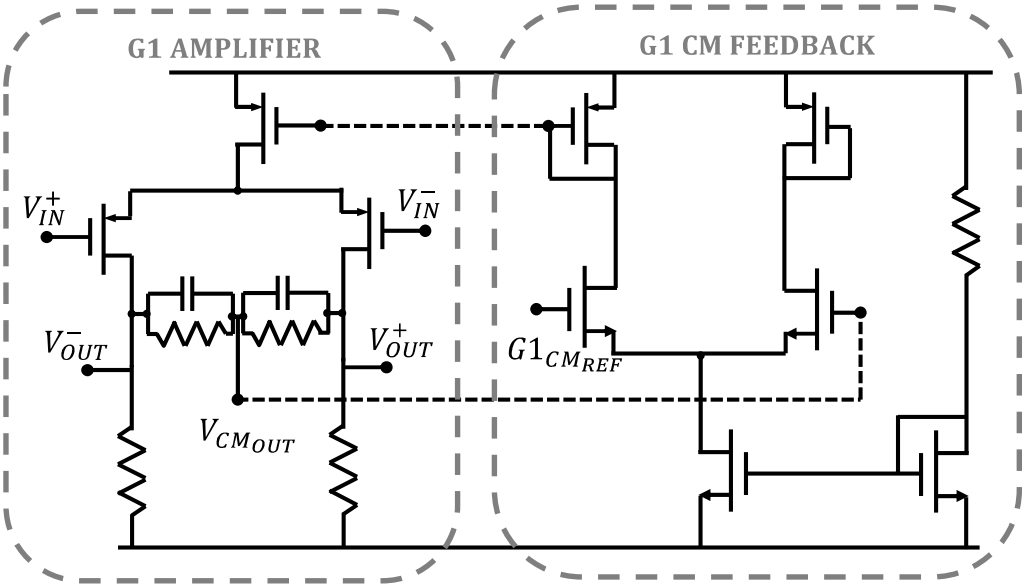

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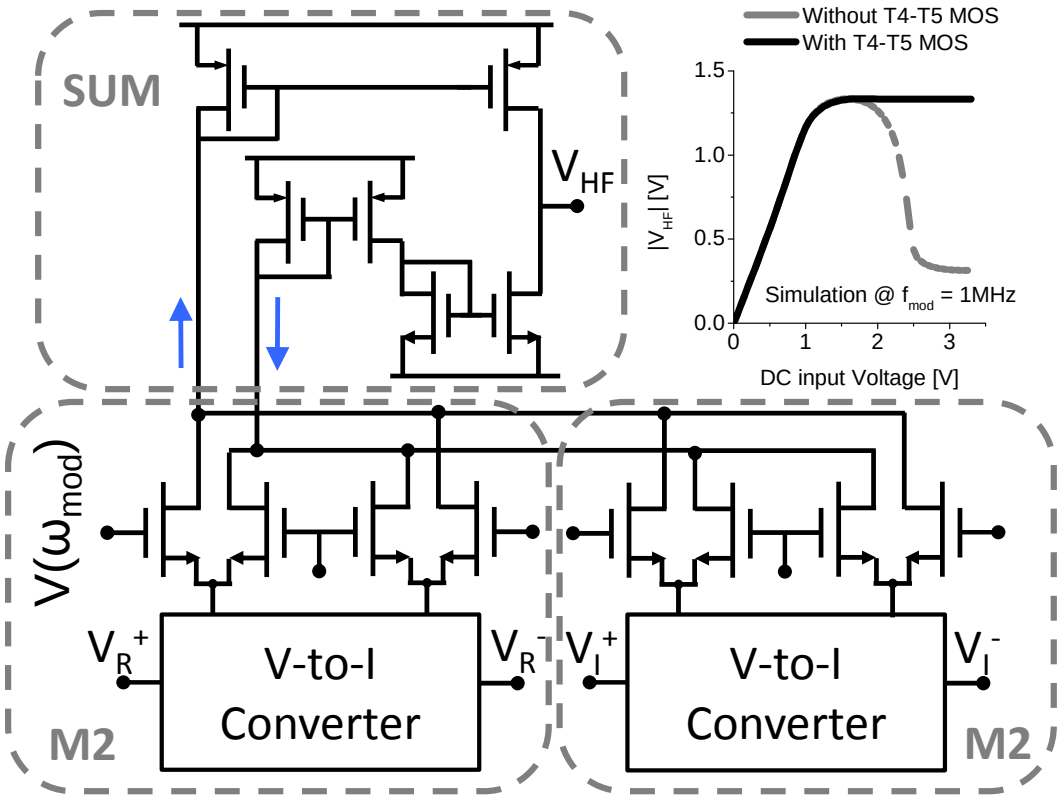

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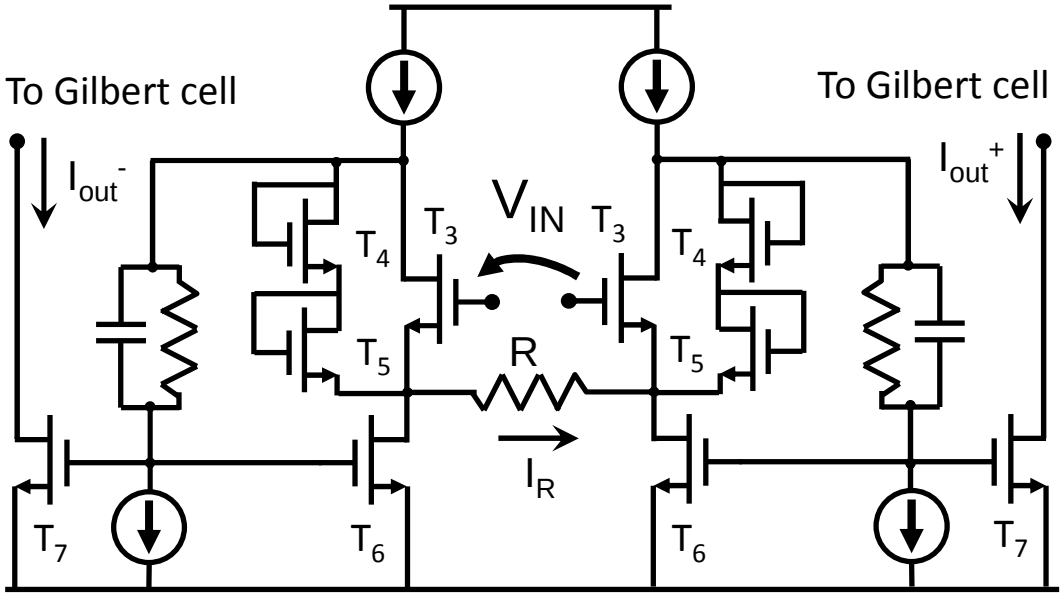

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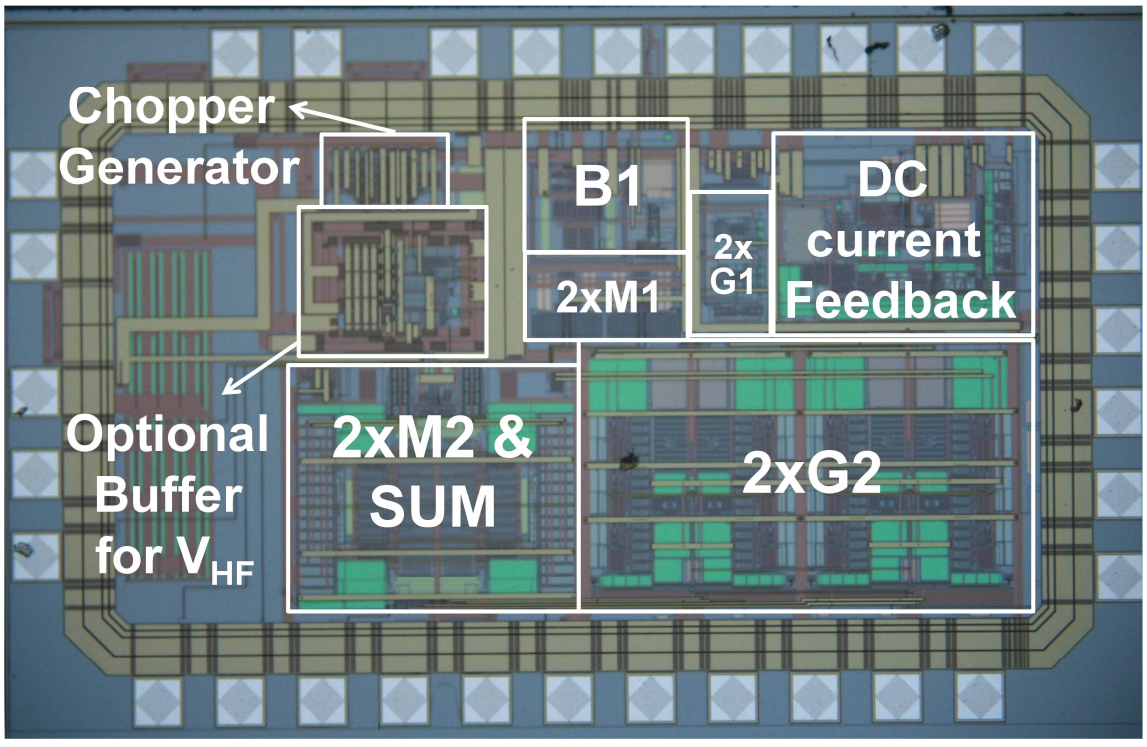

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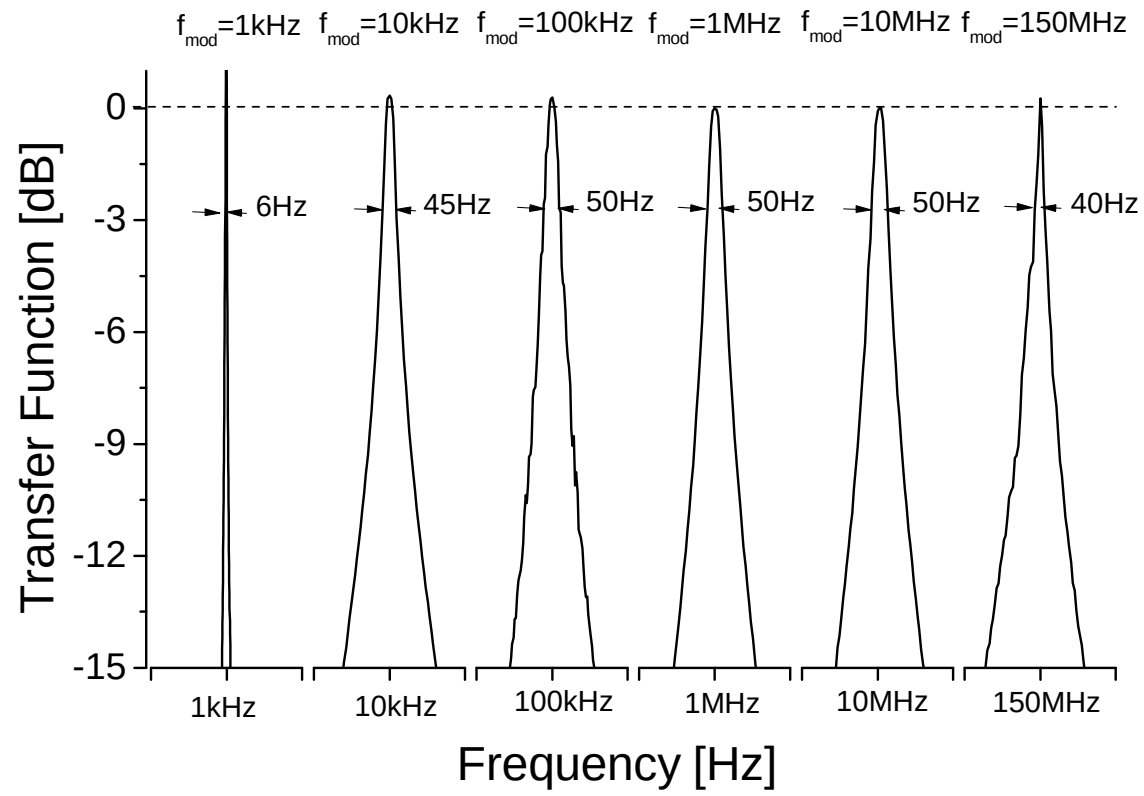

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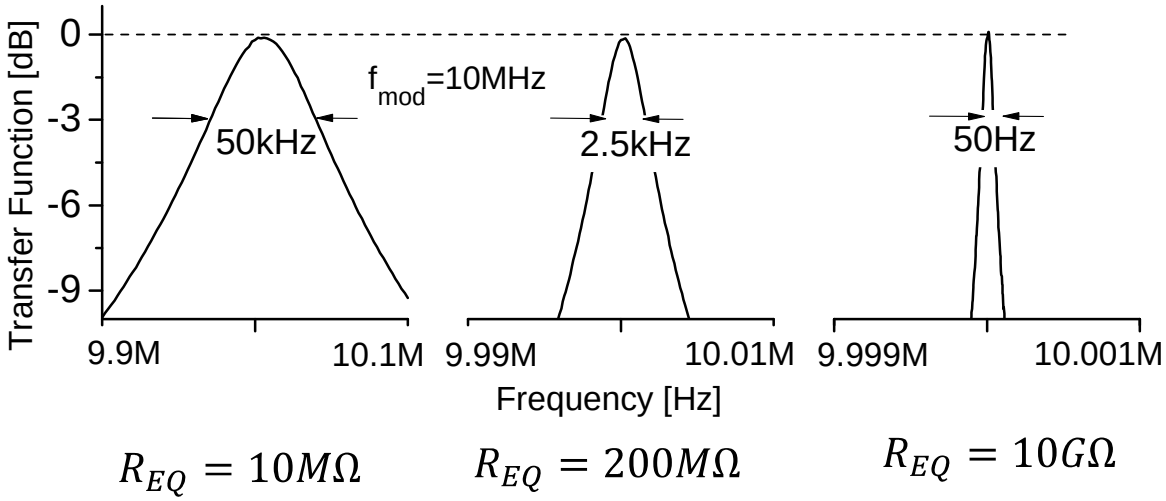

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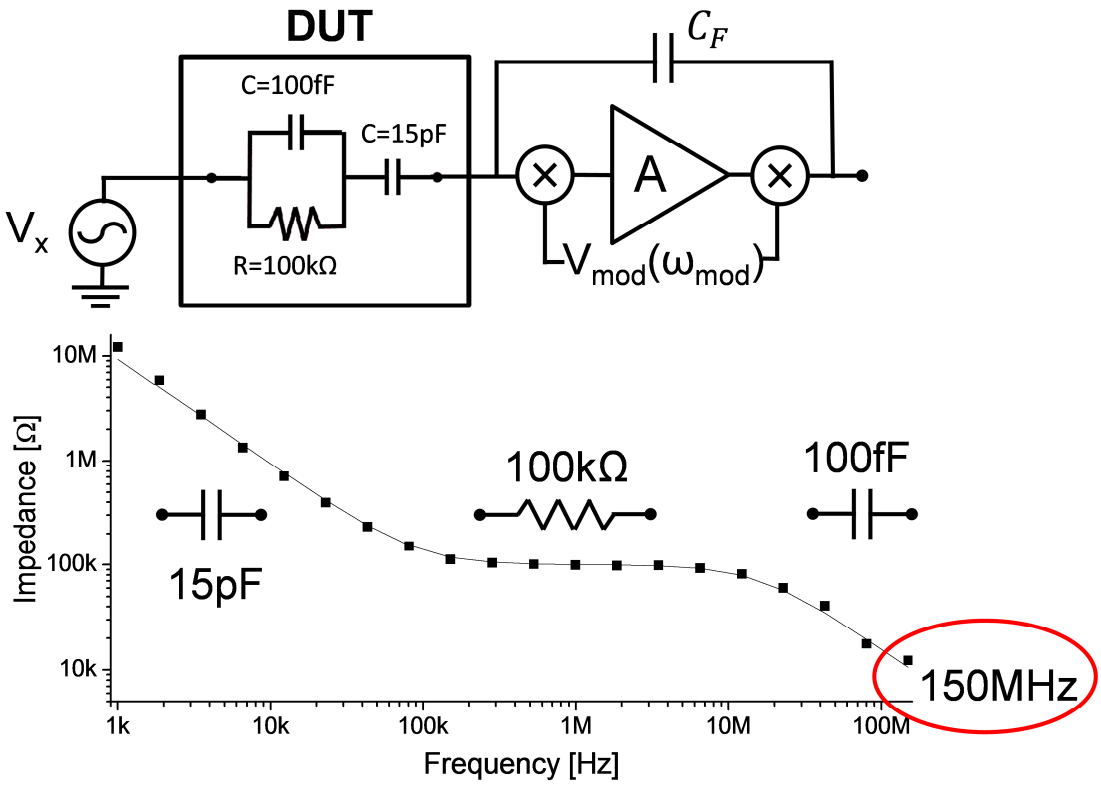

Figure 13

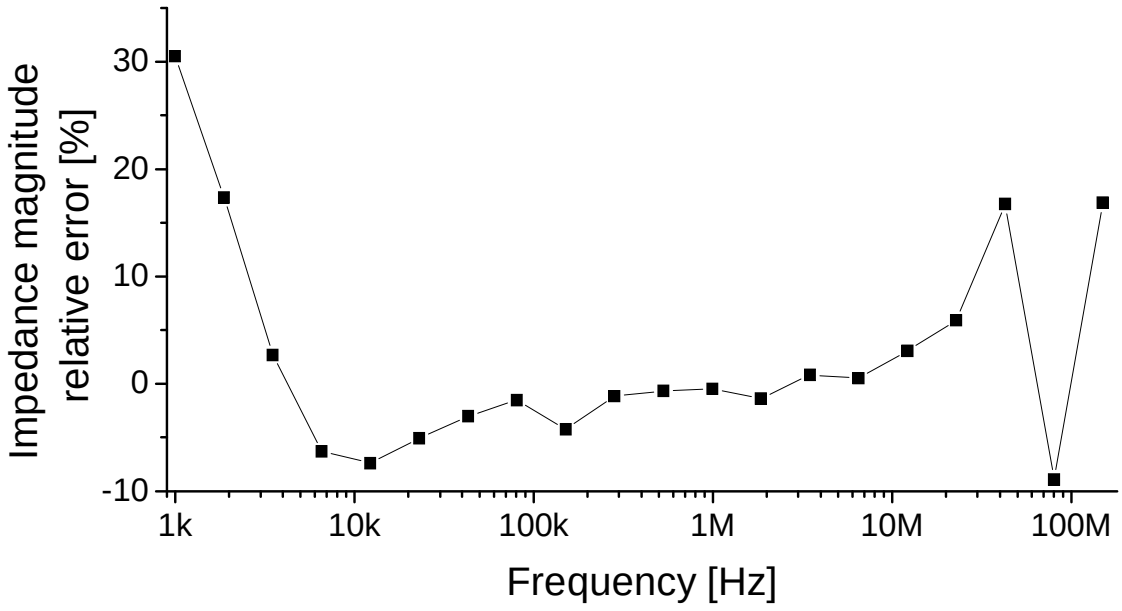

Figure 14

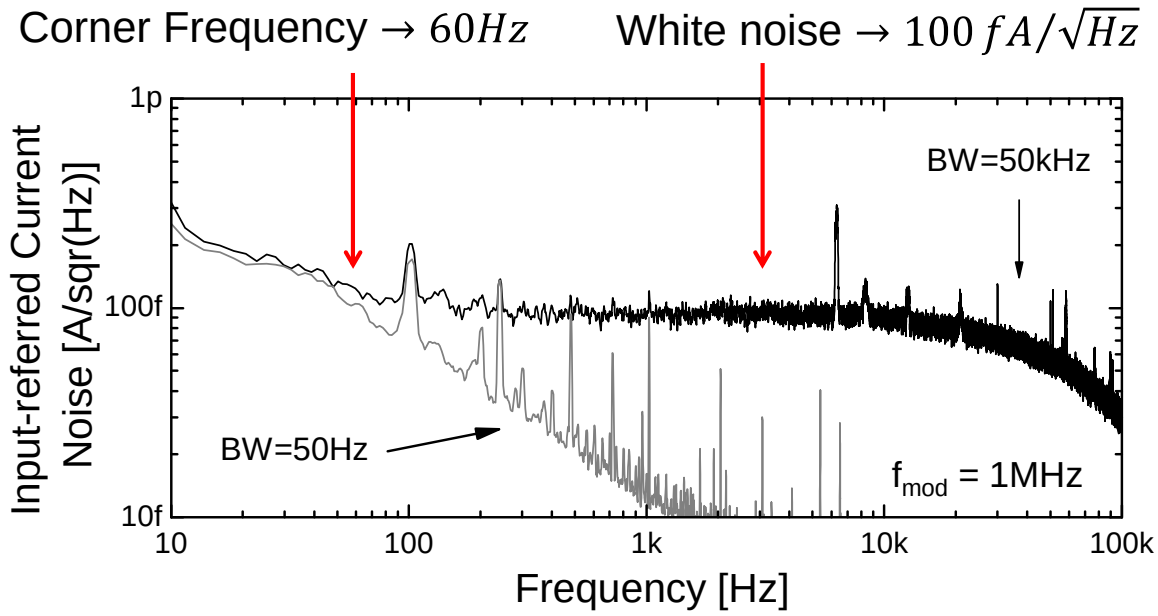
Corner Frequency → $60Hz$
White noise → $100\,fA/\sqrt{Hz}$
Input-referred Current Noise [A/sqr(Hz)]
1p
100f
10f
10
100
1k
10k
100k
Frequency [Hz]
BW=50kHz
BW=50Hz
f_{mod} = 1MHz

Figure 15

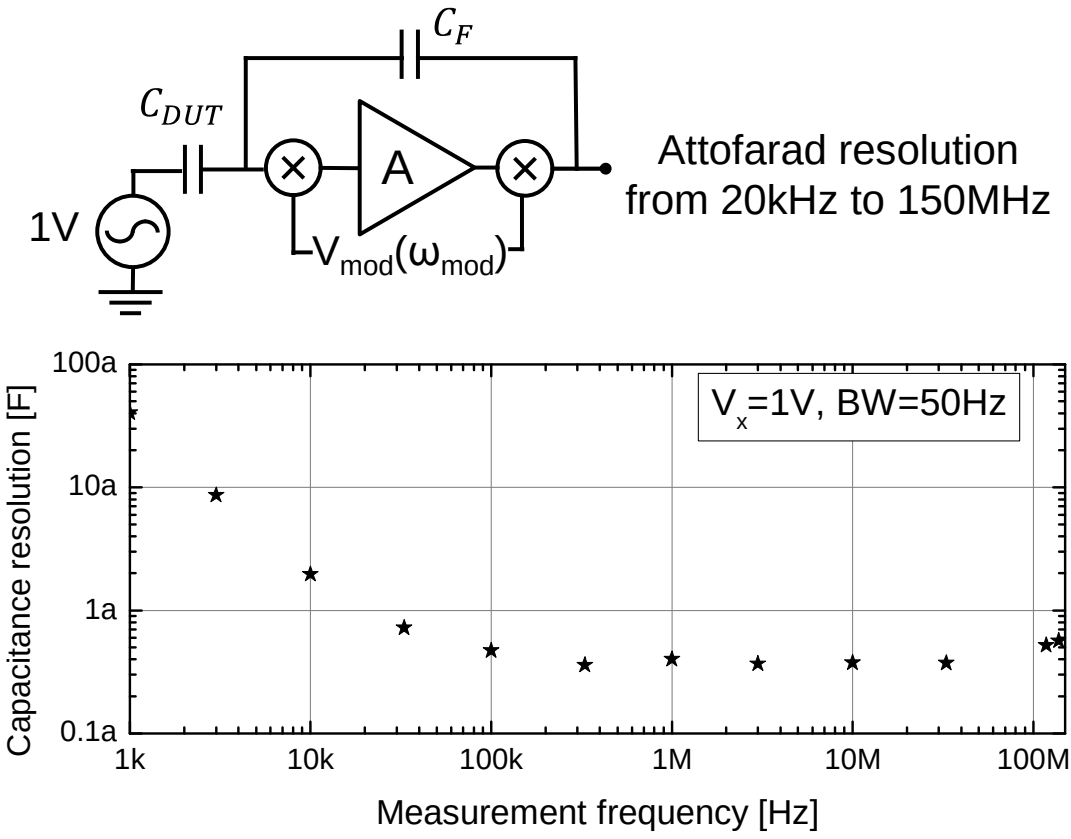

Figure 16

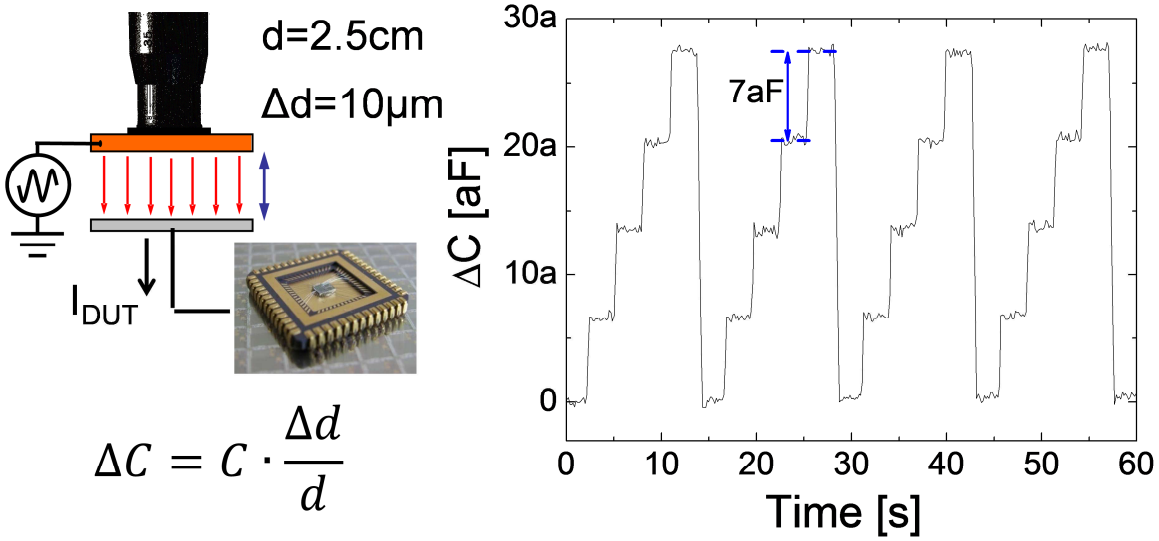

Figure 17

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF THE ART

	[5]	[6]	[7]	[8]	This work	Agilent 4294A
Structure	Multiplyng ADC	Heterodyne conversion	Coherent detection	Coherent detection	Mod/dem	Mod/dem coupled to a vector ratio detector
Frequency range	0.1Hz - 10kHz	10Hz – 100kHz	10Hz – 50MHz	100Hz – 2MHz	1kHz -150MHz	40Hz -110MHz
Channel count	16	1	100	1	1	1
DC current range (max. resolution)	100pA	200pA	25mA	10nA	60nA	Up to 20mA
Capacitance resolution (V_x=1V, BW= 10Hz)	5.1aF* (10kHz)	13aF* (2kHz)	-	0.25aF (10kHz)	2aF (10kHz)	250aF (10kHz)
	-	-	6.4aF* (2.5MHz)	0.05aF (2.5MHz)	0.35aF (2.5MHz)	8aF (2.5MHz)
	-	-	-	-	0.6aF (150MHz)	11aF (f=110MHz)
Process	0.13μm	0.18 μm	0.35 μm	0.35 μm	0.35 μm	-
Supply	1.2V	1.8V	3.3V	3V	3V	-
Chip area	1.68 mm^2	0.48mm^2	4 mm^2	0.5 mm^2	1.6 mm^2	-
Power consumption	1.8mW	144uW	84.8mW	60mW	112.5mW	-
Features	Low-power & multichannel	Low-power	Wide bandwidth & multichannel	High sensitivity	High sensitivity & wide bandwidth	Bench-top Instrument

* Estimated from the parameters given in the paper

Table of figures:

17 Tracking with time of a 7aF steps on a 15fF capacitance. Applied voltage V_x=1V, f_s=1MHz, BW=10Hz.