Introduction to the Special Issue on the 2014 IEEE International Solid-State Circuits Conference (ISSCC)

I. Introduction

THIS special issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is dedicated to select papers taken from the Analog, Data Converter, RF, Wireless and Wireline Communications sessions at the IEEE International Solid-State Circuits Conference (ISSCC) in San Francisco, CA, USA, held in February 2014. As always, selecting a subset of papers from these high quality sessions proved to be a difficult task. We hope, however, that the papers included in this issue are representative of the key innovations seen at the conference.

II. Analog Papers

Analog techniques cover diversified classes of applications, including an aF-resolution impedance analyzer circuitry, a sub-1 V filter with nm-CMOS switched-mode amplifier, a highly reconfigurable switched capacitor, as well as highly efficient inductive buck converters and nW power harvesters. All the papers with innovative circuits achieve state-of-the-art performance.

The first paper, by Bianchi *et al.* from Politecnico di Milano, describes an impedance analyzer chip for an impedance spectroscopy with a capacitance resolution as small as 0.4 aF in the 100 kHz–150 MHz range. The chip was implemented in 0.35 μm CMOS. It works from 1 kHz up to 150 MHz, independently on an input capacitance value up to about 100 pF, and provides two direct DC outputs proportional to the real and imaginary components of the target admittance, eliminating the need for an external lock-in structure or a filter.

The second paper, by Vigraham *et al.* from Columbia University, demonstrates a very low-voltage 4th-order 70 MHz continuous time active-RC Butterworth filter, achieving 55.8 dB peak SNDR at a full-scale differential voltage of 873 mV with a 0.6 V supply. The circuit is implemented in 65 nm CMOS. The switched-mode operational amplifiers are proposed as a new class of feedback amplifier and leverage the faster switching speeds of nanoscale CMOS to realize high-linearity feedback amplifiers.

The third paper, by Salem *et al.* from the University of California at San Diego, proposes a recursive switched capacitor (SC) convertor with the dynamical reconfiguration among $2^N - 1$ ratios. The converter is implemented in 0.25 μm CMOS. A 4 bit demonstrator achieves a wide output voltage range from 0.04 to 2.16 V, which is 40.4% larger than a conventional 3-ratio SC converter. It also demonstrates a peak efficiency of 85.8% from a 2.5 V input supply.

The fourth paper, by Cheng *et al.* from the Hong Kong University of Science and Technology, describes a voltage-mode controlled buck converter, featuring a high-accuracy delay-compensated ramp generator and a differential difference amplifier based type-III compensator. The chip was fabricated in 0.13 μm CMOS. It achieves the wide duty-cycle ranges of 0.75 and 0.59 when switching at 10 MHz and 30 MHz with peak efficiencies of 91.8% and 86.6%, respectively, and a maximum output power of 3.6 W at 2.4 V.

The fifth paper, by Jung *et al.* from the University of Michigan, Ann Arbor, reports a fully integrated energy harvester from a solar cell. The chip was fabricated in 0.18 μm CMOS. A proposed self-oscillating switched capacitor DC-DC voltage doubler $>$70% efficiency across a 1 nA to 0.35 mA output current range with the low idle power consumption of 170 pW, and is cascaded for a configurable conversion ratio from 9$\times$ to 23$\times$. The harvester delivers 5 nW–5 μW output power with $>$40% efficiency and has an idle power consumption $<$3 nW.

The sixth paper, by Bandyopadhyay *et al.*, proposes a nanoWatt power management unit (PMU) for an autonomous wireless sensor that sustains itself by harvesting energy from the endocochlear potential inside the mammalian ear. The circuits were implemented in 0.18 μm CMOS. The chip features a pW charge pump and a nW boost converter and implements a cold start. The PMU works under a system power budget of 1.1 nW to 6.25 nW with a quiescent power of 544 pW.

III. Data Converter Papers

Seven state-of-the-art data converter papers have been selected for this special issue and span a broad range of architectures and techniques, such as SAR, pipelined architectures, interleaving, and delta-sigma modulation. The sampling speeds range spans from 16 kHz to 20 GHz and the converters have been implemented in process technologies ranging from 28 nm to 0.18 μm CMOS. The designs aim for different performance targets which are ultra low-power, state-of-the-art power efficiency, high dynamic range, high linearity, and high speed.

The first paper, by Yaul *et al.* from MIT, presents a 10 bit LSB-first successive approximation algorithm. The energy per conversion and number of bitcycles per conversion used by this algorithm both scale logarithmically with the activity of the input signal, such that an N-bit conversion uses between 2 and $2N + 1$ bitcycles, compared to N for a conventional binary SAR. The SAR design operates at 0.6 V and achieves 9.73 bits at 16 kHz rate and an input signal dependent FoM between 3.5 and 20 fJ/conversion-step.

The next paper, by van der Goes *et al.* from Broadcom and Wolfson Microelectronics, shows a low-power 2$\times$ interleaved

pipelined SAR ADC. The key aspects in achieving the excellent power efficiency include the ADC architecture, integrator-based amplifiers used for noise-filtering, the finite settling of the reference voltage during the SAR conversion, and the modified DAC switching scheme to reduce the DAC switching energy. The ADC achieves a peak SNDR of 68 dB at 80 Ms/s with 1.5 mW power. The FoM is 9.1 fJ/conversion-step.

The next paper, by Lee *et al.* from MIT, shows a time-interleaved SAR ADC with background timing skew calibration. A full-speed flash ADC shared among 8 SAR ADC channels provides MSBs to the SAR ADCs in one cycle. The flash ADC is also used as a reference of timing skew calibration. Measurements of the prototype ADC show 51.4 dB SNDR at 1 GS/s with 18.9 mW and a FoM of 62.3 fJ/conversion-step.

Ali *et al.* from Analog Devices show a 14 bit 1 GS/s RF sampling pipelined ADC. The ADC utilizes correlation-based background calibration for correction of inter-stage gain, settling and memory errors, input distortion cancellation, non-linear charge injection compensation and dithering. With a 140 MHz and 2 Vpp input signal, the SNR is 69 dB and the SFDR is 86 dB at 1.2 W power consumption.

In the following paper, by Dong *et al.* from Analog Devices and the University of Toronto, a 0–3 multi-stage noise-shaping ADC is presented. A 17-level flash ADC is utilized to perform the coarse quantization and a third-order 7-level continuous-time delta-sigma back-end digitizes the residue error of the front-end. Clocked at 3.2 GHz, the ADC achieves a dynamic range of 88 dB over 53 MHz signal bandwidth with a power consumption of 235 mW and a Schreier FoM of 171.6 dB.

The next paper, by McMahill *et al.* from Maxim Integrated, demonstrates a 4.6 Gsps 14 bit DAC in a 160 channel QAM modulator for cable headend systems. The key techniques to achieve the performance level of the DAC are an interleaved architecture, an interleaving circuit for segment and interleave retiming as well as digital pre-distortion. With a 500 MHz input signal the DAC demonstrates an SFDR of 69 dBc and IMD of -79 dBc at 2.3 W.

The final paper, by Chen *et al.* from Carnegie Mellon University, describes a 20 GS/s 6 bit time-interleaved ADC in 32 nm CMOS SOI technology. The ADC incorporates a time-to-digital converter to sense timing skew, and the randomness of process mismatch is exploited to compensate for the clock misalignment and dynamic offset errors of comparators. The ADC achieves an SNDR of 30.7 dB at Nyquist rate while consuming 69.5 mW with a FoM of 124 fJ/conversion-step.

IV. RF Papers

The seven RF papers selected for this special issue from three RF session of ISSCC 2014, present state-of-the-art designs in the area of RF power amplifier, mmW, and THz circuits, as well as frequency generation.

The first paper, by Kousai *et al.* from Toshiba, describes a polar amplifier in 130 nm CMOS, for 3G/4G applications with antenna load impedance detection. This circuit is followed by a low-loss impedance tuner with SOI switch. The impedance detection exploits a polar technique, in this way the antenna impedance is tuned in a vector fashion, this technique can operate with non-constant envelope signals. The peak output power of the PA chip is 30.8 dBm, at 1.95 GHz. For a VSWR of 2.5, the peak PAE is higher than 40% when tuning is enabled. The tuning efficiency at 6 dB back off increases from 30% to 40%. The tuner can cover a VSWR of about 6.

The second PA paper, by Oihsi *et al.* from Fujitsu, also for 3G/4G handsets, presents an Envelope Elimination and Restoration (EER) power amplifier, and fully integrated in 90 nm CMOS technology. To achieve accurate timing between the envelope and phase signals, a time aligner based on a delay-locked loop is integrated, which compensates the time mismatch. A novel envelope/phase generator is also implemented to generate the wide bandwidth signals. The output power is 28 dBm for WCDMA and 26 dBm for LTE. The measurements show a PAE and ACLR of 39% and -41 dBc for WCDMA, while for 20 MHz bandwidth LTE these figures are 32% and -33 dBc, respectively.

The third paper, by Giannini *et al.* from imec, reports the design of a 79 GHz continuous-wave radar transmitter, realized in 28 nm CMOS. The circuit's operations are based on the use of a sub-harmonically injection-locked oscillator, which locks on the 5th input harmonics, and on a side-lobe rejection baseband-mixer, that prevents the violation of the spectral mask. The 79 GHz carrier is modulated by a 2 Gsps pseudo-noise sequence, and the output power in a 4 GHz bandwidth is 11 dBm. The power consumption of the entire transmitter is 121 mW from the 0.9 V supply.

Pfeiffer *et al.* from the University of Wuppertal present a reconfigurable source-module for real-time THz imaging application, fabricated in a 130 nm SiGe BiCMOS technology. The module consists of an array of 16 source-pixels that operate incoherently. Each element includes an on-chip ring antenna and a two triple-push oscillator, locked at 180°. The total radiated power is about 1 mW, the average power of a source-pixel is 62.5 mW, and the EIRP per pixel is about 25 dBm. The chip consumes 2.5 W from a 2.4 V supply and 3.2 mW from a digital 1.2 V supply, respectively.

The fourth paper, by Chiang *et al.* from UC Irvine and UC Davis, describes the design of a 0.3 THz frequency synthesizer for imaging application, implemented in a 90 nm SiGe BiCMOS technology. The synthesizer is a PLL, having a 96 MHz reference, based on a triple-push VCO and of a Colpitts active varactor. While the third VCO harmonic is the synthesizer output, its fundamental is fed to the divider chain that adopts a three-phase injection scheme to achieve the desired tuning range. The synthesizer output power is -14 dBm at 290 GHz, with 8% tuning range and -82 dBc/Hz phase noise @1 MHz. The power dissipation is 376 mW.

The paper by Chang *et al.*, from National Taiwan University, presents a sub-sampling (divider-less) fractional-N PLL, realized in a 180 nm CMOS technology. To obtain fractional-N behavior, a digital pulse width modulator is employed to sample the VCO output, while the divider-less architecture limits the in-band noise. The synthesizer is locked to a 48 MHz reference and dissipates 17.3 mW while the integrated jitter over the 2.1–2.4 GHz tuning range varies between 266 fs and 400 fs. The in-band fractional spur is -48 dBc, and the in-band phase noise (at 50 kHz) is -112 dBc/Hz.

Finally, Yoo *et al.* from Chung-Ang University report the design of a direct digital frequency synthesizer clocked at 2 GHz, fabricated in a 55 nm CMOS technology. Several design techniques are employed to achieve the desired performance, in particular to reduce the power dissipation both in the phase accumulator and digital decoder, and improve the spectral purity. The synthesizer features 9 bit amplitude, and a minimum frequency step of 0.46 Hz for a 2 GHz clock. The minimum spurious-free dynamic range is 55 dBc, while the power dissipation is 130 mW.

V. Wireless Communication Papers

Six papers have been selected for this special issue from the Wireless Communication sessions. The first three papers address low-power applications like WBAN and Zigbee where state-of-the-art performance is achieved by employing current-reuse, phase-tracking and Q-enhancement techniques. The fourth paper presents a highly integrated 60 GHz CMOS chip-set with 16 RX and 16 TX paths. Finally, the last two papers focus on cellular applications and how to relax cellular front-end requirements by TX leakage cancellation and tunable channel selectivity at RF.

In the first paper, by Lin *et al.* from the University of Macau and Instituto Superior Technico, present a Zigbee receiver in 65 nm CMOS for the 433 to 960 MHz bands, achieving an 8.1 dB noise figure while consuming 1.15 mW. The receiver demonstrates new techniques for current reuse, and employs N-path feedback and downconversion to reuse the input LNA for both RF and baseband signals.

Liu *et al.* from imec present, in the second paper, a 2.4 GHz receiver in 65 nm CMOS employing a digital phase-tracking loop to perform direct phase-to-digital conversion. The receiver achieves -92 dBm sensitivity for 2 Mb/s signals in the IEEE 802.15.4 standard while consuming 2.4 mW.

In the third paper, Cheng *et al.* from Oregon State University and Fudan University, present a 2.4 to 2.7 GHz WBAN receiver in 65 nm CMOS, able to demodulate 971 kb/s signals with -90 dBm sensitivity while consuming 1.05 mW. The receiver combines a Q-enhanced LNA with sub-sampling to provide low-power downconversion with minimal noise folding.

The fourth paper, by Boers *et al.* from Broadcom, presents a highly integrated 60 GHz 802.11ad, 16×16 phased-antenna-array transceiver chipset with polarization diversity in 40 nm CMOS, including RF/PHY and MAC. It supports up to 64-QAM modulation and throughput of over 3.5 Gb/s at 10 m. Radio power consumption is 960/1190 mW (RX/TX), while a single coaxial cable is used to interface between chips to ease integration to PC platforms.

Zhou *et al.* from Columbia University present, in the fifth paper, a blocker-resilient software-defined receiver in 65 nm CMOS with a low-noise active TX leakage cancellation scheme. This receiver can cancel up to $+2$ dBm peak TX leakage at the RX input, enabling an effective IIP 3 of $+30$ dBm (enhancement of 18 dB) with an associated increase in NF <0.5 dB.

In the sixth of the Wireless papers, Park and Razavi from UCLA introduce a wideband receiver concept based on Miller bandpass N-path filters around the LNA in 65 nm CMOS. The receiver provides an attenuation of 15 dB in the middle of the alternate adjacent channel and a noise figure of 5.4 dB with a 0 dBm blocker at 23 MHz offset.

VI. Wireline Communication Papers

The first four of the six Wireline Communication papers selected for the Special Issue describe design techniques for high-speed transceivers for a wide range of applications ranging from backplanes to 100 Gb Ethernet. The fifth paper describes a continuous time equalizer for dispersion compensation and the final paper presents a full-duplex 1000Base-T line driver.

The first paper is by Musah *et al.* from Intel. They describe the design of high-density interconnect consisting of 8-lane bidirectional links in 22 nm CMOS technology. Optimal power performance was achieved across a wide range of data rates (4 Gb/s–32 Gb/s) using bundling of lanes, supply voltage scaling, power gating, and transmit swing control techniques. Elaborate equalization is performed to overcome more than 25 dB channel loss.

Kimura *et al.* from LSI Corporation present a 28 Gb/s multi-standard SerDes in 28 nm CMOS. They employ a trans-impedance-amplifier-based continuous-time equalizer along with 14-tap decision feedback equalizer (DFE) to overcome more than 34 dB channel loss while consuming 560 mW/lane of power.

Balan *et al.* from nVIDIA Corporation describe a 15–22 Gb/s serial link transceiver in 28 nm CMOS. They employ programmable 2-tap pre-emphasis on the transmit side along with a trans-admittance–trans-impedance single-stage linear equalizer and IIR-DFE on the receive side to compensate for more than 20 dB of channel loss. The 16-lane transceiver occupies 1.66 mm$\times$1.6 mm of area and achieves an excellent energy efficiency of 6.5 mW/Gb/s at 20 Gb/s data rate.

Singh *et al.* from Broadcom Corporation presents a 2×28 Gb/s transceiver for a 100GbE Gearbox PHY in 40 nm CMOS. Power consumption is reduced using global resonant clock distribution network implemented using programmable distributed on-chip inductors. They report excellent jitter performance of only 202 $\mathrm{fs_{rms}}$ at the transmitter output.

Mammei *et al.* from the University of Pavia and STMicroelectronics report a 10 Gb/s–25 Gb/s 7-tap continuous-time FIR equalizer for dispersion compensation in multi-mode fiber links. The delay line is implemented using a cascade of active all-pass stages that are optimized for linearity and noise. The prototype equalizer fabricated in a 28 nm LP CMOS occupies only 0.085 $\mathrm{mm^2}$.

Pan *et al.* from Broadcom Corporation present the final paper in this section. They describe a full-duplex line driver in 28 nm CMOS that maximizes the power efficiency using a class-AB push-pull output stage. By merging transmission, reception, and termination they eliminate the hybrid while still meeting 1000BASE-T and 100BASE-TX compliance tests.

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