(54) **Title:** RANDOM NUMBER GENERATION FROM MULTIPLE MEMORY STATES

(57) **Abstract:** The present invention relates to a device (1) for generating random numbers, comprising a pair of memristors (P,Q). The pair of memristors comprises a first and a second memristor, each memristor of the pair in turn comprises a top electrode (TE), a bottom electrode (BE) and an intermediate layer (SL) adapted to switch resistance in response to predetermined voltage values applied between the top electrode and the bottom electrode. Each memristor (P, Q) is operatively connected to an output terminal by means of its bottom electrode. A control logic is connected to the memristors for applying suitable voltages necessary to determine a change of resistance in at least one memristor of the pair. In detail, the control logic is configured to: fix the voltage of the output terminal to a predetermined value and apply said transition voltage to cause a change of resistance in at least one memristor of the pair, leave the voltage at said output terminal floating and apply to the top electrodes of said first and second memristor two read voltages having opposite sign and amplitude lower than said transition voltage.

RANDOM NUMBER GENERATION FROM MULTIPLE MEMORY STATES

DESCRIPTION

TECHNICAL FIELD

The present invention relates to electronic methods and devices for generating random numbers.

The invention finds a preferred application in systems-on-chip requiring generation of random numbers for cryptography applications or containing a hardware signature for the purpose of security of transmitted information.

Generally the invention relates to a device according to the preamble of claim 1 and to a relevant method for generating random numbers.

PRIOR ART

Random number generation is essential for generating random cryptography keys for secure transmission protocols [1]. Pervasiveness of Internet-based communication and the need of protecting data from eavesdropping lead to the need for compact random number generation circuits (RNG), able to generate true random numbers with high entropy quality and high *throughput*. In order to generate true random numbers, that do not rely on deterministic algorithms and are totally unpredictable, it is important to identify a convenient on-chip entropy source and to design the corresponding circuit for generating the random bit stream with high throughput and stability. Previous approaches for generating true random numbers provide as the source the random telegraph noise (RTN) in dielectrics [2] or in resistive-switching memories (RRAM) [3]. The RTN appears as a random fluctuation of current, or resistance, between two or more levels, resulting from the random charging/discharging of bistable defects [4]. However, RTN is difficult to control in terms of amplitude and frequency, thus increasing the need for dedicated techniques for exploiting RTN. Moreover RTN has been shown to be unstable in RRAMs, where the current fluctuation at a given bias can show unpredictable onset and

interruption [5]. Other schemes, based on physical fluctuation phenomena, therefore are under investigation to obtain efficient and stable random number generation.

Recently novel RNG concepts based on the switching variability in low-voltage memory technologies, such as spin transfer torque (STT) magnetic memories MRAM ([6], [7]) and RRAM ([8], [9]) have been proposed.

The switching statistical variability in RRAM was similarly applied to develop physical unclonable functions (PUF) [10] and to improve learning in neuromorphic circuits [11].

For generating random numbers it is possible to exploit the stochastic variation of a switching parameter, such as the voltage V_{set} necessary for setting the transition from high to low resistance [12]. Application of a voltage close to the median value of the distribution of V_{set} statistically results in a transition only in a random fraction of attempts. An important problem in this approach, however, is the need for a careful tracking of the applied voltage, which must be exactly centered in the median value of the V_{set} distribution to guarantee a perfect balance between 0 and 1 [12]. For this aim, real-time voltage tracking techniques must be used for compensating 0 and 1 probabilities [7].

Random number generating circuits using memristors are described in US 8,680,906 B1, EP 2 933 720 A1, KR101566949 and US20140268994.

Patent applications EP2933720, KR101566949 and US20140268994 use a memristor by employing stochastic writing to obtain random functions. However such solutions use only one memristor, which makes the uniform generation of random bits more complicated and subjected to an accurate calibration of the generating algorithm.

The patent US 8,680,906, to United States Air Force, uses two memristors in series arrangement. Memristors initially are prepared in a low resistance state (LRS), then a voltage is applied to the ends of the series connection such

to cause the random reset of one of the two memristors. Such operation causes the random reset only in one memristor, where all the applied voltage is substantially concentrated, this leading to a rapid degeneration of memristors.

Other solutions using two memristors are described in [13] and [14].

[13] and [14] disclose circuits for implementing a PUF, where two RRAM cells (in HRS) are connected to two respective inputs of a comparator that generates a output bit depending on the resistance difference of the two cells. [13] also discloses that, to stabilize the output of the comparator, the cell having the lower resistance can be set in LRS, thus increasing the difference between resistances. The drawback of such solution is the need for a suitable circuit for programming the state of the memristors, downstream the reading and the comparison of resistances in the 2 memristors.

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OBJECTS AND SUMMARY OF THE INVENTION

It is the object of the present invention to overcome prior art drawbacks.

Particularly it is the object of the present invention to provide a method and a circuit for generating random numbers based on memristors that does not need probability tracking techniques.

These and further objects of the present invention are achieved by a device and a method embodying the characteristics of the annexed claims, which are an integral part of the present description.

Generally the device for generating random numbers comprises a pair of memristors. The pair of memristors comprises a first and a second memristor, each memristor of the pair in turn comprising a top electrode, a bottom electrode and an intermediate layer adapted to switch resistance in response to predetermined voltage values applied between the top electrode and the bottom electrode. Each memristor is operatively connected to an output terminal by its bottom electrode. A control logic is connected to memristors for applying suitable voltages necessary for determining a change of resistance in at least one of the memristors of the pair.

In detail the control logic is configured to:

- fix the voltage of the output terminal to a predetermined value and apply said transition voltage to cause a change of resistance in at least one memristor of the pair,

- leave the voltage at said output terminal floating and apply to the top

terminals of the first and second memristors two read voltages having opposite sign and amplitude lower than said transition voltage.

The particular connection of the two memristors, that actually are controlled in parallel, allows the resistance of the memristors to be changed without applying high voltages. By using the randomness of the resistance value of the memristor after the application of a SET or RESET voltage, it is possible to generate at the output terminal a voltage that can be positive or negative with a probability substantially of 50%, therefore it is possible to generate a random number (1 or 0) by associating it with the value of the voltage present at the output terminal.

The invention relates also to methods for generating random numbers that use the particular arrangement of the memristors mentioned above.

Further objects and advantages of the present invention will be more clear from the detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described here below with reference to not limitative examples, provided by way of example and not as a limitation in the annexed drawings. These drawings show different aspects and embodiments of the present invention and, where appropriate, reference numerals showing like structures, components, materials and/or elements in different figures are denoted by like reference numerals.

Figure 1 is a device for generating random numbers (RNG) and the sequence of voltage pulses that have to be applied for RNG.

Figure 2 is a memristor and its voltage-current characteristics.

Figure 3 is a flow chart of a RNG method.

Figure 4 is a variant of the device of figure 1 and the sequence of voltage pulses that have to be applied for RNG.

Figure 5 schematically is a cell of a RRAM.

Figure 6 is the experimental results obtained by a RNG cycle implemented by

the device of figure 4.

Figure 7 is a sequence of voltage pulses that, once applied to the device of figure 4, allow a different RNG method to be implemented.

Figure 8 is the experimental results obtained by a RNG cycle implemented by the device of figure 4 and the method of figure 7.

DETAILED DESCRIPTION OF THE INVENTION

While the invention is susceptible of various modifications and alternative constructions, some disclosed embodiments are shown in the drawings and will be described in details herein below. It should be understood, however, that there is no intention to limit the invention to the specific disclosed embodiment but, on the contrary, the invention intends to cover all the modifications, alternative constructions and equivalents that fall within the scope of the invention as defined in the claims.

The use of "for example", "etc.", "or" denotes non-exclusive alternatives without limitation, unless otherwise noted. The use of "comprises" means "comprises, but not limited to", unless otherwise noted.

Figure 1(a) shows a device 1 for generating random numbers, comprising a generating section 10 and a control logic 11 (for example a microprocessor or a FPGA) generating the necessary signals for controlling the generating section 10.

The generating section comprises two memristors (P and Q) connected in parallel to the input terminal of a comparator 12 whose other input terminal is grounded.

The word memristor means a variable resistance device whose resistance value can be changed by applying a suitable voltage at its ends.

An example of a memristor is shown in figure 2 (a), it comprises a switching layer (SL) of HfO_2 (or another oxide) with a TiN bottom electrode (BE) and a Ti top electrode (TE), that acts as oxygen exchange layer for generating defects at TE side.

Such as shown in figure 2b, the application of a positive voltage (that is from BE to TE) V_{set} at the ends of the memristor, causes SET transition, where switching occurs from high resistance state (HRS) to low resistance state (LRS), while the application of a negative voltage V_{reset} causes RESET transition from LRS to HRS.   Each memristor P and Q therefore has a variable resistance that can be programmed by causing a SET or RESET transition.

In the example described here, the memristors have a SET voltage V_{SET} =1,5V and a RESET voltage V_{RESET} = -0,9V for a typical ramp rate of 10^3 V/s. A compliance current (limitation) IC = 50 µA was used during the SET transition by applying a relatively low gate voltage. A maximum negative voltage V_{stop} of 1,5V is applied during the reset sweep.

With reference again to the device of figure 1(a), for random number generation, the control logic 11 applies voltage signals to the inputs of the generating section 10 according to a method providing three steps that are cyclically repeated and are shown herein below with reference to figure 1b and figure 3.

Firstly the method provides to apply (301) a positive voltage to the top electrode (TE) of P and Q to cause SET transition. In the example of figure 1 the control logic 11 keeps to ground the voltage V_{out} measured at the positive input terminal of the comparator 12 and applies to the ends of the memristors P and Q a triangular voltage pulse (V_P, V_Q) of 1 ms in duration and amplitude higher than V_{SET}.

Then, step 302, a negative voltage V_{RESET} is applied to top electrodes of P and Q to cause the RESET transition in both the variable resistances R_P and R_Q. Also in this case, for the reset voltage a triangular pulse is applied of 1 ms in duration and an amplitude higher than (in absolute value) V_{RESET}.

Finally, step 303, the step reading the random bit is performed. In this step the control logic 11 is disconnected from the input terminal of the

comparator to which memristors P and Q are connected and applies to the top electrode TE of the transistor P a voltage $V_P = +V_{Read}$ and, to the electrode TE of Q a voltage $V_Q = -V_{Read}$, where $2V_{Read} < V_{Set}$. V_{Read} can be for example equal to 0,3 V, therefore it is not enough for causing a change of resistance in the memristors. In the example of figure 1(b), also for the reading a triangular pulse is applied with 1 ms in duration and amplitude V_{read}.

Now the input node of the comparator 12 has a voltage that will be slightly positive or negative depending on whether the resistance of P is smaller or greater than the resistance of Q, respectively. Therefore it is possible to assign a logic value of 1 or 0 to the value of the measured voltage of V_{OUT}.

This method uses the characteristic of memristors that, statistically, are never with the same HRS resistance after SET and RESET process. As a result of the relatively high statistical variation of HRS resistance, V_{out} randomly changes from one to another reading cycle, thus acting as an output bit value in the RNG method. In this arrangement, the variation in HRS resistance acts as entropy source for the RNG method.

The output of the analog comparator (12) is used to digitally regenerate V_{out}.

Figure 4 (a) shows a variant of the circuit of figure 1, that uses two cells 13 and 14 of a RRAM with 1T1R structure.

Each cell, shown in figure 4(b), comprises a memristor of the type described above with reference to figure 2(a), connected to the drain of a cell transistor 20, for example a MOSFET.

The source of the cell transistor 20 is connected to the positive input of the comparator 12, thus by applying a sufficiently high gate voltage V_{G2} it is possible to short circuit the transistor and to connect the positive input of the comparator 12 to the bottom electrode BE of each memristor P, Q.

In the device of figure 4, the generating section 10 comprises a transistor 15, particularly a MOSFET, whose drain is connected to the positive electrode of the comparator 12 and whose source is grounded.

In order to implement the method of figure 3, the control logic 11 controls voltages V_P, V_Q, V_{G1} and V_{G2} such as shown in figure 4 (b).

During SET phase, V_{G1} is kept high (for example equal to the power voltage of the circuit V_{DD}) in order to ground the voltage V_{OUT}. Cell transistors 20 are switched on by applying a voltage V_{G2} just above threshold, while to the top electrodes TE of P and Q a positive voltage equal to or higher than voltage V_{SET} is applied. In the example shown here V_P and V_Q are brought to the power voltage VDD, higher than threshold one. Both the memristors therefore perform a SET transition and switch to low resistance value (LRS). In the example described herein triangular voltage pulses of 1 ms in duration are applied to the electrodes TE of P and Q, however it is possible to use different waveforms (e.g. rectangular or parabolic) and of different duration.

Then during the reset phase the transistor 15 is short circuited, meaning that V_{G1} is kept high (for example equal to the power voltage of the circuit V_{DD}) in order to ground the voltage V_{OUT}. A similar control is performed on V_{G2} to be sure that the drain source voltage of the transistor is as near as possible to zero and that all the voltage V_P and V_Q (negative and equal, or in higher modulus, to V_{RESET}) drops at the ends of the respective memristor P and Q, that therefore switches to high resistance state (HRS).

During reading, the transistor 15 is switched off ($V_{G1}=0$), such to leave its drain voltage as floating. On the contrary V_{G2} is kept high, to be sure that substantially all voltages V_P and V_Q applied to positive electrodes of P and Q are between such electrodes and the positive input of the comparator 12. As said above with reference to figure 3, in this step the voltages V_P and V_Q are of equal modulus and opposite sign: V_P = Vread and V_Q=-Vread. The voltage V_{OUT} therefore will take a positive or negative sign depending on the value of the resistances of P and Q; the corresponding voltage V_{OUT2} therefore will be equal to the power voltage VDD or to ground voltage, thus determining a bit with a logic value 1 or 0.

In order to demonstrate the efficiency of the device and of the RNG method described above, figure 6 shows the results of some tests performed with the circuit of figure 4(a).

Figure 6(a) shows the cumulative distribution of resistance R_P of P and of resistance R_Q of Q, measured after SET and RESET transitions.

RNG method was tested during 1000 cycles, this provides a sufficient statistical accuracy with a negligible degradation of the device.

Distributions R_P and R_Q are almost identical both in LRS and HRS, which is the key to reach an unbiased RNG of true random numbers.

Figure 6 (b) shows experimental and calculated distributions of V_{out} obtained during reading. The measured distribution of V_{out} follows a bimodal form with probability transition of 50%.

As it can be observed still in figure 6(b), the bimodal distribution was improved by introducing in the circuit of figure 4(a) an analog comparator (12), that allows a V_{out2} to be equally distributed on values $+V_{max}$ (corresponding to a logic 1) and $-V_{max}$ (corresponding to a logic 0).

The comparator 12 can be replaced by one or more integrated CMOS inverters in an integrated circuit to reduce the area occupied on the chip.

Figure 6 (c) shows voltages V_{out} and V_{out2} measured during 1000 cycles of the RNG method, while figure 6 (d) shows the corresponding probability density function (PDF) of V_{out} and V_{out2}.

Figure 7 shows a sequence of voltage pulses alternative to the sequence of figure 4, that allows, by the same circuit of figure 4(a), a RNG method alternative to that of figure 3 to be implemented.

According to this method, a triangular voltage pulse of 1 ms in duration and with a value higher than (in absolute value) V_{Reset} is initially applied to top electrodes (TE) of P and Q. During such step the transistors 15 and 20 are kept switched on with a gate voltage high enough to short circuit drain and source (e.g. $V_{G1}=V_{G2}=V_{DD}>>V_{DS}$), such to bring V_{out} substantially to ground

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and to cause all the voltage V_P and V_Q to fall on memristors P and Q which therefore switch to HRS.

Then a voltage higher than V_{SET} (for example VDD) is applied to memristors P and Q which causes a random transition of P or Q to the LRS. In this step the transistor 15 is kept switched on, but with a gate voltage V_{G1} slightly higher than threshold, such to operate as a resistance to ground for P and Q. Transistors 20 on the contrary are kept switched on with V_{G2} equal to VDD, such to be short circuited. During this step, one of the two transistors switches to LRS; when this happens the potential of its bottom electrode BE and therefore also of V_{OUT}, follows and gets near VDD, reducing voltage at the ends of both the memristors and thus preventing the other memristor from performing SET transition and from switching to LRS. Thus only one of the two memristors carries out the transition to LRS, the one of the two memristors that due to statistical fluctuations has the smallest transition voltage Vset.

Finally the RNG cycle provides to switch off the transistor 15 ($V_{G1}=0$) and to read output voltage V_{OUT} (or V_{OUT2}) as shown above for the device of figure 1 (a), that is by applying a differential voltage (equal to $2V_{READ}$ in this embodiment) between the electrodes TE of P and Q. The voltage V_{out} will have a positive or negative value depending on which of the two memristors has carried out the SET transition.

Since SET transition in P and Q is random, there is no need for any probability tracking circuit, since SET transition is naturally present in a single memristor at each cycle.

Fig. 8 (a) shows the bimodal distribution of resistance R resulting for P and Q, which exhibits a bimodal distribution with a HRS/LRS transition at 50%. Calculations were carried out by randomly moving 50% of the samples from the HRS distribution to LRS distribution. Fig. 8 (b) shows the correlation plot of R_Q as a function of R_P, indicating complementary states, that is P is always

in HRS if Q is in LRS and vice versa. Fig. 8 (c) shows the cumulative distribution of V_{out} and V_{out2}, the latter being the regenerated output of the CMP. Nice bimodal distributions are noted with smooth and abrupt transitions for V_{out} and V_{out2} respectively. Figures 8 (d) and 8 (e) show V_{out} and V_{out2} as a function of the RNG cycle (d) and the corresponding probability density function PDF (e). Calculations were performed for figures 8 (c) and (e), showing a good agreement with data.

In the light of the above mentioned examples it is clear how the invention allows the above objects to be achieved.

It is also clear that the person skilled in the art can make changes to the above examples without for this reason departing from the scope of protection as it results from the annexed claims.

For example, voltage pulses applied to top electrodes (TE) of P and Q can have any shape and duration, for example can have a rectangular or parabolic shape.

Still, the division of the device in the two blocks composed of the generating section 10 and the control logic 11, has to be intended by way of example and not as a limitation. For example the transistor 15 of figures 4 and 7 can be a part of the circuit of the control logic 11.

It has to be noted that teaching of the invention can be applied also to all methods intended to increase entropy of the sequence of random numbers produced by the device 1 of figures 1 and 4. An entropy increase method is any post-processing of raw data, for example a selection of bits according to the Von Neumann algorithm, or any other algorithm intended to modify the sequence or to mix it with another entropy source.

Moreover teaching of the invention can be also applied to all methods intended to pre-condition random number generation devices such to obtain a better functionality (for example a higher cycling life) or for a better generation of random numbers.

It has also to be noted that the memristors that can be used in the device 1 can be of different types; for example all memristors able to change their resistance as a response to the application of pulses are suitable. In the type of usable memristors for example we have:

- Phase change memory devices (Phase Change Memory, PCM);
- Unipolar resistive switching devices (unipolar RRAM);
- Magnetic tunnel junction devices (Magneto-Tunnel Junction, MTJ), such as for example spin-transfer torque memories (STT-RAM) and spin-orbit torque memories (SOT-RAM);
- Ferromagnetic tunnel junction memories (Ferroelectric Tunnel Junction, FTJ).

According to another embodiment, memristors P and Q of the device 1 can be of different types, such as the case when, for example, one of the two memristors is a bipolar RRAM and the other memristor is a unipolar RRAM. With reference to the memristors of the device, 1, memristor devices wherein resistance is modified for a limited time can be also used, such as for example threshold switching devices where LRS spontaneously switches to HRS after SET transition. Such devices for example can contain materials such as:

- insulator-metal transition metal oxides, such as vanadium oxide and niobium oxide;
- amorphous chalcogenides, such as for example some alloys of the group TeAsGeSi;
- insulators such as silicon oxide, or silicon nitride, combined or doped with metals, such as Ag, that exhibit spontaneous transitions from LRS to HRS after set operation.

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CLAIMS

1. Device (1) for generating random numbers, comprising:

    - a pair of memristors (P,Q) comprising a first and a second memristor, each memristor of the pair comprising a top electrode (TE), a bottom electrode (BE) and an intermediate layer (SL) adapted to switch resistance in response to predetermined voltage values applied between the top electrode and the bottom electrode,

    - an output terminal operatively connected to said pair of memristors,

    - a control logic adapted to apply a transition voltage at the ends of each memristor in order to cause a change of resistance in the memristor,

    characterized in that

    each memristor is operatively connected to the output terminal by means of its bottom electrode,

    and in that the control logic is configured to:

    -   fix the voltage of the output terminal to a predetermined value and apply said transition voltage to cause a change of resistance in at least one memristor of the pair,

    -   leave the voltage at said output terminal floating and apply to the top electrodes of said first and second memristor two read voltages having opposite sign and amplitude lower than said transition voltage.

2. Device according to claim 1, wherein the transition voltage is a SET voltage such to cause a transition from high resistance to low resistance in said at least one memristor of the pair, and wherein the control logic is further configured to apply a RESET voltage to said pair of memristors such to cause a transition from low to high resistance in both the memristors of the pair, the control logic being adapted to apply said SET voltage after said RESET voltage.

3. Device according to claim 1, wherein the transition voltage is a RESET voltage such to cause a transition from low resistance to high resistance in both the memristors of the pair, and wherein the control logic is further configured to apply a SET voltage to said pair of memristors such to cause a transition from high to low resistance in at least one memristor of the pair, said SET voltage being applied before said RESET voltage.
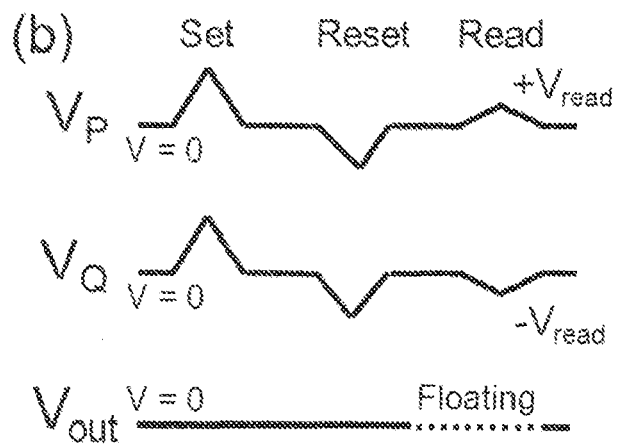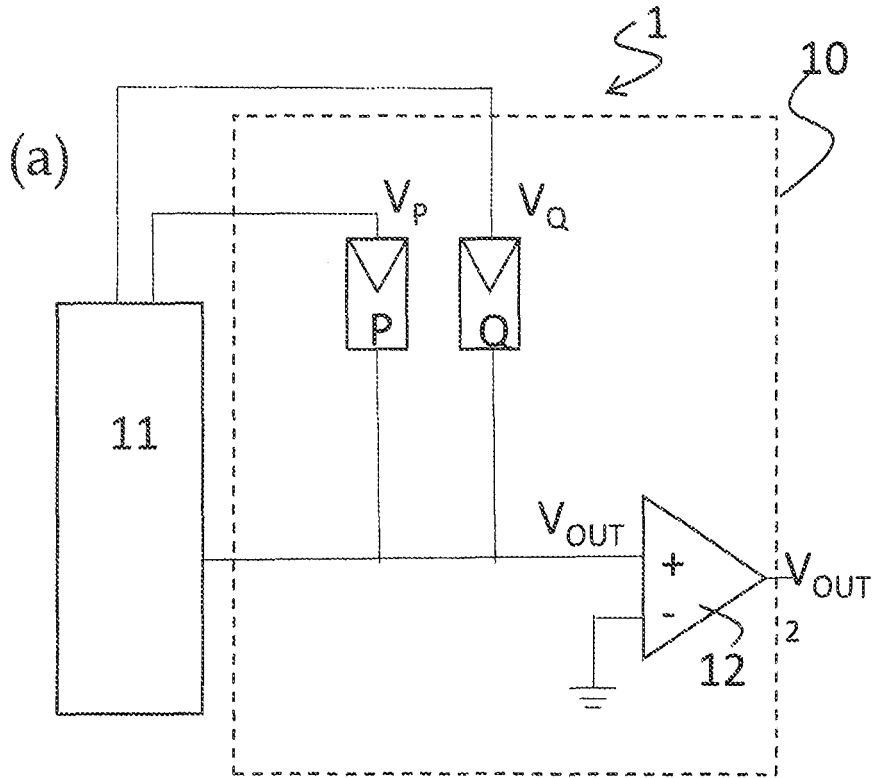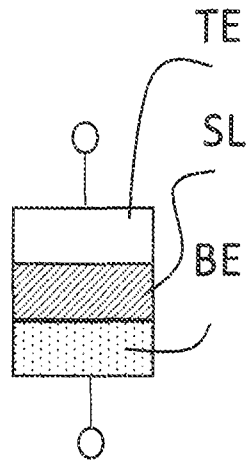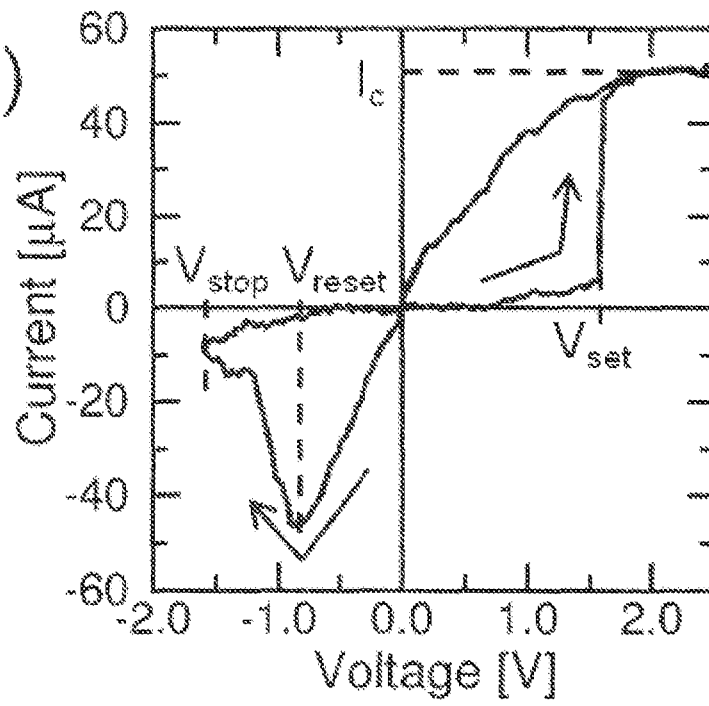
4. Device according to any of the previous claims, further comprising a comparator circuit comprising a first and a second input terminal, wherein the first input terminal is connected to the output terminal and wherein the second input terminal is grounded.

5. Device according to any of the previous claims, wherein the first and the second memristor are comprised in a respective cell of a RRAM, said respective cell comprising a memristor whose bottom electrode (BE) is connected to the drain of a cell transistor (20), said cell transistor (20) comprising a source electrode connected to the output terminal.

6. Device according to any of the previous claims, further comprising a pilot transistor (15) whose source electrode is grounded and whose drain electrode is connected to the output terminal, the control logic being operatively connected to the gate of the pilot transistor to command its switch on and/or switch off.

7. Method for generating random numbers, wherein a random number is generated by using a statistical variation of an electric resistance of at least one memristor of a pair of memristors, said pair of memristors (P,Q) comprising a first and a second memristor, each memristor of the pair comprising a top electrode (TE), a bottom electrode (BE) and an intermediate layer (SL) adapted to switch resistance in response to predetermined voltage values applied between the top electrode and the bottom electrode, the method providing to
   - cause a change of resistance in at least one memristor of the pair by

applying to said at least one memristor a transition voltage,

- read a voltage value at an output terminal operatively connected to said pair of memristors,

- associate a number to the voltage value of the output terminal,

characterized in that

each memristor of the pair is operatively connected to the output terminal by means of its bottom electrode,

and in that the method provides to:

- fix the voltage of the output terminal to a predetermined value and applying said transition voltage to cause a change of resistance in at least one memristor of the pair,

- leave the voltage at said output terminal floating and apply to the top electrodes of said first and second memristor two read voltages having opposite sign and amplitude lower than said transition voltage.

8. Method according to claim 7, wherein the transition voltage is a SET voltage such to cause a transition from high resistance to low resistance in said at least one memristor of the pair, and wherein the method further comprises the step of applying a RESET voltage to said pair of memristors such to cause a transition from low to high resistance in both the memristors of the pair, said SET voltage being applied after said RESET voltage.

9. Method according to claim 7, wherein the transition voltage is a RESET voltage such to cause a transition from low resistance to high resistance in both the memristors of the pair, and wherein the method further comprises the step of applying a SET voltage to said pair of memristors such to cause a transition from high to low resistance in at least one memristor of the pair, said SET voltage being applied before said RESET voltage.

Fig. 1

(a)

(b)

Fig. 2

Fig. 3

Fig. 4

Fig. 5
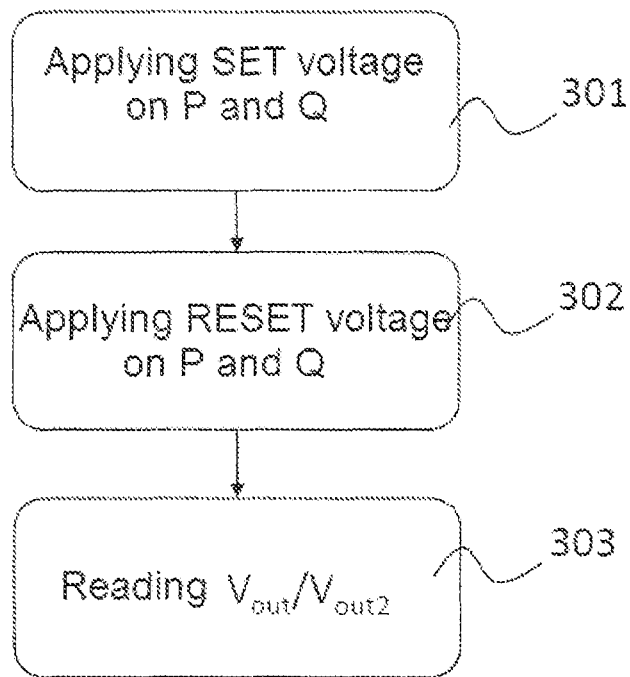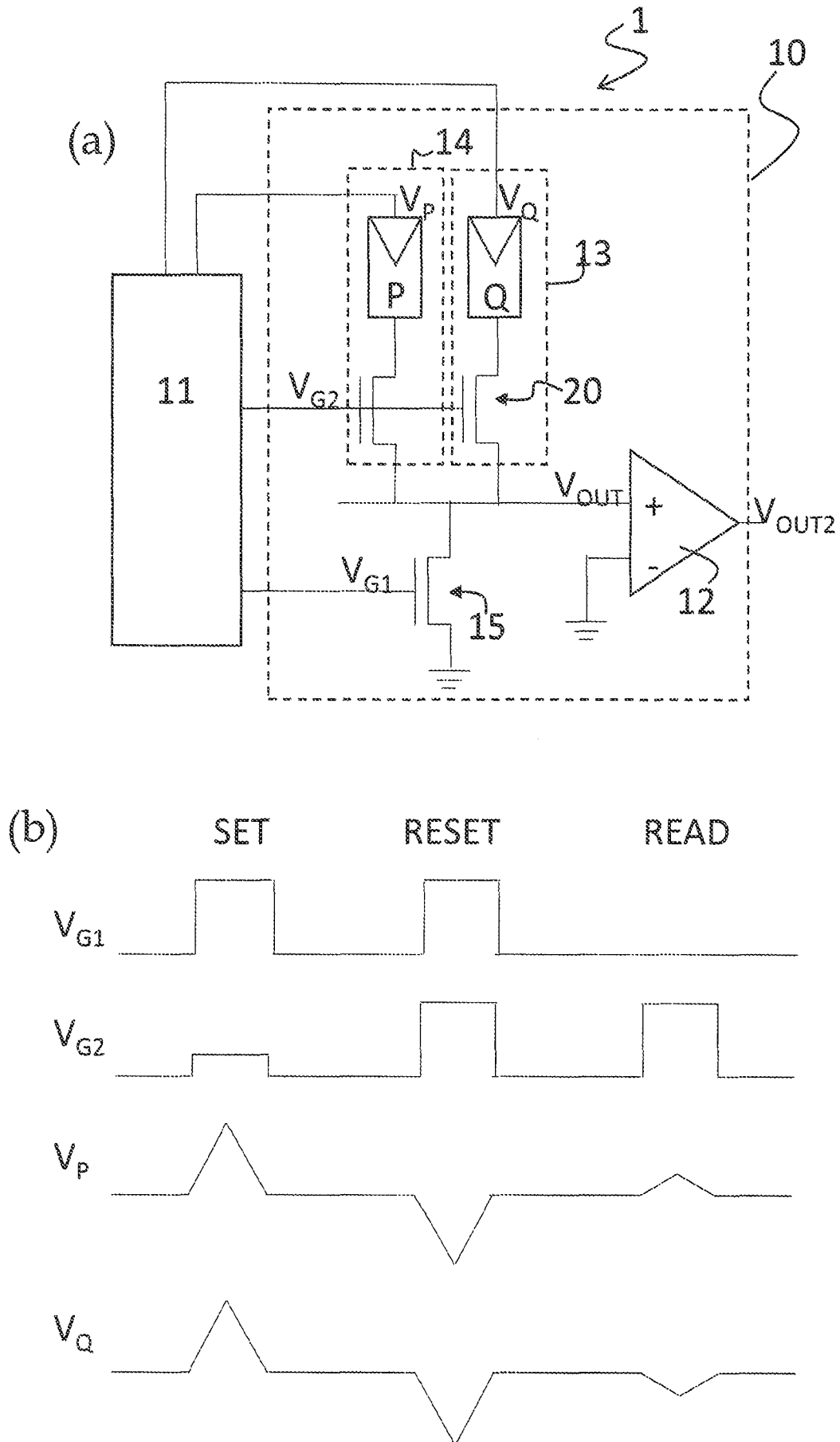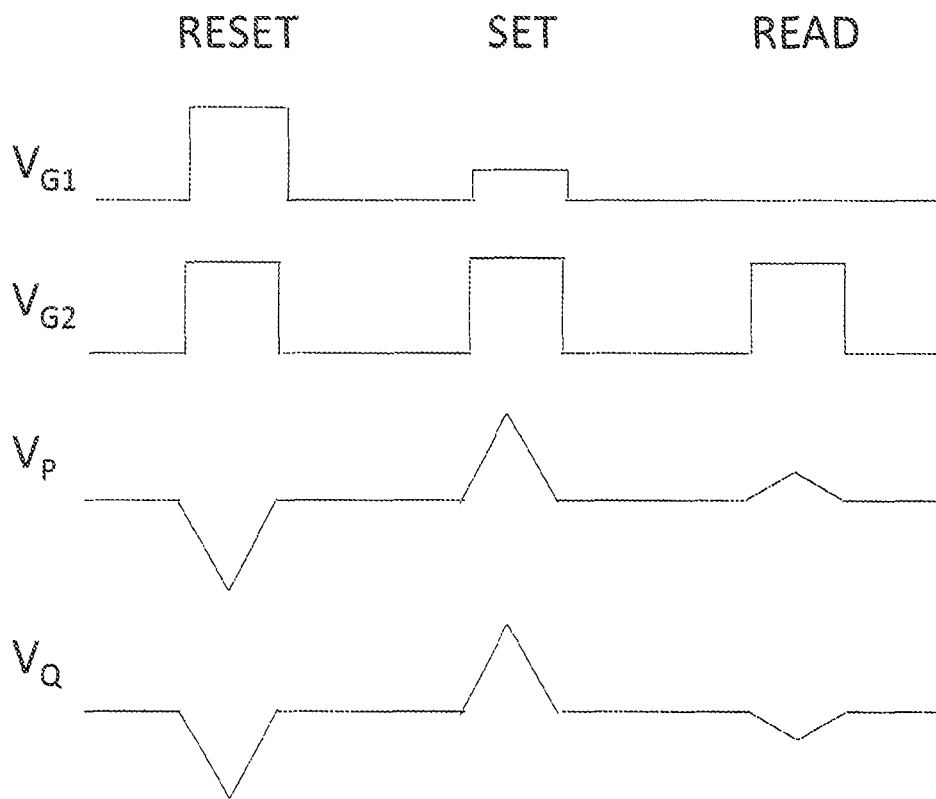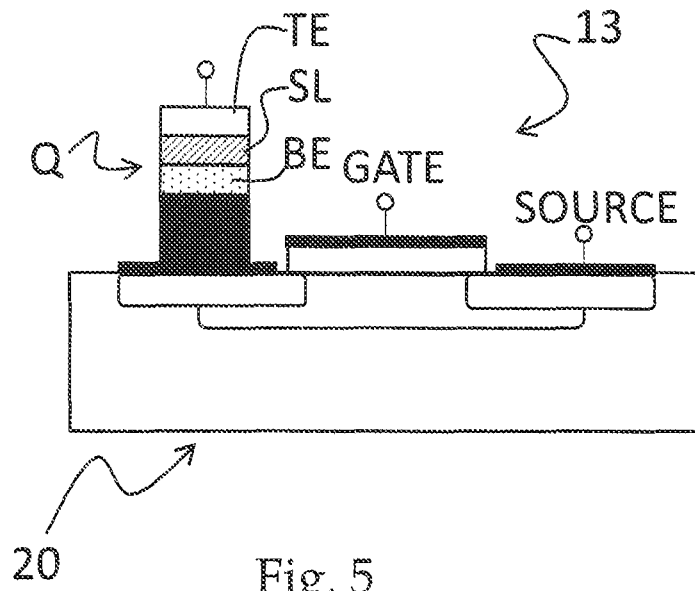
Fig. 7
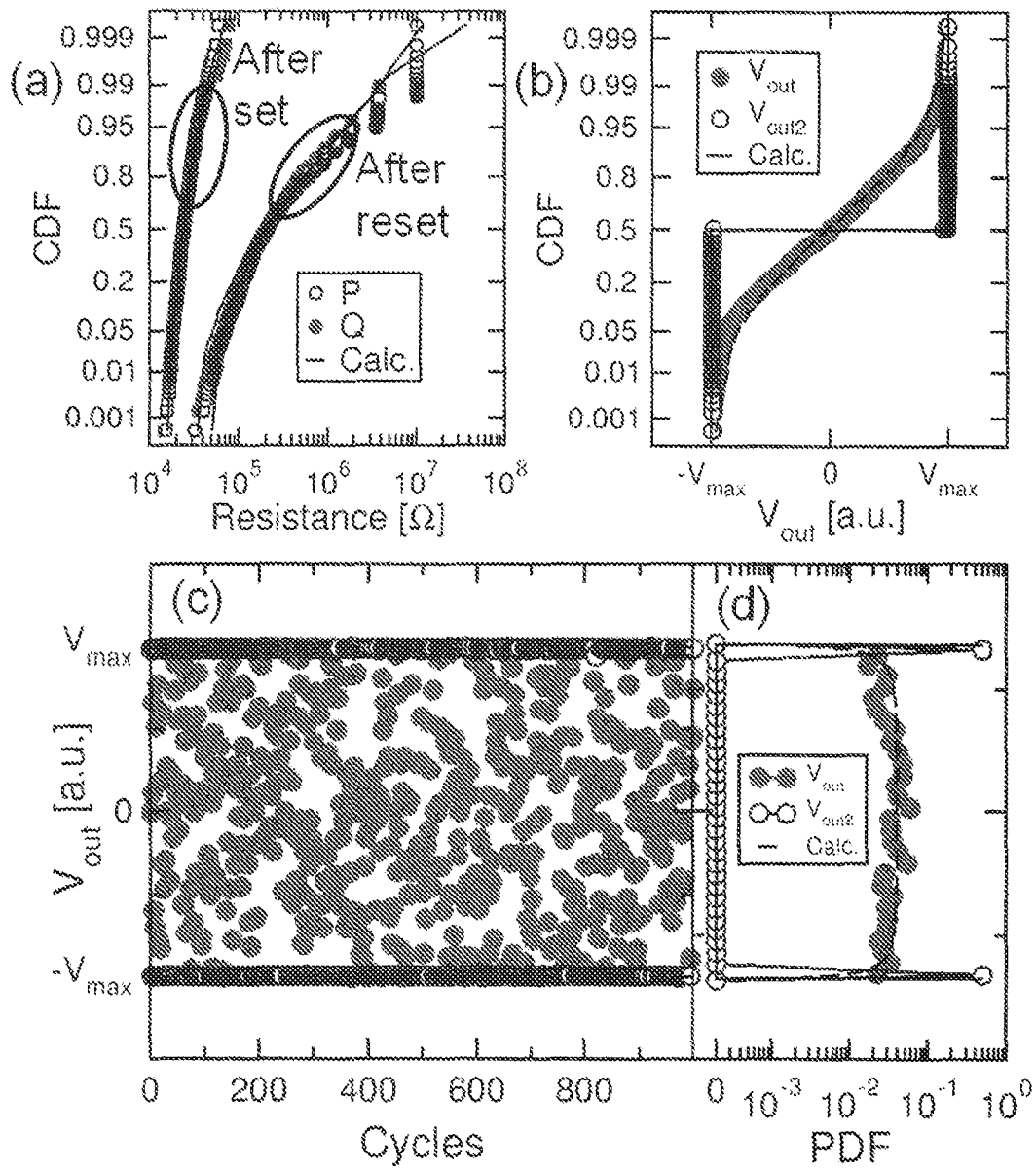
Fig. 6

Fig. 8

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09C1/00   G06F7/58   H04L9/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09C G06F H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 8 680 906 B1 (MCDONALD NATHAN [US] ET AL) 25 March 2014 (2014-03-25) abstract column 1, line 1 - line 38 column 3, line 6 - line 67 claims 1,2 -----	1-9
Y	BALATTI SIMONE ET AL: "Normally-off Logic Based on Resistive Switches-Part II: Logic Circ", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 62, no. 6, 1 June 2015 (2015-06-01), pages 1839-1847, XP011581796, ISSN: 0018-9383, DOI: 10.1109/TED.2015.2423001 [retrieved on 2015-05-18] paragraph [00II] - paragraph [0III] -----	1-9

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[X] Further documents are listed in the continuation of Box C.   [X] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 June 2017	20/06/2017

Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Bec, Thierry

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014/268994 A1 (ROSE GARRETT [US] ET AL) 18 September 2014 (2014-09-18) paragraph [0048] - paragraph [0055] -----	1-9
A	WO 2015/105687 A1 (STC UNM [US]; UNIV CASE WESTERN RESERVE [US]) 16 July 2015 (2015-07-16) paragraph [0038] - paragraph [0042] paragraph [0052] - paragraph [0053] figure 3 -----	1-9
T	EDWARDS ARTHUR H ET AL: "Reconfigurable Memristive Device Technologies", PROCEEDINGS OF THE IEEE, IEEE. NEW YORK, US, vol. 103, no. 7, 1 July 2015 (2015-07-01), pages 1004-1033, XP011585263, ISSN: 0018-9219, DOI: 10.1109/JPROC.2015.2441752 [retrieved on 2015-06-18] paragraph [00II] -----	
A	S. BALATTI ET AL: "Multiple Memory States in Resistive Switching Devices Through Controlled Size and Orientation of the Conductive Filament", ADVANCED MATERIALS, vol. 25, no. 10, 13 March 2013 (2013-03-13), pages 1474-1478, XP055380251, DE ISSN: 0935-9648, DOI: 10.1002/adma.201204097 page 1 - page 4 -----	1-9

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US 2014268994	A1	18-09-2014	NONE		
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			WO	2015105687 A1	16-07-2015