

# Multichannel 65 zF rms Resolution CMOS Monolithic Capacitive Sensor for Counting Single Micrometer-Sized Airborne Particles on Chip

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## ABSTRACT

The first integrated CMOS monolithic sensor system for on-chip capacitive detection of micrometric airborne particulate matter (PM) is presented. The chip is based on a 32-channel lock-in architecture allowing a dust collection area of 1.15 mm<sup>2</sup> where interdigitated differential microelectrodes, fabricated with the top metal and directly exposed to air, allow single particle sensitivity. The preamplifier input capacitance is significantly minimized thanks to the electrode-amplifier proximity and proper partitioning of the sensing area, in order to reduce the noise. Each channel comprises a charge preamplifier with adjustable high-pass filtering for flicker noise shaping, square-wave mixer,  $g_m$ -C tunable low-pass filter (40-750 Hz) and 6-bit digital network for automatic compensation of electrodes mismatch with granularity of 150 aF. Thanks to the capacitive noise of only 65 zF rms with 25 ms temporal resolution, deposition events of single mineral talc particles were recorded down to 1  $\mu$ m diameter with a SNR of  $\approx$ 18 dB. This chip paves the way to pervasive mapping of both in-door and out-door PM in the 1-30  $\mu$ m range.

Keywords: capacitive sensor; zeptoFarad resolution; impedance tracking; particulate matter (PM); air quality; smart sensors.

## I. Particulate Matter (PM) airborne detection status

Airborne Particulate Matter (PM) refers to a mixture of heterogeneous particles suspended in the air having both natural and anthropic origin. Particles are characterized by a variegated chemical composition and by a large distribution of dimensions [1]:  $PM_{10}$  accounts for particles with maximum equivalent aerodynamic diameter of  $10\ \mu\text{m}$ , while “fine” particles are smaller than  $2.5\ \mu\text{m}$  ( $PM_{2.5}$ ). It has been demonstrated that PM is severely hazardous to human health since there is a correlation between high concentrations of PM in the environment and the increase of some pathologies [2]. In particular, fine particles are especially dangerous as they might penetrate deeper into the respiratory system, causing lung and cardiovascular diseases [3-6]. Since tissue interaction and membrane translocation depend on the dimensions of particles, it is relevant from a toxicological point of view to reconstruct the granulometric spectrum of PM [7], alongside with a detailed mapping of PM concentrations to monitor and control air quality. To target this goal significant efforts are required to design low-cost compact sensors that can be embedded in network systems to promote widespread distribution and, thus, pervasive environmental mapping [8-10].

Standard instrumentation is based on gravimetric [11] or laser scattering [12] detection methods and is typically bulky, costly and offering inappropriate spatio-temporal resolution. The former has a pump to force a well-defined air volume through a membrane filter selecting the particles according to their sizes. Off-line the total weight of the membrane is measured and the PM concentration is extracted as an integral value with no granulometric information. On the other hand, the instrument based on laser scattering methods has a laser beam that interacts with a focused airflow causing light deflection according to particle's size. Even if laser scattering is able to provide single particle detection and granulometric information, the instrumentation is too bulky and expensive to be distributed in dense networks.

Trends in miniaturization have been exploiting the MEMS technology, in which PM depositing on a suspended microbalance structure changes the resonant frequency of the microfabricated resonator. Various techniques have been implemented, like Film Bulk acoustic resonator (FBAR) [13] or quartz crystal

microbalance (QCM) [14], both equipped with a microfluidic system to select and transport particles to the surface of the sensor, or electrometer sensing [15] where the particles are ionized by an off-chip bulky apparatus before being measured by a charge-sensing electrometer. Although capable of integrating fine PM, they still lack single-particle counting and size spectroscopy.

In order to target these latter aspects, we proposed an alternative approach leveraging a high-resolution capacitive sensing method [16]: a particle depositing between two metal electrodes of a micro-capacitor, changes the dielectric constant of the interposed air volume, as shown in Fig.1. By measuring the corresponding capacitance increase using a high sensitivity lock-in architecture, single micro-particle detection is achievable. Furthermore, it is possible to estimate the particle size from the amplitude of the capacitance signal, provided that an average PM permittivity is assumed (analogously to laser scattering). In the first implementation with separate microelectrodes and discrete electronics, a resolution of about 2 aF rms was achieved, allowing detection of talc particles down to 6  $\mu\text{m}$ .

This work aims to push the detection limit below to 1  $\mu\text{m}$  particle size and to obtain a compact, portable and low cost system. To this aim the electrodes and the electronics are integrated on a single CMOS chip. The small parasitic capacitance offered by an on-chip solution combined to a careful design of the readout electronics enables a capacitance resolution better than 100 zF that is compatible with the detection of 1  $\mu\text{m}$  PM.

The paper is organized as follows. Section II describes the motivations for the design of a multichannel differential sensor. Section III details the implementation of the CMOS chip. Section IV reports the experimental validation of the fabricated prototype, and Section V concludes the paper.

## II. Multielectrodes differential sensor design

Sensing electrodes have been fabricated on the CMOS chip by using the same top metal layer used for the bonding pads, as shown in Fig.2. The volume underneath the aluminum electrodes is left empty from metal layers to minimize the parasitic capacitance to only the coupling to the distant silicon substrate. The passivation layer above the electrodes is removed allowing the deposition of the target particles directly above the sensing electrodes, thus maximizing the capacitance signal to be detected. The native oxide of the aluminum prevents short circuits among electrodes in case a conductive particle is depositing on them. The opening of the passivation layer is done with the same standard CMOS process step used for the opening of the bond pads, no additional post-processing is required. The AFM topographic map confirms the quality of this process showing an over etching of the underneath oxide of less than 1  $\mu\text{m}$ . The width ( $W=1 \mu\text{m}$ ) and the gap ( $G=1 \mu\text{m}$ ) of the electrodes have been optimized for the detection of 1  $\mu\text{m}$  particles by finite element simulation. Numerical simulations of the capacitance variation as a function of particle diameter (see Fig. 2) show a capacitance step of 700 zF (zeptoFarad) for a particle of 1  $\mu\text{m}$  diameter and dielectric constant of 2. Based on this analysis the electronic chip has been designed to reach a resolution better than 100 zF.

In order to analyze a large air volume, a large sensitive area should be used. We have decided for a 1  $\text{mm}^2$  sensing area, considered a good trade-off between sensor cost and PM collection effectiveness. If a single interdigitated structure would have been used to cover this area, the capacitance step of 700 zF would be superimposed to a total capacitance of about 15pF, requiring a measurement capability of 0.05 ppm. Such sensitivity would impose severe constraints to the read-out electronics and to the stability of the capacitance as well as of the environment around the chip. To relax the specification of the measurement, we have partitioned the 1  $\text{mm}^2$  active area in 32 sensing channels of 500  $\mu\text{m}$  x 70  $\mu\text{m}$  operating in parallel and we also organized the electrodes in an efficient differential structure. As shown in Fig. 3, two sets of interdigitated electrodes, nominally equal in size, share a common electrode connected to a charge preamplifier, while the other two sides are connected to two counter-phase square-wave voltages. In an

ideally matched structure, only the difference in charge due to PM deposition on one of the two interdigitated electrodes is collected by the preamplifier, the rest of the charge being flowing through the two sets of electrodes. Thus, the dynamic range of the charge preamplifier and of the following electronics is significantly relaxed with a beneficial effect in terms of sensitivity. In addition, the noise of the voltage reference  $V_{ref}$  and all environmental fluctuations such as humidity or temperature changes are significantly rejected as they are common to both sets of electrodes. These advantages overcome the minor possibility of a size misestimating when a large PM is depositing at the interface between the two sets of interdigitated electrodes, being counted as a “small” particle due to the partially compensated signal given by the two opposite charges coming from both sets of electrodes.

The chip has a single analog output connected to the 32 channels through a multiplexer (see Fig. 3). Each channel includes the readout front-end, a synchronous demodulator to implement a lock-in architecture and a low-pass filter (LPF) setting the equivalent noise bandwidth to less than 1 kHz as required by the capacitance resolution of 100 zF. Having one LPF for each channel allows a fast scan of the 32 channels outputs, reaching a counting rate of tens of particles per second; if a single LPF in common to the 32 channels at the output of the multiplexer would have been used we would have to wait for the settling time of the LPF at each change of channel, resulting in a solution more than 32 times slower.

### III. Readout frontend and lock-in demodulator design

Figure 4 shows a schematic of the readout analog front-end as designed to fully profit of the differential sensor structure. The on-chip  $\Phi_1$  and  $\Phi_2$  clocks produce two counter-phased square wave voltages with amplitude  $V_{ref}$  and frequency of 200 kHz to bypass the flicker noise of the preamplifier. The external reference voltage  $V_{ref}$  has been chosen equal to the voltage supply (3.3V) to maximize the charge injected in the preamplifier. The current coming from the capacitive sensor is read by a charge preamplifier with a

small feedback capacitor of  $C_F = 20$  fF to guarantee a high gain. A p-channel MOSFET ( $M_{P1}$  in the figure) in pseudo-resistor configuration is added in the feedback loop to ensure DC leakage current discharge irrespective of its sign, acting as a drain-to-substrate p-n junction for positive leakage (entering the preamplifier) and as subthreshold MOSFET for negative leakage. We have chosen a p-MOS transistor with a high threshold voltage (-0.97V) in order to increase the linear dynamic range of the output node.

The preamplifier uses the low noise operational amplifier shown in Fig. 5. The differential input stage has a resistive load sized to have a negligible noise. Consequently, the power spectral density of the equivalent input charge noise  $\overline{q_n^2}(f)$  of the charge preamplifier is limited by the noise of the input transistors:

$$\overline{q_n^2}(f) \approx 2 \cdot \frac{4kT\gamma}{g_m} (C_{UP} + C_{DW} + C_{amp} + C_{stray} + C_F)^2 \quad (1)$$

where  $g_m \approx \sqrt{2\mu C_{ox}W/L I_{bias}}$  is the transconductance of the input transistors, the  $\gamma$  parameter is about 2/3,  $C_{UP}$ ,  $C_{DW}$  and  $C_{stray}$  are the capacitances of the sensors (respectively of 180 fF, 180 fF and 120 fF) and  $C_{amp} \approx 2/3 \cdot C_{ox}WL$  is the capacitance of the amplifier given by the input transistor. The flicker noise is neglected thanks to the measurement frequency higher than the corner frequency. The bias current  $I_{bias}$  of the input transistors has been fixed to 100  $\mu$ A to minimize the power consumption maintaining a noise compatible with the target capacitance resolution. The size of the input transistor has been optimized to minimize Eq. (1), that is its gate capacitance equal to 1/3 of the total input capacitance (500 fF), leading to  $W = 102 \mu\text{m}$  and  $L = 0.6 \mu\text{m}$  (minimum value to achieve a good matching of the differential input pair). The result is a voltage noise of the input transistor of  $6.2 \text{ nV}/\sqrt{\text{Hz}}$  and an equivalent input charge noise of  $\overline{q_n^2}(f) \approx (8 \text{ zC}/\sqrt{\text{Hz}})^2$ , which corresponds to a capacitance noise floor of  $\sqrt{\overline{q_n^2}(f)}/V_{ref} = 2.4 \text{ zF}/\sqrt{\text{Hz}}$ . Consequently, the preamplifier imposes an

equivalent noise bandwidth lower than 1.6 kHz to reach the required capacitance resolution of 100 zF (defined as the rms value of the capacitance measurement as imposed by the analog output of the chip). Such small bandwidth centered at the modulation frequency of 200 kHz is fixed by the LPFs following the demodulation stage.

The differential input stage is connected to a second differential stage with a mirrored cascode that provides additional gain (total dc gain of 107 dB) to the operational amplifier and a gain-bandwidth product of 140 MHz assuring a closed-loop bandwidth of 7 MHz. Since the noise constraints are relaxed by the first stage, the bias current of this second stage is only 10  $\mu$ A. Finally, a source follower grants a low output impedance, as required for driving the capacitance load of the following high gain (40x) voltage amplifier. The latter has been added to the chain in order to minimize the noise contribution of the following low-pass filter. The capacitive feedback of the voltage amplifier uses two p-MOS transistors ( $M_{P2}$  and  $M_{P3}$  in Fig. 4) to fix the DC bias point. The symmetrical configuration of these two pseudo-resistors allows for a larger linear dynamic range of 2.8 V<sub>p-p</sub> [17]. Both amplifiers OP1 and OP2 are offset by 1.65V to set the sensor signal within the 0 V-3.3 V voltage supply.

#### A. Lock-in demodulator

Figure 6 shows the Non-Return-to-Zero (NRZ) passive mixer [18] and the low pass  $g_m$ -C filtering section, together performing the lock-in demodulation. The input switch is driven synchronously with the square waves applied to the sensor, so to track & hold the two levels of the incoming signal separately on the two filtering paths. The difference between the outputs of the two filters tracks the unbalanced capacitance of the sensor, that is the variation due to the PM deposition. The switch is implemented with transistors of small size ( $W/L = 3 \mu\text{m}/0.35 \mu\text{m}$ ) to reduce the clock feed-through and the charge injection [19]. Thus, the noise added by the mixer is limited to the unavoidable noise folding associated with the

sampling operation [20], estimated in about 6 dB. Differently from a more common double-balanced passive mixer, the NRZ architecture down-converts the single-ended output of the voltage amplifier directly to a DC signal at the input of the two LPFs, ideally without frequency components at the demodulation frequency and its harmonics. The small AC signal at the input of the LPF, mainly given by the noise of the previous stages, allows an effective filtering by using a simple 1<sup>st</sup> order filter implemented with a  $g_m$ -C stage without paying the limited differential linear range of this architecture. The capacitance of the filter has been set to  $C=1$  pF as a trade-off between the area occupation and the theoretical limit of its noise,  $kT/C$ . The required cut-off frequency lower than 1 kHz imposes a transconductance value of the order of few nS. This has been obtained using an operational transconductance amplifier with current division [21], as shown in Fig. 7. The bandwidth is tunable from 40 Hz to 750 Hz by selecting, via an external voltage  $V_{p2}$ , the biasing current of the input stage from 0.5 to 12 nA. A complementary differential input pairs provides a rail-to-rail common mode operation of the OTA, thus ensuring a wide dynamic range of the LPF. To dump the high frequency feedthrough from the input  $V_{in+}$  to the output node through the gate-source capacitances of the input transistors that would limit the out of band attenuation of the filter, the sources of the differential pairs have been shunted to ground by capacitances  $C_p$  and  $C_n$  (both 500 fF) obtaining a measured attenuation of -55 dB.

As a consequence of the OTA architecture with current division, the noise of the filter is mainly given by the transistors operated with the lowest bias current. The noise has been reduced to the output transistors M11 and M12 by using mirrors with a current reduction of 5:1. The full current division of 20:1 is also partially implemented by the input stage of the OTA for avoiding large transistors in the mirrors, as would be required for an accurate 20:1 mirror ratio. The resulting white noise of the  $g_m$ -C filter is  $8/5 kT/C$ , that is less than a factor 2 higher than the theoretical limit. The corner frequency of the flicker noise is fixed to less than 1 Hz by operating all the transistors in sub-threshold regime. The noise contribution of the filter accounts for about the 30% of the total noise of the readout electronics.

## B. Electrodes mismatch compensation network

The voltage amplifier between the charge preamplifier and the lock-in demodulator has been added to limit the noise of the  $g_m$ -C filter. The high gain of 40 sets the input full scale of each channel in terms of capacitance signal to a value of about 1 fF, limited by the saturation of the voltage amplifier. Process mismatch of the electrodes may themselves be higher than this value causing saturation of the channel at switch-on. Similarly, the differential electrodes can be unbalanced by the random deposition of the particles limiting the operative time of the sensor before the saturation. To circumvent these possibilities, a variable capacitor in parallel to the electrodes has been added and digitally controlled to ensure an all-time balanced condition of the differential sensor structure. The variable capacitor, that we call digital-to-capacitance converter (DCC), is implemented by inserting a physical 4.6 fF capacitance to the input node, the other electrode being connected to the output of a five bit resistor string-based DAC supplied by the same voltage reference  $V_{ref}$  of the electrodes (see Fig. 4). An additional bit establishes the sign of the compensating capacitive current injected into the virtual ground of the charge preamplifier. Consequently, the DCC has a minimum variation of the equivalent capacitance of  $LSB=4.6\text{ fF}/32=150\text{ aF}$  well within the 1 fF of the dynamic range of the readout frontend. The experimental characterization of this converter is reported in Fig. 8 and shows a linear behavior with differential non linearity of 15 aF, equivalent to 0.1 LSB. Thanks to the monotonic behavior of the DCC, a self-calibration network has been implemented in each channel to automatically adjust the compensating capacitance. It uses only 4 comparators, logic gates and an up-down counter and generates the bits for the DCC based on the analog output level compared to threshold voltages so to ensure that the differential output signal is always within the allowed linear dynamic range.

## C. Low frequency noise shaping

A point of concern in the analog front-end is the high value of pseudo-resistor  $M_{P1}$  as a consequence of the very low leakage current at the input node of the preamplifier, mainly given by the reverse current of the drain-substrate p-n junction of  $M_{P1}$  itself. In this condition, the equivalent resistance of  $M_{P1}$ ,  $1/g_{mP1}$ , can reach values higher than 1 T $\Omega$  [22] with an extremely high amplification of the random fluctuations of the leakage current. Since the surface of the chip is in direct contact with the air to be accessible to the particles, the leakage current can be prone to environmental changes, in particular to the illumination that is converted into a photocurrent by the reverse-biased p-n junctions. In addition, the flicker noise of the input operational amplifier (OP1 in Fig. 4) is amplified by  $1+(C_{UP}+C_{DW}+C_{stray}+C_{amp})/C_F \approx 35$  starting from the frequency  $f_{HP} = g_{mP1}/(2\pi C_F)$ , below 100 Hz in typical conditions. The flicker noise and the random fluctuations of the leakage current are then further amplified by 40 from the following voltage amplifier and sampled by the NRZ mixer. The frequency components much slower than the mixer frequency (200 kHz) are sampled in the same way at the inputs of the two LPF, thus converting them in a large common mode of the differential output of the channel. Montecarlo simulations show a common-mode rejection ratio of the LPFs limited by the process mismatches to 54 dB (mean value, 32 dB in the worst case) and an increase of the differential output noise by a factor 3 caused by the flicker noise of OP1. In order to limit this low frequency noise feedthrough, the transistor  $M_{P1}$  has been biased by injecting a DC current  $I_{INJ}$  at the input node of the charge preamplifier, as shown in Fig. 9.  $I_{INJ}$  is used to increase the transconductance of  $M_{P1}$  and correspondingly to reduce the low frequency gain of the preamplifier without any modification of the signal path at the modulation frequency. The bias current  $I_{INJ}$  is of tens of pA and is produced by means of a current demultiplier (by a factor 50) driven by an off-chip 1 G $\Omega$  resistor in common to all 32 channels. The effectiveness of this noise shaping process can be seen in the experimental data of Fig. 10. The graph shows the equivalent capacitive noise of a single channel as a function of the high pass frequency pole  $f_{HP}$  that is tuned by changing the voltage  $V_{p1}$  applied to the 1 G $\Omega$  (Fig. 10, inset). A noise shaping at around 1 kHz is already sufficient to improve the sensitivity of the system by a factor of 3. By increasing the value of  $f_{HP}$  further, the noise reaches a plateau at 60 zF rms, about 1/5<sup>th</sup> of the noise level with  $I_{INJ}=0$ . Such plateau

suggests that the value of the injected current is not critical, leaving the system performance almost insensitive to  $M_{P1}$  technology and temperature fluctuations.

#### IV. Experimental Results

The chip has been implemented in AMS 0.35  $\mu\text{m}$  C35B4 technology, and it is shown in Fig. 11. It occupies a total area of 6  $\text{mm}^2$  with a dust-collection surface of 1.15  $\text{mm}^2$ . As visible, the pads for wire-bonding of the signals have been concentrated in one side in order to leave the other three sides of the die free from bonding wires and thus accessible for fluidic structures guiding the deposition of PM [16]. The supply voltage is 3.3 V and current consumption is 25.6 mA, justified by the extremely high sensitivity required in the application. The die is directly bonded on a small PCB, acting as replaceable carrier board, plugged into a motherboard providing power supply, regulated references, clocks and connection to a standard data acquisition system (NI6289 by National Instruments). A graphical user interface developed in LabView displays and saves the traces of the 32 channels in real time. The output voltage of the chip is converted into a capacitance variation using the gain provided by post-layout simulations. Measurements on a test chip having an additional bonding pad at the input node of the preamplifier have shown a discrepancy less than 15% between the measured gain and the simulated gain. The recorded traces are processed to extract the fast capacitance variations given by the deposition of a particle irrespective of the capacitance baseline (related to the mismatch of the differential structure and to the particles previously landed on the electrodes).

The measured noise level in all 32 channels at four different filter bandwidths is shown in Fig.12. The rms capacitance noise is calculated on an acquisition of 1 minute of the output noise and using the post-layout gain provided by the simulator. The gain accuracy has been estimated better than 10% based on the experimental results of a single channel test chip with an additional pad at the input of the preamplifier, here

removed for noise and area minimization of the multichannel structure. The figure certifies that a minimum resolution of  $\approx 45$  zF rms can be achieved with the narrowest signal bandwidth of 40 Hz. By taking in account the inaccuracy of the gain (10%, worst case), the averaged resolution on the 32 channels is 65 zF rms. Measurements also show a noise proportional to the square root of the bandwidth as it is in the case of dominant white noise, highlighting that the contribution of the low frequency flicker noise of the input stage and of the  $g_m$ -C stages has indeed been made negligible. The comparison with the state of the art in CMOS capacitance detectors is reported in Table 1. Although a direct comparison is difficult because of the different applications, this work achieves the best capacitance resolution with a lower measurement time and a power dissipation per channel comparable to many other works.

In order to validate the detection capability of the chip, test particles with defined dielectric constant and characterized dimensions [16] have been used as model for airborne PM. In particular mineral talc (Microtalc FC CG by Mondo Minerals characterized by a lognormal diameter distribution with a median of 8  $\mu\text{m}$  and dielectric constant of 2.4) has been mechanically suspended in air above the chip at different concentrations and distances from the chip operated without package and Faraday cage. Before and after deposition sessions, an optical microscope has been used for visual inspection of the sensing electrodes area, thus providing sets of images for estimating the size of deposited particles. The visual inspection has been simplified by performing a periodic cleaning of the surface with nitrogen jets.

An example of a deposition event is reported in Fig. 13. A single talc particle of approximately 5  $\mu\text{m}$  diameter (as estimated by the micro-photograph, showing also a defect stuck on the electrodes used as visual reference) landing on channel 18 produces a capacitance variation of about 10 aF. For this measurement the noise level is  $\sim 80$  zF rms with a bandwidth of 85 Hz. The signal-to-noise-ratio (SNR) is equal to  $10 \text{ aF} / 80 \text{ zF} = 125$  allowing very clean detection, two orders of magnitude better than what achieved with the previous discrete-component implementation [16]. The figure also reports the signals of the adjacent channels (17 and 19) certifying the absence of detectable cross-talk. The deposition of the

particle produces a fast capacitance variation that can be easily separated from slow drifts due to temperature or humidity fluctuations.

Several particles have been counted in similar experiments of controlled dust deposition with microscope cross-checking as reported in Fig. 14. Despite some uncertainty in the estimate of the equivalent volume due to the non-spherical shape of real particles and to the intrinsic bidimensionality of microscope images, the experimental data are consistent with numerical simulations (Fig. 2). Here the size of detected particles ranges from  $\sim 1 \mu\text{m}$  (0.7 aF) to  $\sim 12 \mu\text{m}$  (27 aF). By extrapolating the relation between  $\Delta C$  and the diameter of particles and considering the best circuit resolution of 65 zF, the smallest detectable diameter of a talc particle (i.e. with very low  $\epsilon_r = 2.4$ ) would be  $0.3 \mu\text{m}$  (with a SNR = 1), which is comparable with the detection limit of state of the art instrumentation based on laser scattering.

## V. Conclusion

An unprecedented 65 zeptoFarad resolution (see the comparison in Tab. 1) has been demonstrated for a multichannel (32x) CMOS capacitive sensor with on-chip electrodes and large sensitive area ( $1.15 \text{ mm}^2$ ). This performance has been obtained by designing an ad-hoc differential electrodes structure and implementing a circuit for flicker noise shaping of the input preamplifier. The chip is consequently perfectly suited for real-time counting and sizing of airborne particles in the 1-30  $\mu\text{m}$  range, achieving the detection of single PM with an equivalent diameter below  $1 \mu\text{m}$ , as we have experimentally demonstrated. The thin native oxide covering the Al metal electrodes prevents short circuits in the case of conductive particles. Furthermore, since water droplets may provide large artifacts ( $\epsilon_r = 80$ ) and false counts, it is necessary to endow the air sampling system with a heated probe that forces evaporation of aerosols. The sensor may be completed with a surface cleaning system (for example using mechanical vibrations and / or air

jets) for the removal of deposited particles when they cover a large portion of the active area. Alternatively, the sensor can be used as a disposable cartridge without a surface cleaning system.

The technological solution of fabricating the micrometric sensing electrodes by using the same top metal layer of the bonding pads, without any additional post-processing, makes the proposed sensor potentially low-cost for mass production and ready for integration into more complex ICs. Thank to these features, it is possible to envision the embedment of future generations of this ASIC, possibly combined with proper inlet fluidics, in compact wireless sensors nodes, spread in the urban environment, as well as in handheld devices, such as smart-phones, for personal dosimetry, pervasive air quality monitoring and participatory PM mapping.

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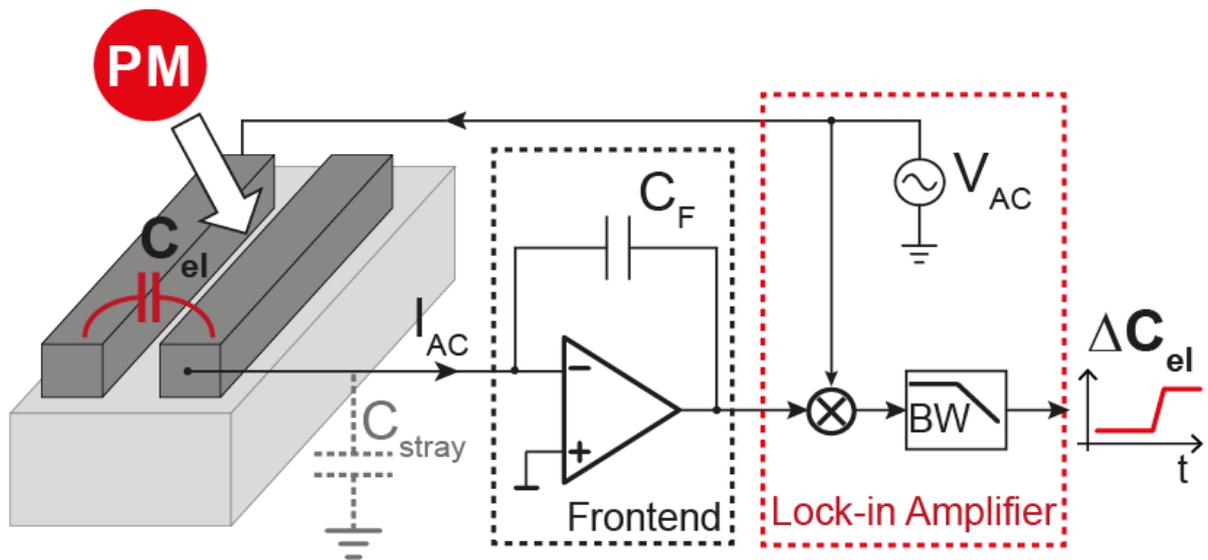


Figure 1

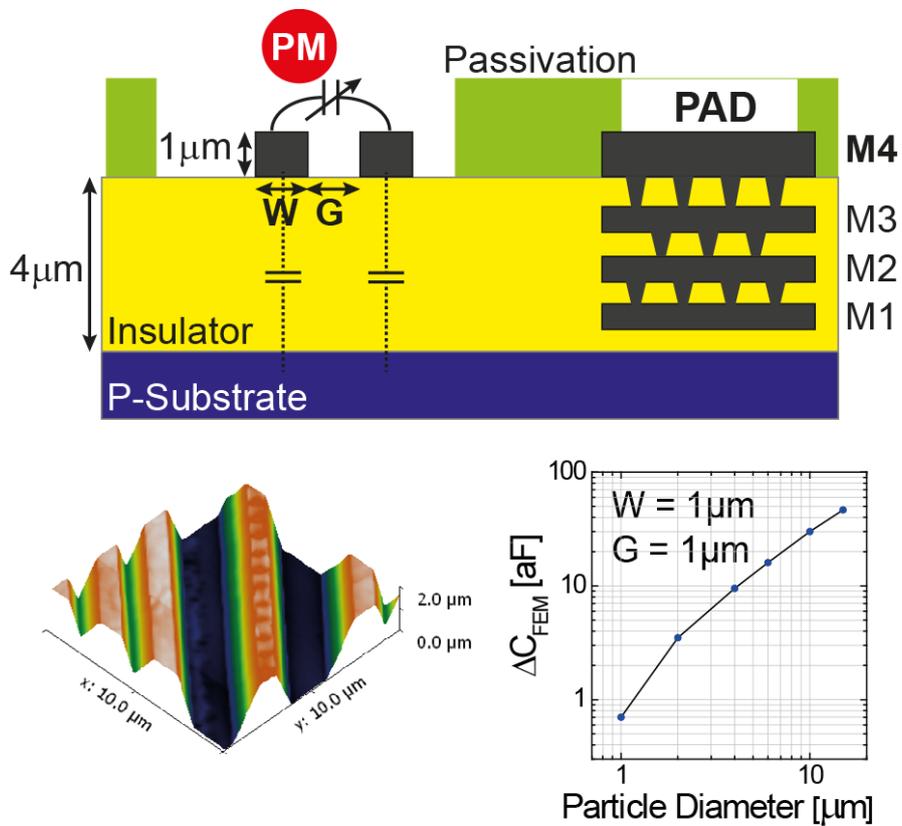


Figure 2

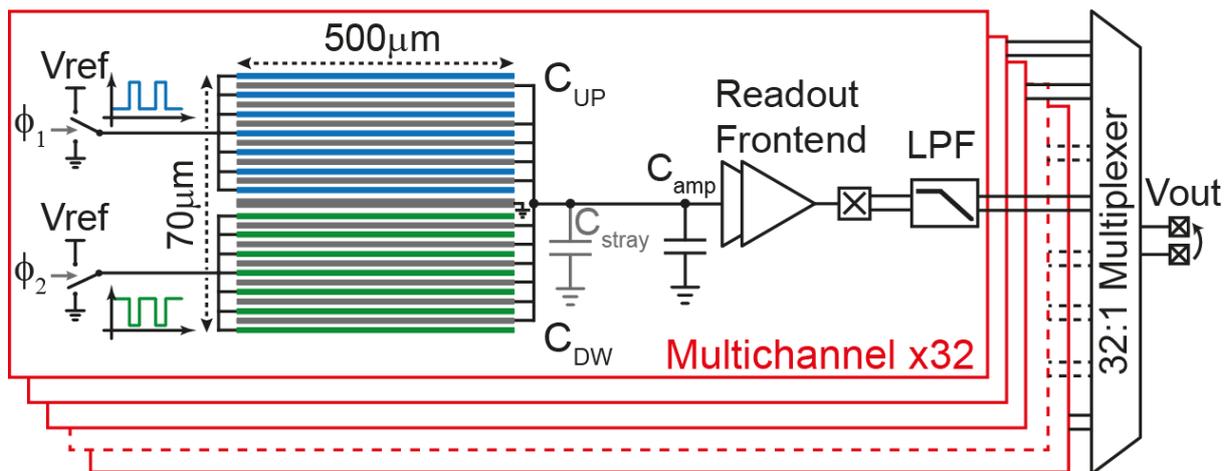


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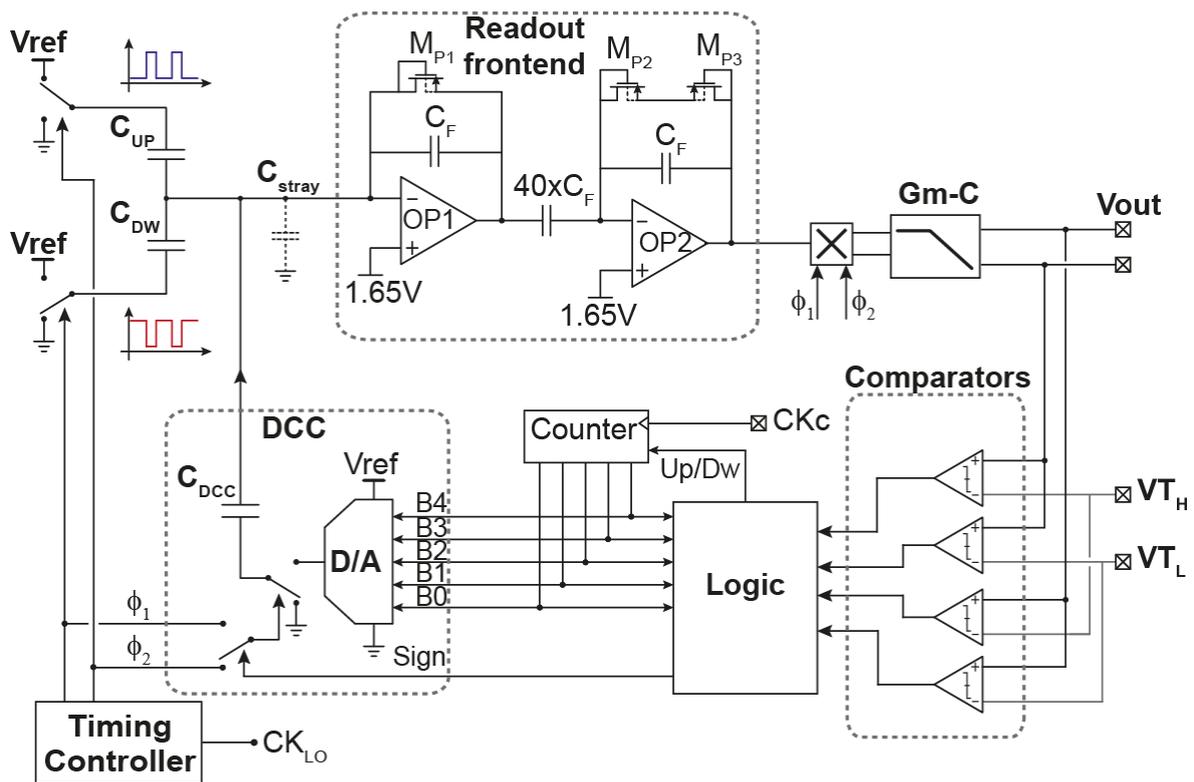


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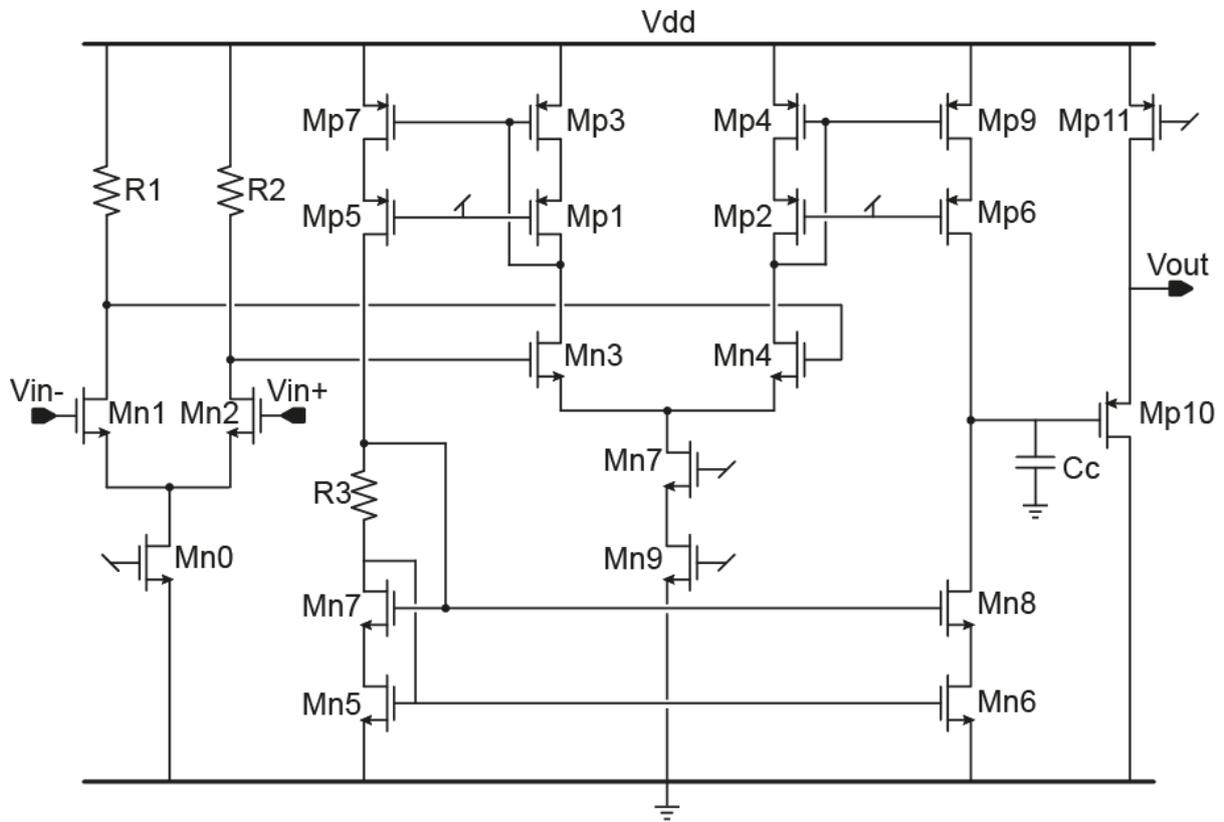


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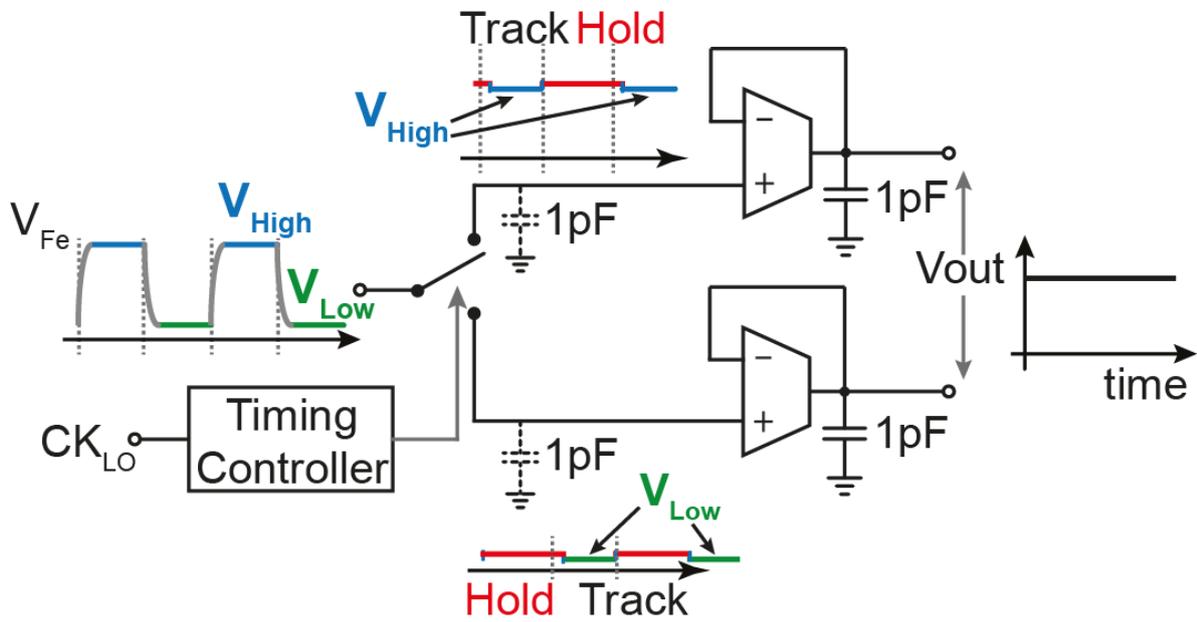


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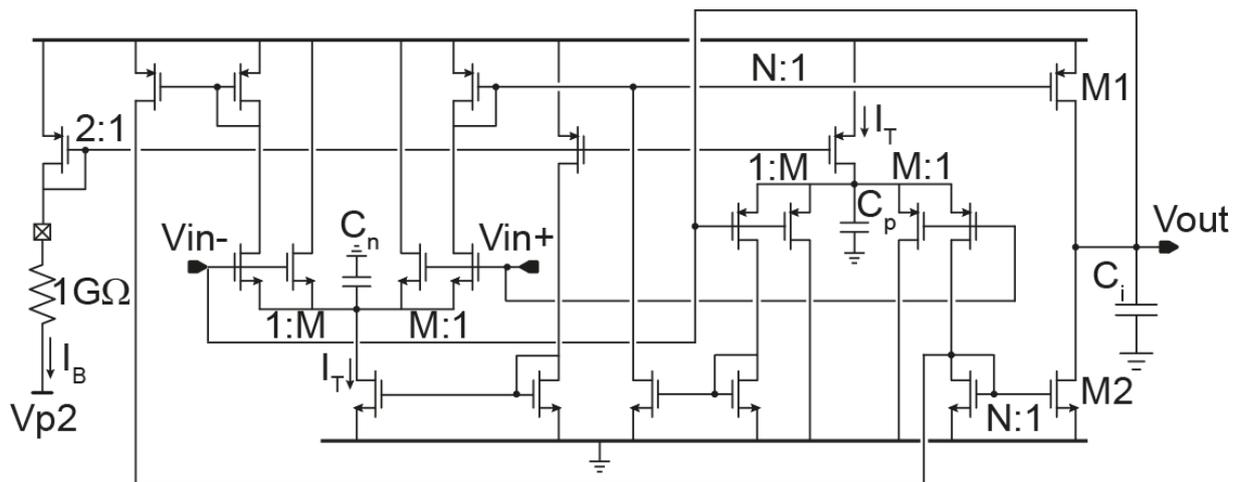


Figure 7

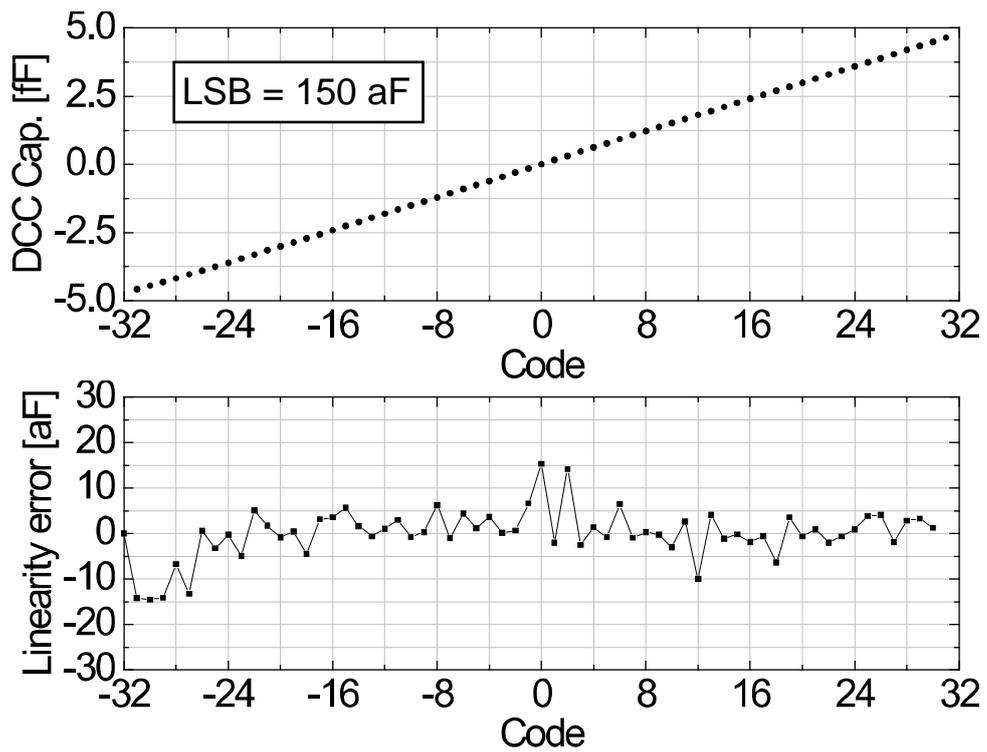


Figure 8

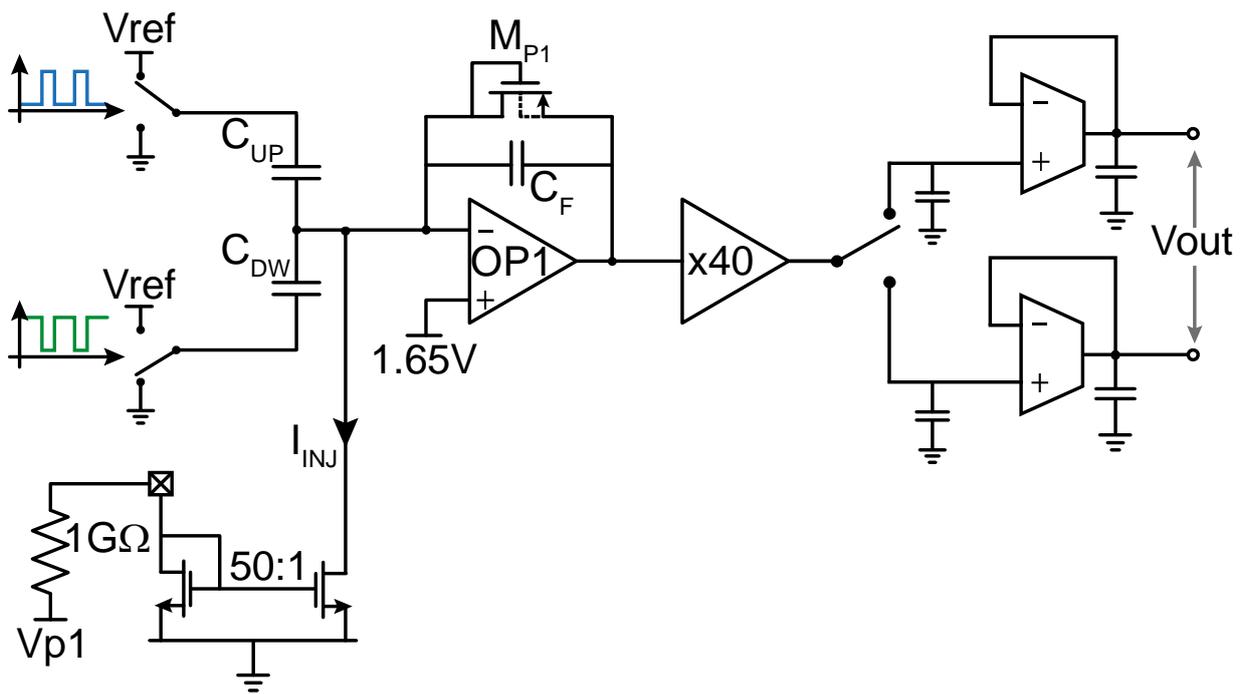


Figure 9

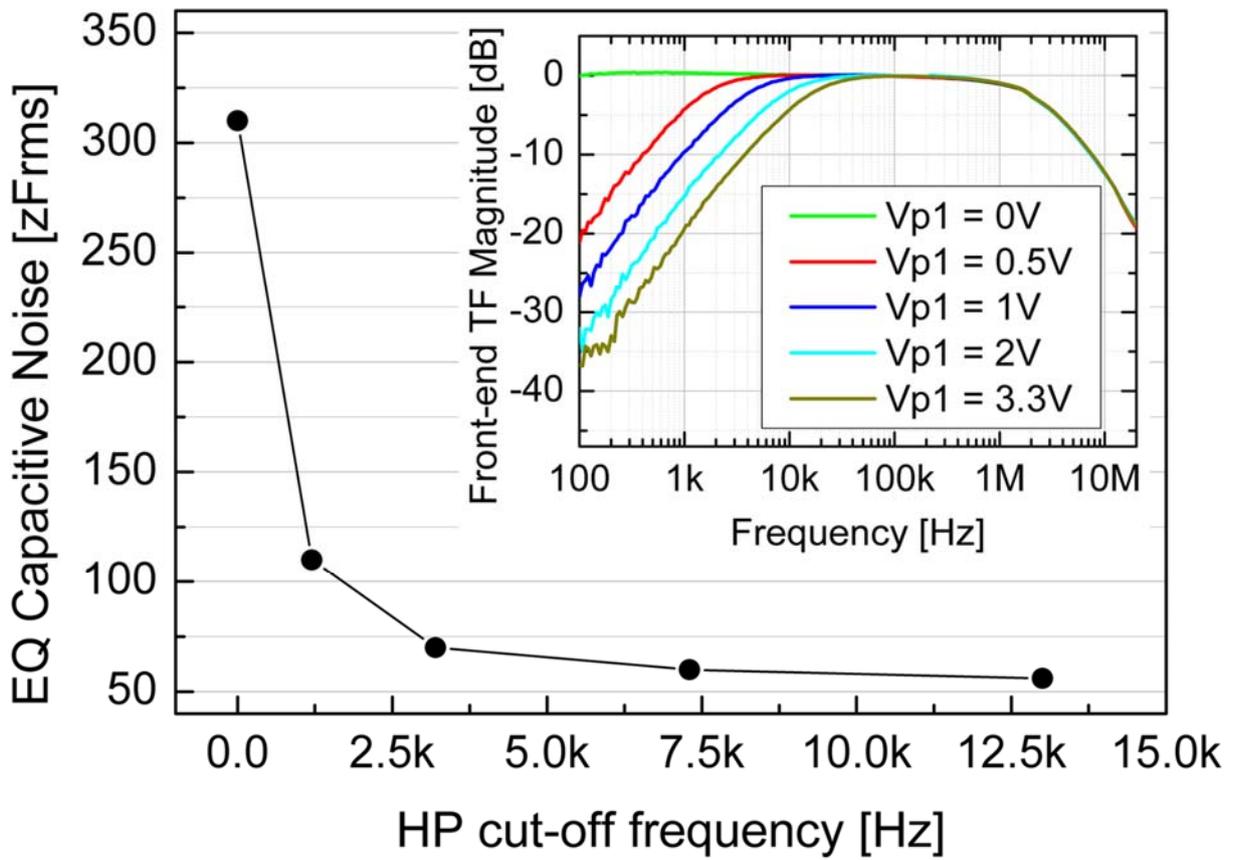


Figure 10

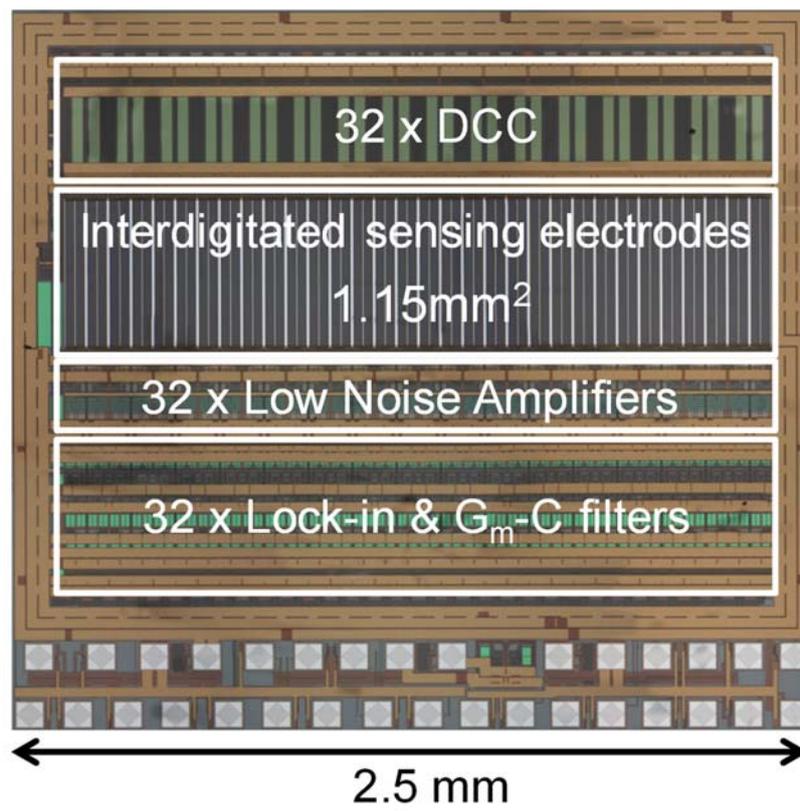


Figure 11

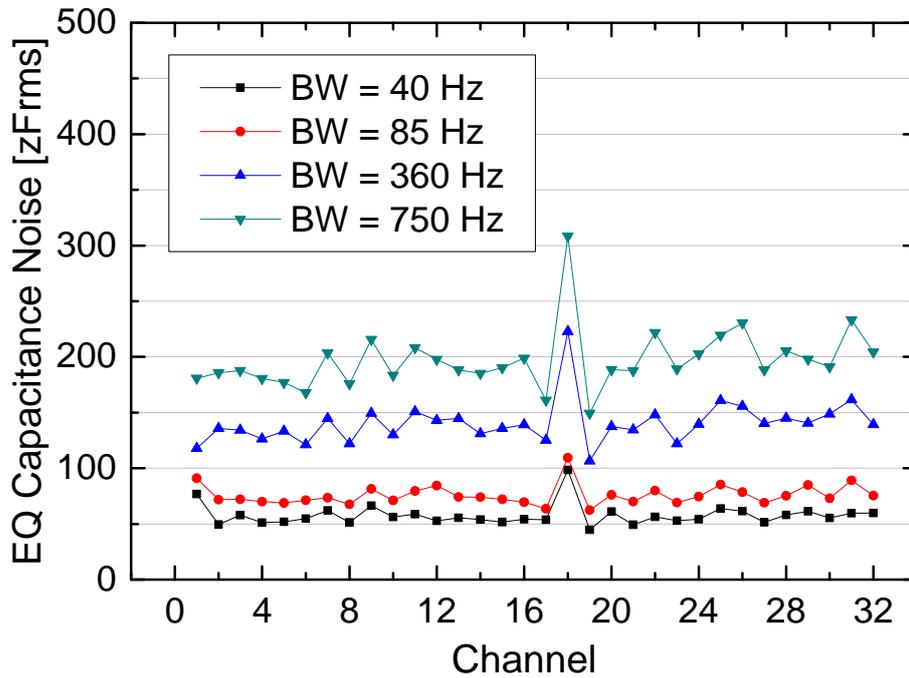


Figure 12

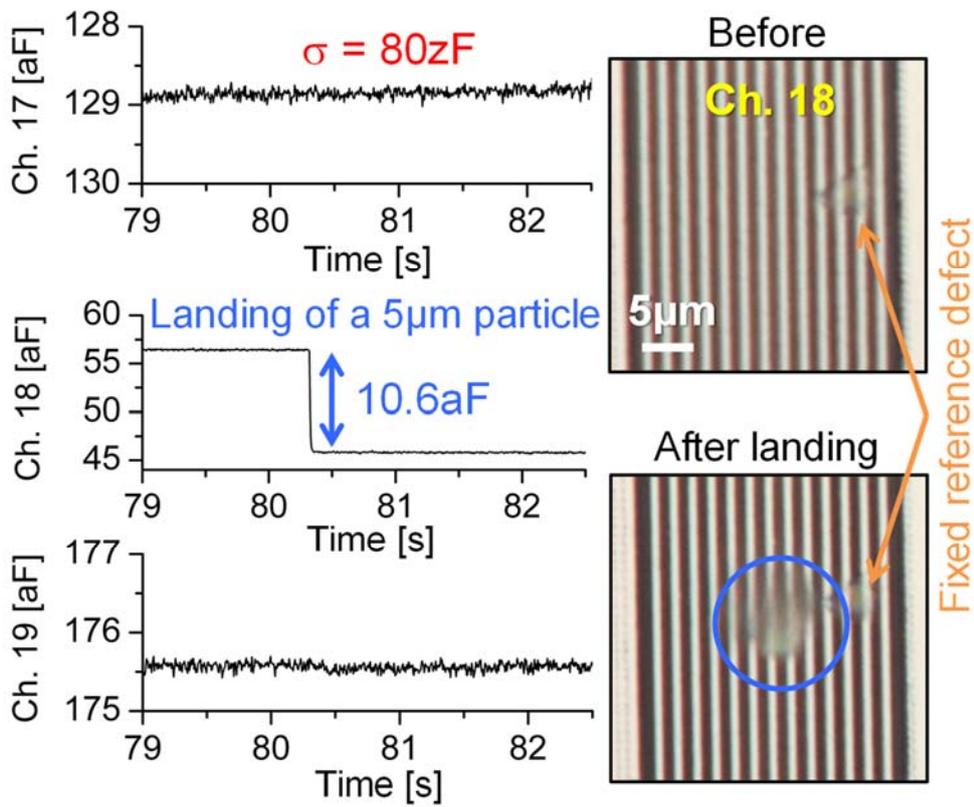


Figure 13

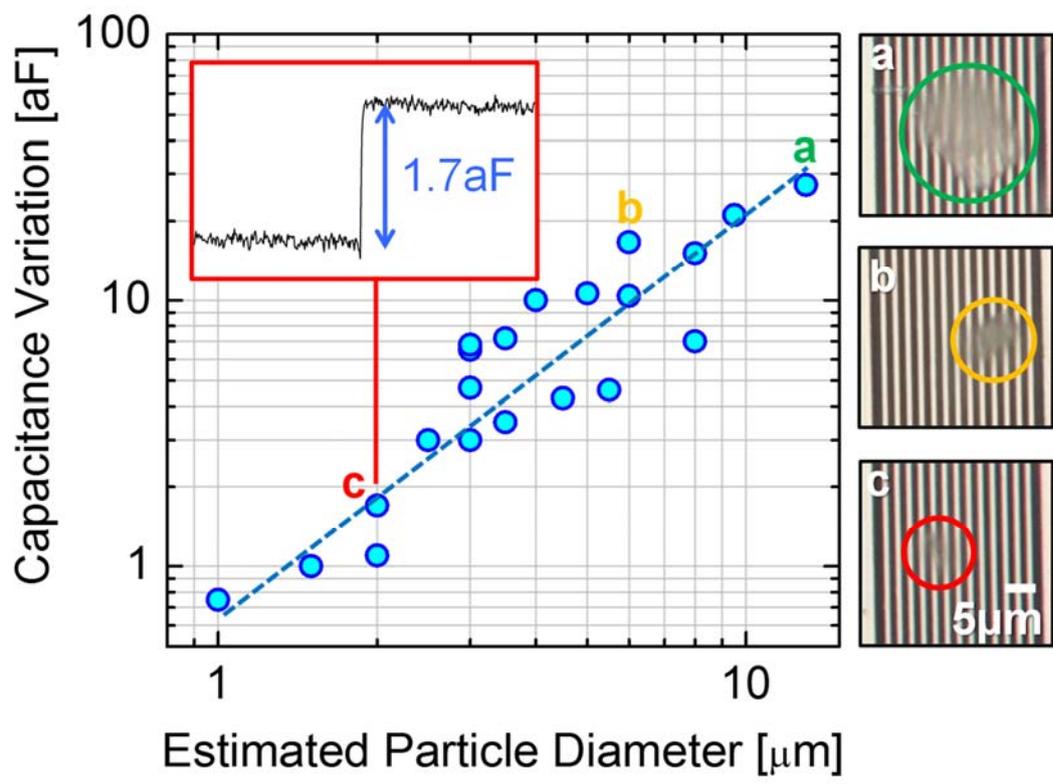


Figure 14

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF THE ART

	[23]	[24]	[25]	[26]	[27]	[28]	This work
Technology	0.35 $\mu$ m	0.35 $\mu$ m	0.5 $\mu$ m	0.6 $\mu$ m	0.13 $\mu$ m	0.35 $\mu$ m	0.35 $\mu$ m
Structure	Lock-in	Mod/Dem	Switched-capacitor	Switched-capacitor	Lock-in	Lock-in	Lock-in
Application	IS*	IS*	MEMS	MEMS	IS*	IS*	Airborne particle detector
Cap. resolution (rms)	0.15 aF	0.35 aF	<2 aF	0.42 aF	5.1aF <sup>+</sup>	6.4 aF <sup>+</sup>	0.065 aF
Meas. time	80 ms	80 ms	0.8 s	0.8 s	--	80 ms	25 ms
# channels	1	1	1	1	16	100	32
Power dissipation	60 mW	135 mW	23 mW	3.75mW	1.8 mW	84.8 mW	84 mW
Area	0.5 mm <sup>2</sup>	1.6 mm <sup>2</sup>	7.8 mm <sup>2</sup>	0.33 mm <sup>2</sup>	1.68 mm <sup>2</sup>	4 mm <sup>2</sup>	6 mm <sup>2</sup>
Supply	3 V	3 V	7 V	3 V	1.2 V	3.3 V	3.3 V

\* Impedance Spectroscopy

+ Estimated from the parameters given in the paper

## Table of figures:

- 1 Scheme of the capacitive sensing method showing the PM particle depositing between two conductive electrodes, the AC voltage source to drive the sensor, the front-end transimpedance amplifier to collect the signal current and the mixer-filter to lock and demodulate at  $f_{AC}$ .
- 2 Cross-section of the CMOS chip highlighting how the uppermost metal layer (M4) can be used for the production of the sensing electrodes. Bottom left is an AFM image of the electrodes region showing a limited over etching of the insulator. Bottom right is the expected capacitance variation as function of PM diameter as obtained by COMSOL simulation.
- 3 Schematic of one channel of the sensor (out of 32) showing the differential architecture of the sensing element made of two sets of equal interdigitated electrodes driven by counter-phased square-wave signals and sharing the common electrode connected to the charge preamplifier.
- 4 Close-up of the electronic schematic of each channel of the sensor.
- 5 Detail at transistor level of the Operational Amplifier OP1 of Fig. 4.
- 6 Lock-in demodulator scheme made of a passive Non-Return-to-Zero mixer and two low-pass  $g_m$ -C filters.
- 7  $g_m$ -C filter with current division and rail-to-rail input stage. The external voltage  $V_{p2}$  sets the bandwidth of the filter.
- 8 Experimental characterization of the Digital-to-Capacitance Converter (DCC) showing a differential non-linearity of less than 15aF
- 9 Schematic of the circuit performing low frequency noise shaping, acting on the transconductance of  $M_{p1}$  by setting the bias current  $I_{inj}$  through an external voltage  $V_{p1}$ .
- 10 Equivalent capacitive noise of a single channel as a function of the high pass frequency pole of the noise shaper that is tuned by changing the voltage  $V_{p1}$  applied to the 1 G $\Omega$  (see Fig. 9). The plateau of 56 zF certifies the extremely high performance of the system.

- 11 Microphotograph of the chip fabricated in standard AMS 0.35 $\mu\text{m}$  CMOS process: the total area is 2.4 mm by 2.5 mm, current dissipation is 25 mA at 3.3 V power supply and the sensitive area with microelectrodes exposed to air for dust collection is 1.1mm<sup>2</sup>.
- 12 Measured capacitive noise for each channel of the sensor showing an averaged resolution of 65 zF rms. The bandwidth of the measurement is tuned by changing the voltage  $V_{p2}$  of the  $g_m$ -C filters (see Fig. 7).
- 13 Example of real-time tracking of a deposition event. A single talc particle ( $\epsilon_r = 2.4$ ) of equivalent diameter  $\sim 5 \mu\text{m}$  (estimated from the subsequent microscope image) lands on channel 18, producing a capacitance variation of 10.6 aF (clearly detectable with a SNR = 125 set by an 80 zF rms noise floor at 80 Hz bandwidth). No measureable cross-talk is simultaneously observed in the adjacent channels (17 and 19) where no PM is depositing.
- 14 Summary scatter plot showing several talc deposition experiments **on the same chip**, demonstrating a detectable size range from 1  $\mu\text{m}$  up to more than 10  $\mu\text{m}$ . **Single events are reported.** The correlation between capacitance variations and particle equivalent diameters (a is  $\sim 12 \mu\text{m}$ , b is  $\sim 6 \mu\text{m}$  c is  $\sim 2 \mu\text{m}$ ) is consistent with what expected, despite the uncertainty in the shape analysis of the bidimensional microscope photographs taken after each deposition sequence. The inset reports the signal change for case c, where a 1.7 aF step is easily detected.