Fast fully-integrated front-end circuit to overcome pile-up limits in time-correlated single photon counting with single photon avalanche diodes

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Abstract: Time-Correlated Single Photon Counting (TCSPC) is an essential tool in many scientific applications, where the recording of optical pulses with picosecond precision is required. Unfortunately, a key issue has to be faced: distortion phenomena can affect TCSPC experiments at high count rates. In order to avoid this problem, TCSPC experiments have been commonly carried out by limiting the maximum operating frequency of a measurement channel below 5% of the excitation frequency, leading to a long acquisition time. Recently, it has been demonstrated that matching the detector dead time to the excitation period allows to keep distortion around zero regardless of the rate of impinging photons. This solution paves the way to unprecedented measurement speed in TCSPC experiments. In this scenario, the front-end circuits that drive the detector play a crucial role in determining the performance of the system, both in terms of measurement speed and timing performance. Here we present two fully integrated front-end circuits for Single Photon Avalanche Diodes (SPADs): a fast Active Quenching Circuit (AQC) and a fully-differential current pick-up circuit. The AQC can apply very fast voltage variations, as short as 1.6ns, to reset external custom-technology SPAD detectors. A fast reset, indeed, is a key parameter to maximize the measurement speed. The current pick-up circuit is based on a fully differential structure which allows unprecedented rejection of disturbances that typically affect SPAD-based systems at the end of the dead time. The circuit permits to sense the current edge resulting from a photon detection with picosecond accuracy and precision even a few picoseconds after the end of the dead time imposed by the AQC. This is a crucial requirement when the system is operated at high rates. Both circuits have been deeply characterized, especially in terms of achievable measurement speed and timing performance.

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1. Introduction

Time Correlated Single Photon Counting (TCSPC) is widely recognized as the technique of choice in many scientific applications where fast and faint optical pulses need to be recorded with picosecond precision [1]. For instance, in biological and biomedical sciences it represents the enabling technique for powerful investigation tools like Fluorescence Lifetime Imaging Microscopy (FLIM) and Förster Resonance Energy Transfer (FRET) [2–4]. In those applications a sample is periodically excited by means of a pulsed laser source; then single photons re-emitted by the sample are collected to form a histogram, depending on their arrival time within the excitation period. In this way it is possible to record the shape of the luminous pulse with incomparable resolution and noise performance. On the other hand, TCSPC is recognized as an intrinsically slow technique. Indeed, a typical TCSPC acquisition channel is not able to detect more than a photon during an excitation period, so every time a second photon impinges on the detector during a cycle it is not recorded and the histogram undergoes the so-called pile-up distortion [1]. Historically, TCSPC experiments have been carried out by limiting the excitation power to keep the average number of detected photons in a period well below unit (typically below 0.05) in order to reduce distortion under an acceptable level. However, this solution requires a large number of periods to collect a statistically relevant number of samples. In addition, modern TCSPC modules come along with a relatively long dead time which can last for hundreds of nanoseconds after a photon has been detected [1,5], thus contributing to further decrease the measurement speed.

In [6] we proposed a novel solution, aimed at maximizing the operating speed of a single TCSPC measurement channel avoiding, at the same time, that pile-up distortion affects the recorded curve. It requires the exploitation of an extremely fast converter, featuring a negligible dead time and a SPAD coupled to an Active Quenching Circuit (AQC) with finely tunable dead time. The exploitation of such a system permits to operate in an optimum working condition, where distortion approaches zero even when the experiment is performed at high detection rate. In particular, if the dead time is perfectly matched to the excitation period, it is possible to reach a measurement speedup of almost an order of magnitude with respect to the limit imposed by pile-up distortion [6], which can be further increased extending the proposed solution to a multichannel approach.

In this scenario, the AQC and the pick-up electronics used to sense the detection of a photon play a crucial role in enabling the exploitation of the proposed technique, since they concur to determine the dead time of the system. Considering a relatively fast excitation rate of 80 MHz, that is typical for mode-locked lasers used in medical and biological applications, the AQC must be able to set a fixed dead time as low as 12.5 ns after a photon is detected. In addition, both detector and pick-up circuit must switch back to the initial bias condition just after the end of the dead time, meaning that: i) the AQC must provide an extremely fast voltage transition on the SPAD to turn it on and, ii) the pick-up must be ready to sense the detector current with picosecond precision and accuracy immediately after the SPAD has been turned on.

In this paper we present a new integrated front-end, which combines the above-mentioned features with the ability to drive external custom-technology SPADs. Custom SPADs, indeed, have been proven to provide the best in-class performance [7], combining high Photon Detection Efficiency (PDE) in the infrared region [8] and low Dark Count Rate (DCR) [9]. In addition, the exploitation of custom detectors allows us to limit afterpulsing events, that is a critical point when a SPAD is operated with low dead time. For instance, in [9] we proved that an afterpulsing probability as low as 2% can be achieved with a 50-µm-diameter custom detector operated at 10-ns dead time.

The front-end includes a new AQC, which is able to activate an external custom SPAD from the cathode side in less than 2 ns at the end of a programmable dead time and a new trans-impedance pick-up circuit, which permits to sense the avalanche current of the detector from the anode side, ensuring excellent timing performance even when a photon is recorded just after the end of the dead time. A key feature of the proposed pick-up is a fully-differential structure able to reject electrical disturbances generated by the AQC during the fast reset of the detector at the end of the dead time.

The paper is organized as follows: a brief review of the dead time optimization technique proposed in [6] is given in section II, to better highlight the main requirements that quenching and pick-up electronics must meet. The architectures of the new AQC and pick-up circuits are described in section III. A TCSPC system exploiting the proposed front-end circuits has been fully characterized in terms of timing performance after the end of the dead time and experimental results are reported in section IV. Finally, section V concludes the paper.

2. Dead time and measurement speed in TCSPC systems

In typical TCSPC experiments two effects limit the maximum achievable measurement speed: on one hand pile-up distortion imposes that the rate of photons detected by the system is typically kept between 1% and 5% of the excitation rate, on the other hand the dead time related to the conversion electronics typically makes the system blind for many excitation periods after an event has been recorded, thus representing the major source of efficiency loss [1].

In [6], we theoretically proved that pile-up distortion can be reduced down to zero by using an extremely-fast conversion electronics, and a detector with dead time matched to the excitation period, thus paving the way to unprecedented measurement speed.

Concerning the conversion electronics, recent advances in time-measurement circuits allowed us to decrease the dead time associated to the electronics down to about 10 nanoseconds [10–12]. For instance, we recently proposed a converter based on an array of Time-to-Amplitude Converters (TACs), which is able to measure more than an event during each excitation cycle, given an average detection rate up to 80 MHz [13]. In addition, it features excellent performance in terms of timing jitter (as low as 20 ps FWHM) and Differential Non Linearity (better than 0.04 LSB peak-peak) [14]. In contrast with classic TCSPC measurement channels, where the maximum operating rate is limited by the finite speed of the converters, the exploitation of fast time-measurement circuits gives rise to a completely different situation, where the dead time of the detector represents the only source of counting loss. If the detector dead time matches the duration of the excitation period, distortion reduces down to zero, regardless of the rate of impinging photons [6]. It follows that a fine tune of the detector dead time permits to increase the detection rate well above the pile-up limit without facing any distortion effect. So far, some fast AQCs have been proposed in the literature, able to keep a SPAD blind for a dead time in the order of 10 ns [15–18], thus opening the way to an optimization of the dead time even when considering a relatively fast excitation rate of 80 MHz. For instance, in 2017 we proposed the first integrated quenching circuit able to operate an external 50-µm custom-technology SPAD with a finely tunable dead time as low as 10 ns [19].

In this scenario, the maximum achievable measurement speed strongly depends on the behavior of the AQC during the dead time. In particular, the time required by the AQC to reset the detector at the end of the dead time must be kept as low as possible in order to maximize the measurement speed, as detailed in [6]. This is a particularly critical point when using a high-performance custom SPAD. Indeed, the exploitation of a customized detector technology prevents the full integration of SPAD, readout and quenching electronics on the same silicon chip, making the parasitics related to external connections (e.g. bonding wires) to limit the settling time of the voltage transitions applied on the detector.

A fast AQC has been designed on purpose to cope with this problem, as explained in detail in the following section. Nevertheless, a quick reset of the SPAD voltage is not sufficient to take maximum advantage of a dead time matched to the excitation period. Indeed, it is also required that the system is able to record events with excellent timing performance just after the end of the dead time. To this purpose, we designed a dedicated pick-up circuit, that is described in section 3.2.

3. Active Quenching Circuit and current pick-up

3.1. Active Quenching Circuit

In order to maximize the operating speed of a TCSPC channel with dead time matched to the excitation period, we developed a new integrated AQC, designed in high-voltage 0.18µm CMOS technology from AustriaMicroSystems (AMS H18), which is able to drive an external custom-technology SPAD with a reset time in the order of 1.6 ns.

The simplified schematic of the AQC is shown in Fig. 1. It is based on the architecture presented in [18] but including some refinements to speed up the reset transition and to reduce disturbances generated during the reset phase. This AQC operates the detector from the cathode side, while a current-pick-up circuit is placed at the anode of the detector to sense the rising edge of the avalanche current generated at the photon arrival time with picosecond precision and represents the first stage of the time-measurement electronics. The AQC is composed of two high-voltage transistors M_Q and M_R, which are responsible for the quenching phase and the reset phase respectively, while three distinct logic blocks control the operation of the circuit: a sense stage, a high-side logic and a low-side logic. The exploitation of high-voltage transistors, able to support up to 50 V between drain and source terminals, gives us the possibility to generate high-voltage pulses at the AQC output. In this way, our AQC is compatible with a large variety of SPAD detectors, including the recently-proposed

Red Enhanced SPAD (RE-SPAD) [8], which features a remarkably high PDE of 40% at 800-nm wavelength. On the other hand, the logic circuits are based on low-voltage transistors, that combine high speed and low area occupation, but need to be biased below 2 V, which is the absolute maximum gate-source voltage set by the technology. In order to combine high-voltage operation of the AQC with low bias voltage of the control logic, every logic block is biased independently at 1.8V rail-to-rail, while a level shifter based on high-voltage transistors enables a communication between high-side and low-side logic (not shown in Fig. 1).
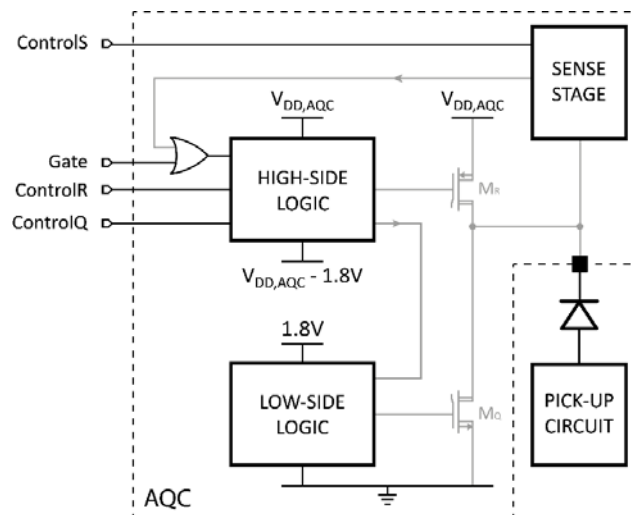

Fig. 1. Schematic of the proposed AQC. It features three distinct logic blocks, biased at 1.8V rail-to-rail, namely a sense stage, a high-side logic and a low-side logic, that control the operation of the AQC, while two high-voltage transistors (M_R and M_Q) are used to control the voltage level on the SPAD cathode. The pick-up circuit connected at the anode of the SPAD is used to sense the avalanche current generated by the detector and represents the first stage of the time-measurement electronics.

Every time an event triggers an avalanche, the SPAD current flows through the sense stage. Here the analog voltage *controlS* permits to adjust a threshold level that is used to identify the rising edge of the SPAD current. When the current crosses the threshold the sense stage sends a logic pulse to the high-side logic to start the quenching routine. First of all, the high-side logic communicates to the low-side logic to increase the gate voltage of M_Q, thus reducing the voltage applied on the detector below breakdown. After a fixed time, which depends on the voltage on the analog input *controlQ* [18], the high-side logic communicates to the low-side circuit to turn M_Q off, while M_R is turned on to start the reset phase, where the cathode voltage is forced to $V_{DD,AQC}$, i.e. the initial bias condition. In order to speed up the reset phase, that is a crucial point to increase the measurement speed, particular care has been devoted to the design of M_R. In particular, the W/L ratio has been sized to ensure higher conductivity with respect to the reset transistor used in [19]. After a programmable time, whose duration depends on the value of *controlR*, also M_R is turned off, so the AQC is able to enter a new quenching routine if a photon is detected. In this scenario, the overall dead time is given by the sum of two intervals: the first one where M_Q is on, that depends on the *controlQ* value, and the second one where M_R is on, that depends on *controlR*.

The circuit includes also a *Gate* input, which is used to gate-off the SPAD detector if needed. Given the schematic depicted in Fig. 1, *Gate* is combined with the signal coming from the sense logic by means of a OR gate, so when *Gate* goes high, the system enters a dead time, as in the case of a photon detection. It is worth highlighting that *Gate* can be forced at a high logic level for a duration which can be longer than the dead time determined by *controlQ*

and *controlR*. In this case, the system is kept in the hold-off phase until *Gate* returns to '0', then the reset phase starts in sync with the falling edge of the *Gate* signal. This feature will play a fundamental role in the system characterization which is described in section 4.

3.2. Duration of the reset transition

Given a dead time matched to the excitation period, the duration of the reset phase represents the major limitation to the speed of TCSPC measurements. In general, the duration of the reset transition depends on the speed of the voltage transient imposed by the AQC on the detector, which is related to the conductivity of M_R and to the effective capacitance of the SPAD at the cathode side. Nevertheless, other effects concur in determining the recovery time of the system after the end of the dead time.

On one hand, bonding wires used to connect electronics and detector to the external world do not behave as ideal conductors when the electrical parameters are subject to fast transitions. In particular, the presence of parasitic inductances associated to the interconnections can give rise to voltage oscillations at the SPAD terminals, induced both by the fast activation of M_R and by current pulses generated by the logic circuits. On the other hand, the activation of M_R leads to a fast voltage transition applied on the detector, which in turn gives rise to a high impulsive current flowing through the junction capacitance of the SPAD, which is injected in the pick-up circuit. This current can be sufficiently high to move the pick-up electronics far from its initial bias point; so the pick-up circuit requires a certain time to restore its initial bias condition. A similar effect is associated to voltage transitions applied on the gate of M_R by the high-side logic. Indeed, the presence of a large parasitic capacitance between gate and drain of M_R leads to a current pulse flowing toward the pick-up circuit as well. In this scenario, the reset transition can be considered concluded only when the whole system, including both detector and pick-up circuit, is back to the initial bias conditions. Therefore, a long recovery time of the pick-up electronics can represent a limit to the duration of the reset time.

In order to reduce the time needed to restore the initial bias condition of the system, particular care has been devoted to the design of both AQC and pick-up circuit.

Concerning the AQC, we provided the chip with two separated pads to bring the $V_{DD,AQC}$ voltage level to the logic circuits and to the source of M_R, thus avoiding that disturbances induced by the high-side logic on the $V_{DD,AQC}$ voltage level can affect the cathode voltage of the detector. Then, we designed the driver of M_R to have a relatively slow low-to-high transition, in order to limit charge injection through the gate-drain capacitance when M_R is turned off. Concerning the pick-up circuit, it has been implemented with a differential structure that features a high rejection to disturbances generated by the AQC.

3.3 Pick-up circuit

At present, the exploitation of a customized technology to develop SPAD detectors is the key to obtain the best performance in terms of detection probability, DCR and timing precision [7]. On the other hand, a dedicated pick-up circuit is required to take maximum advantage of the excellent characteristics of custom detectors. In 2017, Acconcia et al. presented an integrated Trans-Impedance Amplifier (TIA) followed by a fast voltage comparator, which enables to limit the timing jitter at 32 ps Full Width at Half Maximum (FWHM) when coupled with a custom SPAD [20].

Unfortunately, when a large current pulse is injected in a trans-impedance stage (e.g. during the reset transition), the amplifier can move away from its initial bias condition and a relatively long recovery time is required to restore the proper biasing of the circuit, that is in the order of 10ns for the circuit proposed in [20]. In this scenario, if a photon is detected during the recovery time the rising edge of the avalanche current is sensed with different delay and precision with respect to a photon observed when the TIA is properly biased; as a consequence, the system cannot be used at high-frequency operation. Recently, it has been

demonstrated that a differential architecture can reject disturbances generated by a fast reset of the detector thus enabling to record photons with picosecond precision and accuracy even when detected just after the reset transition [21,22]. In this paper we propose a differential readout based on two identical TIAs, which are integrated on the same chip. A schematic of the pick-up architecture is shown in Fig. 2. The circuit exploits two identical SPAD detectors, driven by the same AQC from the cathode side, while their anode terminals are connected to two integrated TIAs (TIA$_1$ and TIA$_2$), that read the current coming from the detectors at low input impedance. A fast differential comparator [20] combines the outputs of the two amplifiers to generate a voltage pulse which marks the photon arrival with picosecond precision. One of the detectors ("active" SPAD in Fig. 2) is biased above breakdown through the AQC output and is used to detect photons, while the other one is used as dummy cell ("dummy" SPAD in Fig. 2). In particular, the dummy cell is biased below breakdown (V_k in Fig. 2 is selected to keep the SPAD off), meaning that it is not able to detect any photon, and is AC-coupled to the AQC by means of a high-value capacitor (C in Fig. 2). Given that C is much higher than any parasitic capacitance associated to the detector, it behaves as a short-circuit during fast voltage transients at the AQC output. In this way, during the reset transition the path between AQC and TIA$_2$ features almost the same parasitics associated to the active path, so any current disturbance generated by the AQC at cathode side is injected in both amplifiers with the same magnitude. As a consequence, reset disturbances act as a common mode signal and are rejected by the differential comparator. Conversely, when the active SPAD detects a photon the avalanche current flows only through TIA$_1$, thus unbalancing the comparator input.
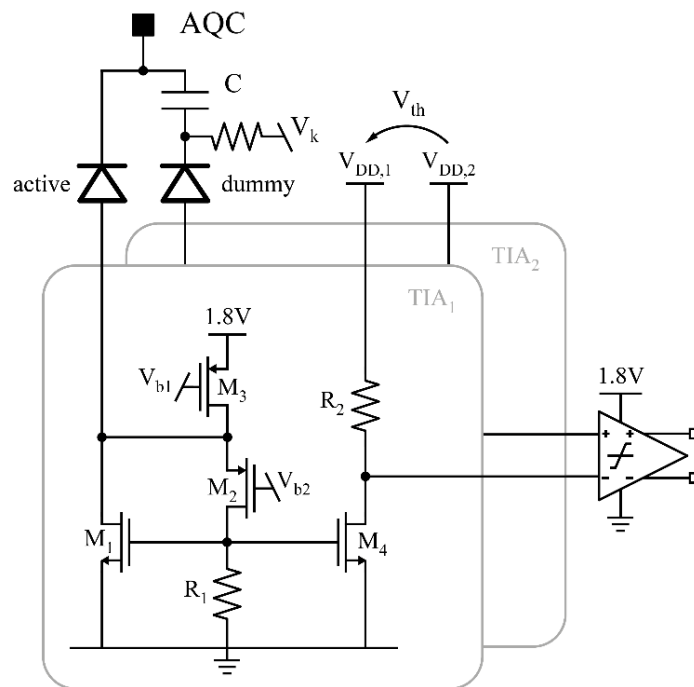

Fig. 2. Schematic of the differential pick-up circuit used to sense the avalanche current of the detector from its anode terminal. The pick-up is constituted by two identical trans-impedance amplifiers (TIA$_1$ and TIA$_2$) that read the current coming from two SPADs. The first detector is directly connected to the AQC and is able to detect photons ("active" SPAD), while the other one is kept off and used as dummy cell to replicate the parasitics of the active detector. In this way, any disturbance generated by the AQC gives rise to a common-mode signal at the comparator input and is rejected

The architecture of the TIAs shown in Fig. 2 is a simplified version of the circuit proposed in [20]. In particular, in [20] a positive feedback loop was exploited to reduce the input impedance of the amplifier at low and medium frequencies below 40 Ohms. Nevertheless, the presence of the positive loop came along with a long time needed to fully recover the initial bias condition after a strong current pulse was injected in the amplifier. To speed up the recovery time, the positive feedback loop has been removed, resulting in a simpler and faster architecture, at the expense of a bit higher input impedance. In any case, transistors have been re-sized to keep the input impedance below 60 Ohms over the entire frequency range.
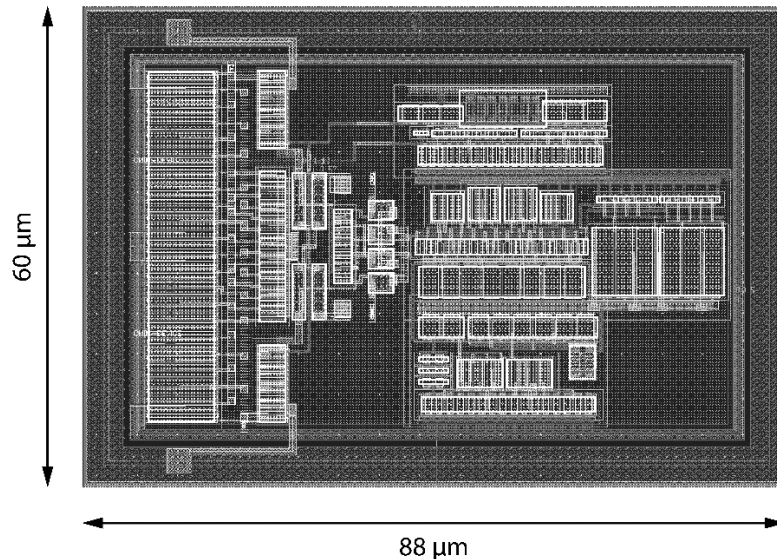

Fig. 3. Layout of the differential pick-up circuit, including the two trans-impedance amplifiers and the comparator

The proposed TIA includes two stages: the first one features a negative feedback loop (constituted by M_1 and R_1 in Fig. 2) to read the current at low input impedance, while the second one is a common-source configuration used to increase the trans-impedance gain of the amplifier. In addition, the second stage makes it possible to finely tune the voltage threshold used by the comparator to sense the rising edge of the avalanche current. Indeed, the pick-up is equipped with an independent pad to provide the positive power supply to the second stages of each TIA (that is $V_{DD,1}$ and $V_{DD,2}$ in Fig. 2). In this scenario, the voltage threshold V_{th} at the input of the comparator is given by the difference between $V_{DD,1}$ and $V_{DD,2}$. Particular care has been devoted to the layout of the overall pick-up circuit, which has been designed to be as symmetrical as possible to avoid any deterministic mismatch between the two amplifiers. Indeed, this is a crucial point to increase the rejection of common-mode disturbances. The layout of the pick-up circuit is shown in Fig. 3.

4. System performance
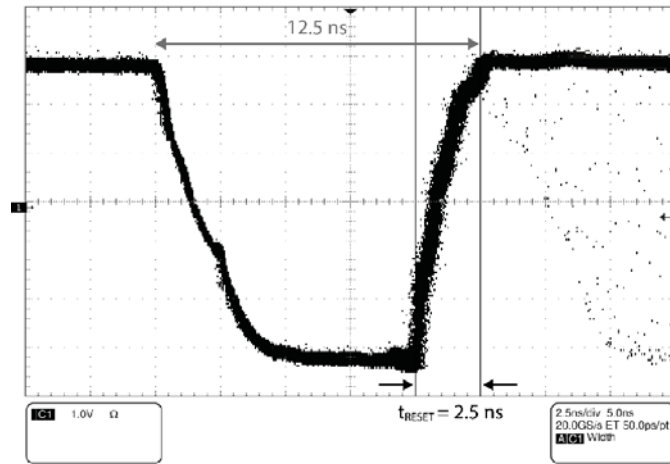
4.1 Experimental characterization

Fig. 4. Voltage transient at the detector cathode when a photon is detected. The AQC brings the SPAD below breakdown for a programmable hold-off time (here 10 ns), then the initial bias condition of the device is restored in about 2.5 ns (t_{RESET})
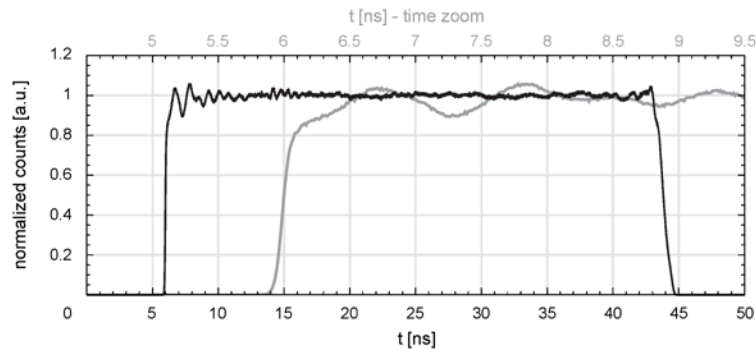

Fig. 5. Normalized distributions of recorded photons under uniform illumination (black curve) and time zoom around the rising edge (grey curve). The histogram has been recorded by turning on the detector periodically for 40ns within a much longer period and exploiting a LED to generate a uniform background light. The voltage threshold of the comparator (V_{th} in Fig. 2) is 200 mV

The presence of a finite reset transition, along with disturbances generated by the reset itself represents the ultimate limit to the measurement speed of a system operated with the dead time matched to the excitation period [6].

The voltage transition at the cathode side upon a photon detection is shown in Fig. 4 for a 50-um custom SPAD operated at 5V above the breakdown voltage. The cathode has been connected to a fast oscilloscope by means of a 0.5-pF capacitance to minimize the capacitive load affecting the AQC driver. When a photon is detected, the AQC lowers the cathode voltage to quench the detector and after a programmable hold-off time the circuit starts the reset phase. In the measurement of Fig. 4 the hold-off interval has been adjusted to obtain a dead time of 12.5 ns, while the measured reset transition is as short as 2.5 ns.

However, it is worth highlighting that the unavoidable presence of residual parasitics associated to the oscilloscope probe and the limited bandwidth of the probe itself (about 1.5 GHz) can limit the maximum speed of the observed voltage transient.

In order to get a more accurate estimation of the reset transition, we performed an indirect measurement of the settling time of the system. A noninvasive way to estimate the duration of the reset transition consists in recording the distribution of events generated by a continuous illumination of the device, when the AQC is operated in gated mode [21,22]. To this purpose, we exploited a low-jitter pulse generator [23] to drive the *Gate* input of the AQC with a programmable square wave, so that it was possible to periodically force the active SPAD in hold-off and activate it for a fixed duration of 40 ns within each period; then we used a LED source to illuminate the active detector in a dark environment, ensuring that the average number of photons in a period was limited well below 0.1, to avoid pile-up distortion. A commercial TCSPC module (Becker&Hickl SPC-130) allowed us to collect recorded events in a histogram, depending on their arrival time within the *Gate* period. Given a uniform distribution of photons over time, an ideal system would lead to a rectangular histogram with duration equal to 40 ns, that is the time the SPAD is on. Conversely, if the system needs a certain settling time to recover the initial bias conditions, the histogram would feature a gradual off-on transition, followed by some oscillations whose amplitude tends to reduce as a function of time. The distribution of counts obtained with the proposed system is shown in Fig. 5. The histogram features an extremely short rise time of about 250 ps, followed by some peaks with decreasing amplitude.
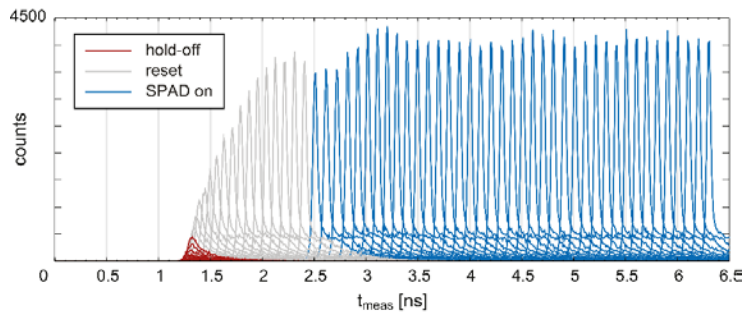

Fig. 6. Histograms obtained with a pulsed illumination at different excitation instants, spaced at steps of 100 ps. Here the x-axis represents the measured arrival time of photons, so the space between histograms is 100 ps only if no distortion occurs. Different colors indicate different phases where the laser excitation takes place. The voltage threshold of the comparator (V_{th} in Fig. 2) is 200 mV

Unfortunately, it is not possible to evaluate the real duration of the reset interval from this result, since the shape of the histogram does not reflect in general the real voltage transition applied on the detector. In particular, the result is an underestimation of the reset transition, as will be demonstrated in the following.

In order to evaluate the real behavior of the system during the detector reset, we exploited a laser diode with pulse width of 10 ps (Antel MPL-820 laser module) to illuminate the SPAD at different excitation instants t_{exc} separated by steps of 100 ps in the proximity of the reset transition; then for each t_{exc}, we recorded events in a histogram for a fixed collection time of 60 s. The result of this measurement is reported in Fig. 6. Here each histogram is related to a different excitation instant, while the x-axis represents the measured arrival time of photons t_{meas}, that corresponds to t_{exc} only in the case of ideal acquisition. A careful analysis of the measurement reported in Fig. 6 permits to discriminate three different operating regions, that are indicated in Fig. 6 with different shades of gray: a hold-off, where the detector is kept below breakdown by the AQC (red), the reset transition (gray) and the time after the reset interval (blue), where the system can be considered at regime ("SPAD on" in Fig. 6).

In order to discriminate the different operating regions, the major timing performance of the system have been extracted from the measurement shown in Fig. 6 and plotted in Fig. 7 as a function of the excitation instant t_{exc}. In particular, Fig. 7(a) shows the deviation of the peak position of the histograms reported in Fig. 6 from the time-instant that corresponds to the real

photon absorption, while the Full Width at Half Maximum (FWHM) of the histograms is reported in Fig. 7(b). Finally, Fig. 7(c) reports the total number of events collected in the histograms as a function of t_{exc}, that reflects the PDE of the system as a function of time.
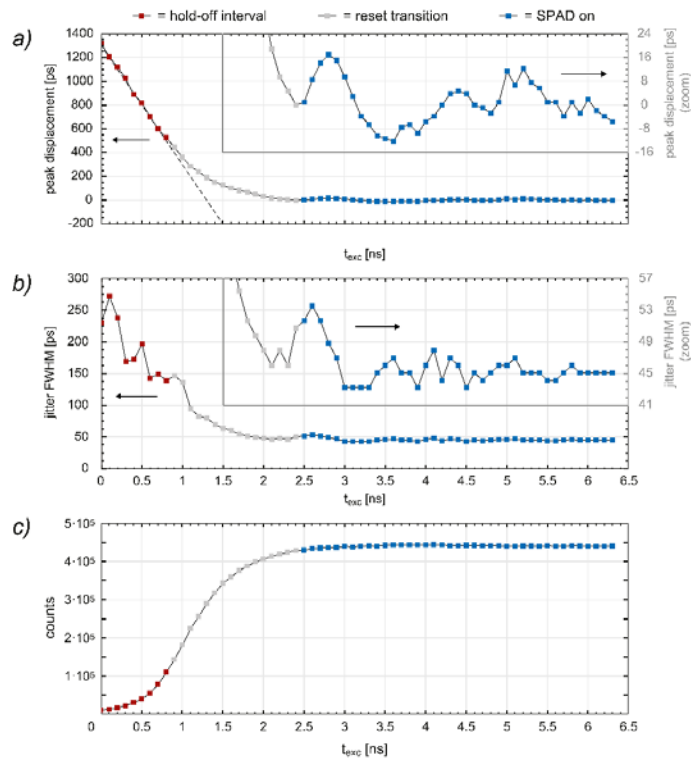

Fig. 7. Detailed analysis of the measurement reported in Fig. 6. a) displacement of the peak positions of the histograms with respect to their ideal position (it is the difference between the peak position expressed as a function of t_{meas} and t_{exc}); b) timing jitter expressed in terms of FWHM of the histograms; c) total number of counts collected in each histogram. The curves are plotted as a function of the excitation instant t_{exc}

When the laser pulse is located far from the reset transition (that is at high values of t_{exc}), the system is at steady-state. In this scenario, the peak displacement shown in Fig. 7(a) approaches zero, meaning that histograms are placed at a time-instant that corresponds to the position of the laser pulse (that is t_{exc} corresponds to t_{meas}). Conversely, when the laser pulse is positioned in proximity of the reset transition, a strong distortion affects the accuracy of the system. In particular, during the hold-off time the peak displacement decreases linearly as a function of time and features a slope equal to one [see the dashed line in Fig. 7(a) as a reference], meaning that histograms belonging to the hold-off phase are all placed in the same position in Fig. 6. This phenomenon has a simple explanation: during the hold-off time the voltage on the detector is kept below breakdown, meaning that an electron-hole pair generated during this phase by a photon absorption cannot give rise instantaneously to an avalanche; however, it can diffuse in the device until the SPAD is turned on. It follows that photons absorbed during the hold-off interval give rise to a histogram whose peak position corresponds to the instant when the SPAD is turned on, that is the beginning of the reset interval, regardless of the excitation time t_{exc}. At the same time, the probability that photons absorbed during the hold-off give rise to an avalanche is related to the lifetime of carriers diffusing in the device, so it decreases exponentially with the time distance between the absorption instant and the reset transition. This effect can be observed in Fig. 7(c), where the first part of the curve features an exponential behavior, whose time-constant has been verified

to be equal to the lifetime of carriers in the device, which can be extracted from the exponential diffusion tail of not-distorted histograms, located on the right end of Fig. 6.

After the hold-off phase, the system enters the reset interval, where the voltage applied on the SPAD increases gradually from the breakdown value up to a regime, meaning that also the PDE increases. As a result, the number of counts collected in the histograms increases accordingly with the PDE, until it reaches a steady-state value, as can be observed from Fig. 7(c). During this interval, the peak displacement depicted in Fig. 7(a) shows a gradual transition toward zero. Indeed, the voltage applied on the device does not influence only the PDE, but also the slope of the current edge generated by an avalanche: the higher the voltage, the faster the rising of the avalanche current. In this scenario, given a fixed threshold used by the comparator to sense the avalanche current, a photon detected at the beginning of the voltage transition is sensed with a higher delay with respect to a photon detected at the end of the reset interval. It is worth noting that this effect leads to a
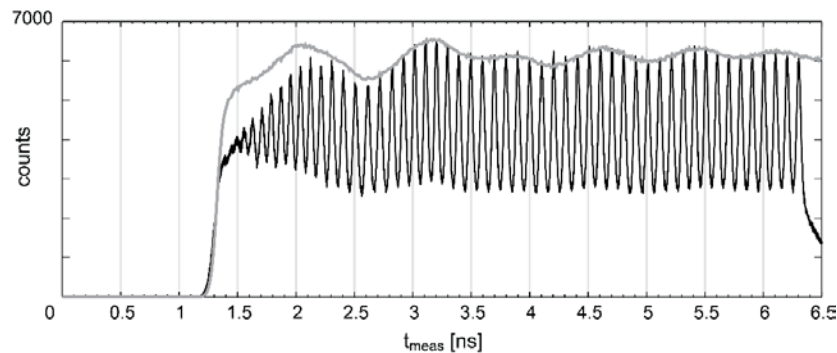

Fig. 8. Comparison between the sum of the histograms reported in Fig. 6 (black curve) and the histogram obtained for a constant illumination (see Fig. 5), here multiplied by a scale factor (grey curve)

compression of the initial part of the time-of-arrival histogram at constant illumination, resulting in a measured off-on transition as short as 250 ps, as shown in Fig. 5. Conversely, the results reported in Figs. 7(a) and 7(c) reveal that the actual duration of the reset transition is around 1.6 ns.

The compression effect can be demonstrated by summing the histograms in Fig. 6: indeed, a uniform illumination can be split in a superposition of illumination pulses occurring at different time instants, and the curve reported in Fig. 5 can be obtained by summing the histograms collected at pulsed illumination. The result is shown in Fig. 8, where the sum of histograms reported in Fig. 6 (black curve) is compared with the histogram reported in Fig. 5 (grey curve), which has been multiplied by a scale factor. As expected, the sum of histograms features a fast rising edge, given by the higher concentration of histograms at low values of t_{meas}. It is worth highlighting that the measurements reported in Figs. 6 and 7 have been performed with relatively large steps of 100 ps, so the sum of histograms reported in Fig. 8 slightly differs from the histogram obtained at constant illumination. In particular, for high values of t_{meas} the spacing between histograms is almost regular (i.e. 100 ps), so the sum is a sampled version of the grey curve reported in Fig. 8. Conversely, for low values of t_{meas}, histograms tend to concentrate in a short interval (see Fig. 6) and the large time step between excitations (in this case 100 ps) leads to a significant reduction of the events that sum up in the same location, meaning that the black curve reported in Fig. 8 features a lower amplitude if compared with the grey curve.

4.2. Measurement speed

Given a TCSPC system with a detector dead time matched to the excitation period, distortion is kept around zero if any photon detected during the dead time is discarded [6]. In this

scenario, the efficiency of the system strongly depends on the fraction of dead time where the system is able to detect photons, that is mainly related to the duration of the reset transition operated by the AQC. For instance, in [6] a remarkable speedup of a factor 8 with respect to a pile-up limited situation has been theoretically demonstrated for a reset time of 4 ns, considering a relatively short dead time of 12.5 ns. Given the AQC proposed in this paper, the detector reset lasts for about 1.6 ns, so the expected speedup is even higher.

On the other hand, the timing performance depends on the ability of the system to measure every photon arrival with the same precision and accuracy, so it is of utmost importance that the system can be considered at steady-state immediately after the end of the dead time. In this paper, the differential architecture of the pick-up circuit permits to record photons with high timing performance even few picoseconds after the end of the reset transition. Indeed, the maximum FWHM after the reset is limited to 53.6 ps [see the zoom in Fig. 7(b)], while the peak displacement is kept below 30 ps peak-to-peak, as highlighted in Fig. 7(a).
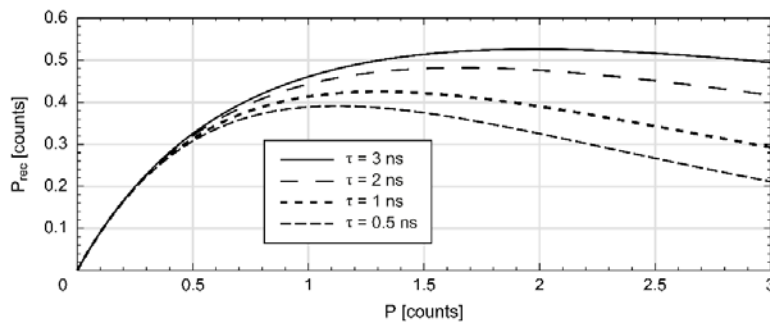

Fig. 9. Average number of recorded photons in a period (P_{rec}) as a function of the average number of photons impinging on the SPAD (P). The curves refer to the system described in the paper when operated with a dead time matched to an excitation period equal to 12.5 ns. τ is the fluorescence time-constant of the luminous pulse analyzed during the TCSPC experiment

Based on the mathematical approach reported in [6], we calculated the impact of the proposed system on the speed of a TCSPC experiment. Figure 9 shows the average number of events recorded in a period, P_{rec} (that is proportional to the measurement speed) as a function of the average number of photons impinging on the detector during an excitation cycle, P, for different values of the fluorescence lifetime τ. It is evident that the maximum of the measurement speed depends both on the rate of impinging photons and on the fluorescence time-constant. In any case, the system is able to operate at an average number of recorded photons of 0.4, that is a factor 8 higher than the typical 0.05 pile-up limit, even considering a relatively low τ of 500 ps, while even better results are obtained for higher values of the lifetime.

5. Conclusions

Recently, it has been demonstrated that a TCSPC channel with a dead time matched to the excitation period can be operated at unprecedented measurement speed, well above the classic pile-up limit. In this scenario, the system must be able to keep the detector blind for a well-defined interval and reset it with an extremely fast reset transition. In addition, picosecond precision and accuracy must be guaranteed immediately after the end of the dead time, in order to avoid any distortion of the recorded histogram.

In this paper we presented two integrated circuits specifically designed to meet these requirements: a fast AQC and a fully differential pick-up circuit. The AQC is able to drive an external custom-technology SPAD from the cathode side with a reset transition as short as 1.6 ns and a finely tunable dead time. The fully- differential pick-up circuit makes it possible to read the detector current from the SPAD anode ensuring excellent timing performance even a few picoseconds after the end of the reset transition imposed by the AQC.