Assembly and soldering procedure of non-stabilized YBCO coils for 1000 A SFCL

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***Abstract*— The Superconducting Fault Current Limiter (SFCL) is the superconducting device for electrical applications closest to overcoming the commercialization threshold. Device and operational costs due to resistive electrical connections and AC losses can be minimized by reducing superconducting tape length and power dissipation in the cryostat. Pursuing this goal, we realized anti-inductive coils of YBCO tapes without a copper stabilizing layer. The higher normal-state resistance allows considerable reduction of the necessary length, for the same current limitation factor. The focus of this work is on the soldering procedure and reinforcement of the superconducting tapes, particularly challenging when it is protected by only a 2 μm thin Ag layer. Our developed procedure enabled the realization of the successfully tested single phases of the 9-kV/15.6-MVA resistive SFCL, currently under development at Ricerca sul Sistema Energetico-RSE S.p.A.**

***Index Terms*—Fault current limiter, high-temperature superconductors, soldering, resistive connections.**

I. Introduction

Current trends in the energy market are reshaping the electrical grid. A steady increase in the number of energy generators, independent power producers and distributed generation contribute to increasing network interconnectivity. These changes increase the probability of harmful short circuit currents (I_{SC}), pushing utilities to develop new solutions to maintain the required service quality. Superconducting Fault Current Limiters (SFCL) offer a unique opportunity to create an efficient and cost-effective method for protecting the grid and guarantying power quality, thus delaying expensive grid upgrades [1]. Under nominal conditions, the device is completely transparent in the installed grid, having no resistance and inductance. In case of short circuit, the increased current immediately triggers the transition from superconducting to resistive state, introducing a resistance in the grid and limiting the short-circuit current. Once the current returns to its nominal value, the superconducting state is restored and the SFCL returns to being a transparent element of the grid.

Such features have triggered the interest of utilities and manufacturers toward the realization and field testing of SFCL [2-4]. These experiences also offer a valuable opportunity to prove the value of High Temperature Superconductors (HTS) for electrical applications [5]. Our research group has successfully realized and installed a BSCCO-based resistive-type 9 kV/3.4 MVA SFCL in the Milano MV distribution grid [6]. The test was concluded after 2 years of service and the successful limitation of a severe three-phase short-circuit event [7]. Following to this success, an upgraded version, 9 kV/15.6 MVA SFCL, will be developed for the same grid substation.

In the design phase we adopted HTS YBCO-coated conductor tapes, because of the higher critical current (I_C), lower AC losses and higher normal state resistance compared to BSCCO tapes. In spite of these positive aspects, several issues appeared: less uniform critical current density (J_C) distribution, non reproducible low resistance junctions and low stress tolerance. In this paper we present and justify the assembly procedure adopted to realize the superconducting coils for the 15.6 MVA SFCL.

We will first explain the development of a technologically convenient and reliable soldering procedure. The tests involve both tape splices (YBCO tape with YBCO tape) and tapes junctions with copper current leads. Soldered connections were investigated by electrical measurement, scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS). To increase thermal and mechanical stability, the assembled coils were impregnated in a glass fiber reinforced epoxy (GFRE). Winding and impregnation procedures were designed to minimize radial stress and avoid performance degradation after thermal cycles and short circuit events. Electrical characterizations were performed to evaluate the HTS status and the coil properties. The final anti-inductive coil was finally tested in a simulated short circuit event [8].

II. Experimental Procedure

In this project 12 mm wide YBCO-coated conductors manufactured by SuperPower Inc. were adopted. The same tape chosen for the final SFCL device. The tapes are made of a 100 μm thick Hastelloy substrate, where a 200 nm thick buffer layer is deposited by Ion Beam Assisted Deposition (IBAD), and a 1μm thick epitaxial YBCO film deposited on top by Metal Organic Chemical Vapor Deposition (MOCVD). The adopted tape has only 2 μm of sputtered silver cap layer and no copper stabilizer. This limit normal state conductivity, reducing the length of superconducting tape necessary to have the same limiting factor, and considerably reduce the final device cost.

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A. *Electrical connections*

Reliable and low resistive electrical connections between two HTS tapes and between the tape and current lead are paramount for the realization of the device. To be successful, the procedure must satisfy the following technological constraints:

1) Temperatures below 250 °C, to avoid alteration of superconductor properties and I_C decrease.
2) Avoid removal of Ag cap layer, to ensure solderability and uniform current injection.
3) Limited mechanical stresses on the YBCO film.
4) Avoid thermal treatment in special atmosphere of the realized component.

Following the successful results reported in the literature [9-11] we decided to solder all of the electrical connections. To avoid dissolution of the thin Ag capping layer (2 μm) it was necessary to use an eutectic alloy of silver, such as $Sn_{96.5}Ag_{3.5}$ or $Sn_{62}Pb_{36}Ag_2$ [12]. For a better obtained performance we adopted $Sn_{96.5}Ag_{3.5}$ alloy (T_{melt}=221 °C), in tapes containing flux (RESINFLUX T3). To splice and solder the YBCO tapes we modified the current leads, to use them as heating elements. Transforming the current lead into an active component during assembly is a practical and flexible approach when different geometries are present in the device, and access with a specific tool is not always possible. Controlled heating for soldering was realized with two resistive heaters and a Pt-100 thermometer, inserted in specifically designed cavities of the current leads. A LakeShore temperature controller ensured accuracy of +/- 3 °C at 230 °C.

B. *Soldering procedure*

We soldered the YBCO tape to the current leads by the following steps (Fig. 1). 1) Degrease the surface of the HTS tape and the current lead with ethanol. 2) Turn on the heating system until the soldering temperature (230°C) is reached and is stable. 3) Cover the surface of the current lead first with flux then with soldering alloy containing flux. 4) Pull the HTS tape with a tension of approximately 25 N to make it adhere to the current lead, and add further soldering alloy to cover it completely. 5) Turn off the heating system and let natural cooling occur, while keeping the tape under tension until complete solidification of the alloy.

When splicing two tapes, a similar procedure as before was used. A 25 μm thick Kapton foil avoided undesired soldering between the tapes and the heating element. Before soldering, ribbons of soldering alloy were sandwiched between the two tapes. In all tests and for the final devices the tapes overlapped for approximately 7 cm. We use adhesive Kapton to keep the tapes connected and aligned. Because the YBCO tapes are asymmetric (HTS is on one side only), two soldering configurations were possible: face-to-face and back-to-face. In the first case, the superconductors were separated by few microns of soldering alloy and silver, resulting in low resistance (below 10 nΩ). In the back-to-face configuration, the Hastelloy substrate between the superconductors increased the joint resistance to 100 nΩ range. Both types of joints had the same reliability and relative variance, confirming the procedure quality.

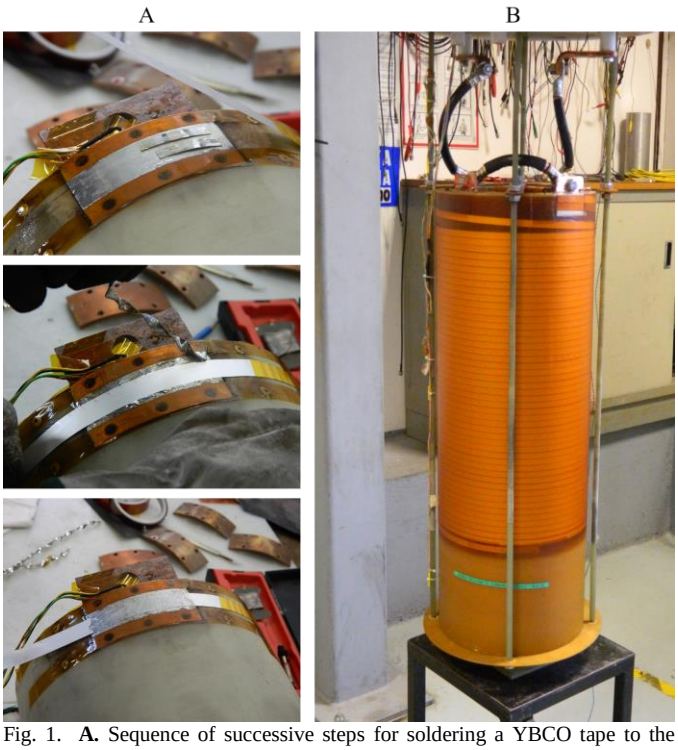

Fig. 1. **A.** Sequence of successive steps for soldering a YBCO tape to the current lead (steps 3 and 4 in the text) **B.** Assembled YBCO coils, after GFRP impregnation and cure. In the picture two concentric coils are connected in parallel for a short circuit test.

Compared to other proposed systems we did not compress the splice with specific equipment. The results obtained with a controlled compression offer comparable performances [9], while introducing practical obstacles in the realization of the final coil for the device. We believe that high quality electrical connections are realized when the soldering material is homogeneously distributed along surfaces. This is achieved by the progressive adhesion of the tape above the melt alloy.

Mechanical performances of the soldered joint are nearly independent of the soldering procedure. Above the critical stress, cracks nucleate and propagate in the ceramic layers between the buffer oxides and the HTS [13]. For this reason, we reinforced the coil and the current leads connections by encapsulating the final assembly with pre-impregnated GFRE. The external encapsulation is designed to reduce the harmful radial stress on the joints, developed during the short circuit event.

C. *Coil winding and GFRE impregnation*

To realize the coils, YBCO tapes were wound on a G10 composite cylinder in an anti-inductive configuration. A specifically designed winding machine controlled tension and pitch, ensuring no damage of the superconductor. The tape, was first soldered on the current lead, helically wound around the cylindrical support until half of the coil length. A second tape of same length was then spliced to the end of the first in a back-to-face configuration, than wound to create an anti-inductive coil. Once fully wound, the second tape was soldered to the other current lead. Adhesive Kapton, 25 μm thick and 24 mm

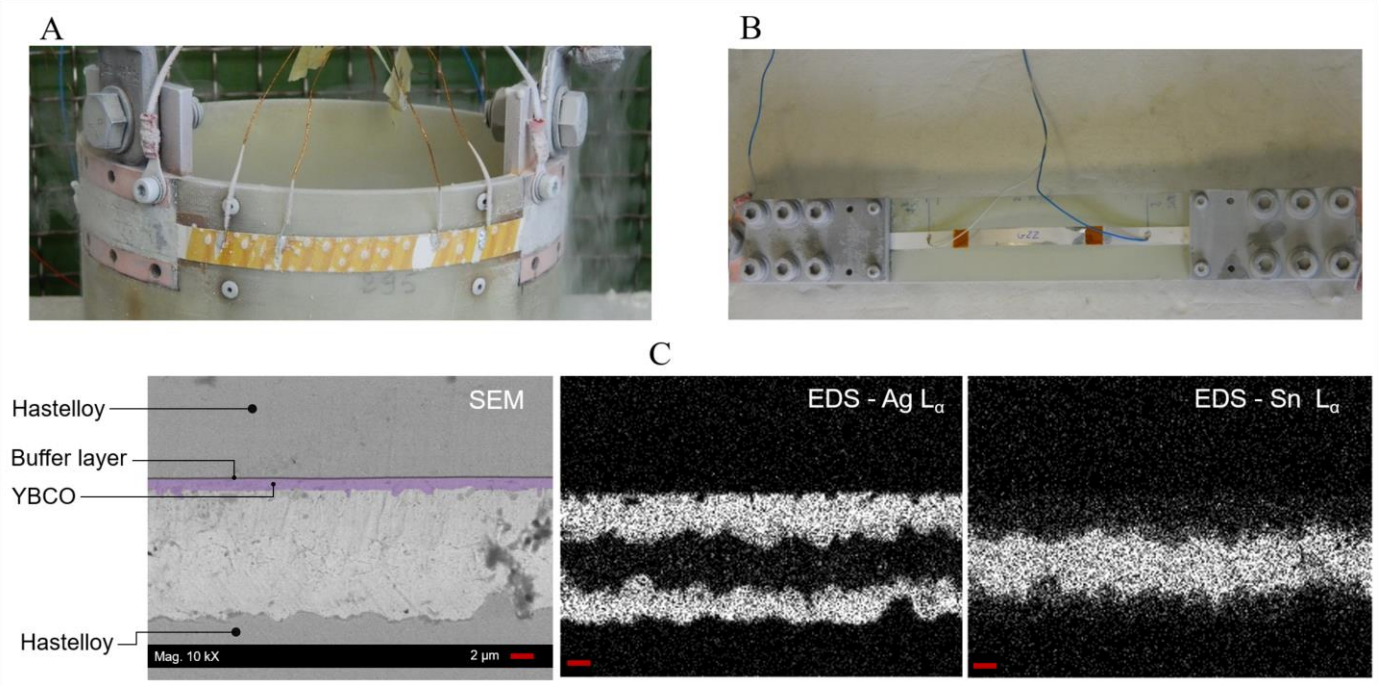

Fig. 2. Experimental setup for electrical characterizations. **A.** Tape soldered to the test coils support, with electrical connection to measure I_C and resistivity of the soldering to the current leads. **B.** Curve splice between two YBCO tapes, the electrical contact with the current leads is realized by pressure using In foils to ensure optimal electrical contact. **C.** SEM and EDS images of a back-to-face splice between YBCO tapes. False color is added to highlight the YBCO layer, buffer layer appear as dark line thanks to atomic mass contrast. EDS image shows interdiffusion of Sn in the Ag layer, which preserve its original thinness.

wide, was wound together with the HTS tape to ensure insulation in the same helix. Two 50 µm thick Kapton foils separated the two helix providing the electrical insulation necessary during the short circuit event, when high tension differences occurred between the two ends of the coils, placed on top of each others. This solution was successfully adopted for the live-tested device [6], and the results from the short circuit tests (coil end-to-end ΔV 5 kV) confirmed its effectiveness for the new SFCL. Once completed the tape winding, another 50 µm Kapton foil cover the entire coil. To increase mechanical and thermal stability the coil is finally encapsulated with a pre-impregnated glass fiber reinforced epoxy. Curing and impregnation were carried in a vacuum bag with a specific thermal cycle, reaching a maximum temperature of 120 °C for 30 min. In this phase, the Kapton foils hindered the formation of shear stresses on the superconducting tape during encapsulation and thermal cycles. The observation is in agreement with the results of Yanagisawa et al. [14].

III. Characterizations

Microstructure and chemical analysis were studied using a Zeiss Supra 40 Field Emission SEM equipped with EDS. The soldered splice was cut without inducing delamination, then mounted in an epoxy resin and polished.

The resistance and critical current of the test samples (Fig. 2 A,B) and final coils were measured at 77 K via four-point method. Two concentric coils were assembled and underwent two 80 ms short circuit tests in the high-power facility of CESI Milan, the first at the reduced prospective short-circuit current (I_{PSC}) of 6 kA_{rms}, and the second at the full I_{PSC} of 10.6 kA_{rms} [8].

IV. Results

A. Soldering

Soldering involves the diffusion of the solder alloy for few µm inside the metal interface. To avoid removal of the Ag coating, which ensures good electrical contact, only silver eutectic alloys can be used. Concerning the latter, the enrichment of silver increases the liquidus temperature, avoiding the coating dissolution at a temperature close to melting point ($T_{eutectic}$). The electron microscopy image (Fig. 2 C) shows a uniform microstructure in the soldering. From EDS the coating layer was recognizable and its thickness was unchanged. It was possible to observe the presence of Sn diffused during the soldering.

Splices and soldering to the current leads showed low and constant resistivity (Fig. 3 A), making the procedure suitable for the realization of the final electrical grid device. The average resistance of the four realized and tested coils was 218 nΩ at 77 K, with a standard deviation of 9.4 nΩ. The device had two current lead joints and one back-to-face splice. Because of the low total resistance and no failures, we preferred not to add two further splices to have face-to-face connections only.

B. I_C stability

Critical current degradation in HTS tapes can be triggered by cracks in the superconducting material or alteration of its stoichiometry and microstructure. The adopted process avoided both, ensuring pristine properties after assembly (Fig. 3.B). The maximum temperatures adopted were below the safety limit, and were applied for a short amount of time: 230 °C for less than 1 min for soldering, and 120 °C for 30 min for GFRE encapsulation.

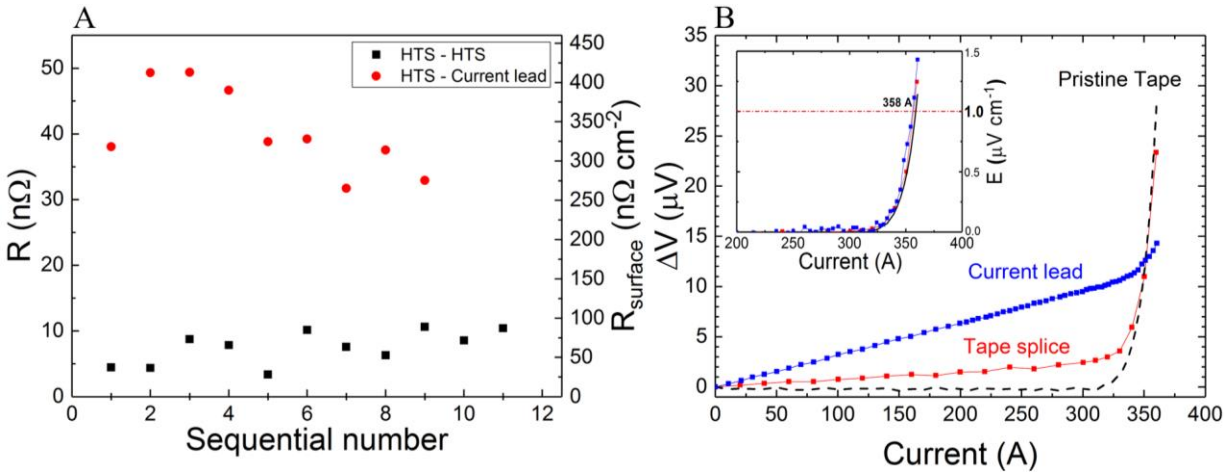

Fig. 3. **A**: Resistance of the tested joints with current leads and face-to-face splices, measured at 77 K. The soldered area is the same in both cases (7 cm), allowing use of the same scale to compute resistance per unit area ($R_{surface}$). **B**: Critical current measurements showing no I_C degradation after soldering. In the inset shows current vs electric field across the pristine tape and junctions after removal of resistive contribution. The I_C is defined as the current at 1 μV/cm.

The insertion of Kapton between the superconductive tape and GFRE avoids direct loads transfer, thus hindering I_C degradation during assembly and thermal cycles.

Commercial insulated tapes are not appropriate for SFCL applications. The realized insulation by the producer causes indentations in the tape, thus decreasing I_C. The indentations were suspected to cause critical current density (J_C) inhomogeneity, acting as the starting point for a destructive localized quench. The use of non-insulated tapes, and the introduction of a Kapton layer during winding was a practical and easy implementable solution to increase device performances.

V. Conclusion

We have reported the procedure for the successful realization of HTS coils of non-stabilized second-generation tape for a projected live-grid resistive SFCL. The coils were successfully tested in a simulated short-circuit event with prospective currents up to 10.6 kA_{rms} [8]. During the test the device performed as expected, limiting the current by a factor of 1.7. The main achievements for the realization of the device are:

1) Reliable soldering procedure for non-stabilized tape, ensuring low resistance, no I_C degradation and reproducibility.
2) Identification of winding and encapsulation procedures that avoid load transfer to the superconducting tape during assembly and service, ensuring no I_C degradation.

Current developments are progressing toward realization of the final device. Further research of the analysis of the mechanical stress in the coils during thermal cycles and fault events is necessary to complete the projected device. Is also necessary to evaluate the effect of J_C inhomogeneity in the superconductor cross-section during quenching.

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