A 15 GHz Broad-band ÷ 2 Frequency Divider in 0.13 μm CMOS for Quadrature Generation

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***Abstract*—This paper presents a 0.13 μm CMOS frequency divider realized with an injection-locking ring oscillator. This topology can achieve a larger input frequency range and better phase accuracy with respect to injection-locking LC oscillators, because of the smoother slope of its phase-frequency plot. Post layout simulations show that the circuit is able to divide an input signal spanning from 7 to 19 GHz, although the available tuning range of the signal source limited the experimental verification to the interval 11-15 GHz, 31% locking range. The divider dissipates 3 mA from 1.2 V power supply.**

***Index Terms*—Frequency division, injection locked oscillators, ring oscillators.**

I. Introduction

FREQUENCY dividers are employed in modern tranceivers both in the feedback path of Phase Locked Loops (PLL) and to generate the I/Q quadrature signals necessary in zero- or low-IF receivers. The design of a fully integrated CMOS divider is critical, above all for its power consumption that is comparable to the one of the Voltage Controlled Oscillator (VCO). Moreover, wide input frequency range and good quadrature accuracy are required in many applications.

We discuss a topology for a ÷2 frequency divider for I/Q generation in a WLAN transceiver for IEEE 802.11a/b/g standards. In the frequency synthesizer only one VCO will be employed, and a first divider must provide the I/Q signals for the 802.11a channels. Then, a following divider makes the signals for the 2.5 GHz band available. Given the channellizations of the standards, the input frequency of the first divider must vary between 9.6 and 11.6 GHz, leading to 18 % input tuning, or locking, range. In order to cover the process spreads, a larger tuning range, up to 30 %, must be targeted. In the next section we will recall why such high tuning range makes not possible to adopt some recently presented low-power solutions, as LC injection locking topology. Then in Section III we discuss the proposed dividers and, in Section IV, we show why this circuit can achieve a wide tuning range thanks to its phase-frequency characteristic. In Section V we present some experimental results, then the conclusions will follow.

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II. High Speed Frequency Dividers

Typically, ÷2 dividers are realized by two D-flip flops in a negative feedback loop, [1]. For multi-GHz input signals, these circuits have a differential current-steering structure that allows fast current switching, sometimes called source-coupled logic (SCL). To reduce the dissipation alternative topologies have been considered in literature, for instance a dynamic logic is employed in [2]. This circuit, however, does not provide I/Q outputs. Probably, the best solution in term of power consumption is to differentially drive two injection locking LC oscillators, as in [3]. The dissipation is substantially reduced, because of the resonant tanks, at the cost of a large area occupation. Unfortunately, this approach is intrinsically narrow band: if the quality factor Q of the LC tanks is lowered, to increase the divider locking range, the dissipation rises. Our tuning range requirements demand a low Q, between two and three, practically voiding the effect of the LC resonance. In this sense, power is traded not only with speed, but also with input locking range. A further example of this trend is the 40 GHz divider in [4], which shows good power performance but features only a 6 % tuning range.

III. Two Stages Ring Oscillators

Since we have to cope at the same time with high input frequency and wide locking band, we decided to injection-lock a two-stages ring oscillator, using the VCO differential outputs. An approach similar to ours was presented in [5] where, however, a different circuit topology is adopted and only simulation results are shown.

The divider is shown in Fig.1, together with the transistor-level scheme of one stage. The transfer function of the single stage can be approximated as:

$$T(s) = T_0 \frac{1 - s/\omega_z}{1 + s/\omega_p} \qquad (1)$$

The small signal dc gain is $T_0 = g_{mi}R/(1 - g_{mc}R)$, being g_{mI} and g_{mc} the transconductances of transistors M_1-M_2 and M_3-M_4 respectively. The dominant pole frequency is $\omega_P=(1-g_{mc}R)/C_OR$, where C_O is the output load capacitance. The transfer function also exhibits a right half-plane zero at higher frequency, $\omega_Z = g_{mi}/C_{gd}$ due to the gate-drain overlap capacitance of the input couple M_1-M_2. To achieve stable oscillation, the Barkhausen criterion for loop phase requires a

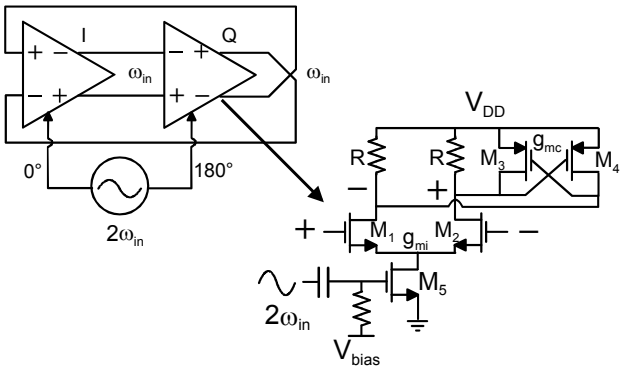

Fig. 1. Ring frequency divider driven by a differential VCO. The scheme of one stage is also shown.

lag of $-\pi/2$ radians for each stage, providing in this way the quadrature outputs. The cross-connection between the two stages in Fig.1 gives the remaining phase shift of π. The $-\pi/2$ delay is reached thanks to the zero, and it is straightforward from (1) to evaluate that this shift is achieved at a frequency which is the geometric mean between the pole and the zero. The ring oscillation frequency is thus $\omega_0 = (\omega_p\,\omega_z)^{1/2}$. Then, using (1) and the Barkhausen criterion for loop magnitude, we obtain the condition for the dc gain: $T_0(\omega_p/\omega_z)^{1/2} = 1$. At the start-up the gain must be larger than one. Then, when the amplitude rises, the "effective" transconductance of the cross-coupled pair M_3-M_4 reduces with respect to the initial small signal value $g_{mc}/2$, until the oscillation becomes stable. Note, from the expression of the dominant pole frequency, that also ω_P and, accordingly, ω_0 vary. Both ω_P and ω_0 increase when the transconductance of the pair M_3-M_4 lowers. In an oscillator this effect would lead to very poor performance in term of frequency stability and phase noise. In our application we do not face this problem, since the circuit is driven by an input signal.

IV. Lock Range and Phase Accuracy

The tail transistors of the two stages, M_5 in Fig. 1 and the analogous transistor of the other stage, are driven by the two differential outputs of the VCO, running at $2\omega_{in}$. In this way the injected current i_{in}, at $2\omega_{in}$ is superimposed to the dc tail bias current I_{DC}. That forces the ring to oscillate at ω_{in}, which is in general different from ω_0. The mechanism of injection locking has been rigorously discussed by many authors, see for instance [3], [6], and is intuitively recalled with the help of Fig. 2. A steady condition is reached when the ring oscillates at ω_{in}, in this case the input couple, M_1-M_2 in Fig. 1, behaves as a mixer for the signal coming from the tail, and converts at its output I_{DC} and i_{in}, both shifted at ω_{in}. The dominant pole filters the higher frequency products of the mixers. Since ω_{in} is different from ω_0, the lag of each stage exceeds $-\pi/2$, by an amount that we call $-\varphi$. Thus the mixer must balance this additional angle by properly adding the opposite shift to its output. That is sketched in Fig. 2, where all the phasors rotate at ω_{in}. V_1 represents the voltage output signal due to the dc current, while v_2 is the additional signal caused by the injected

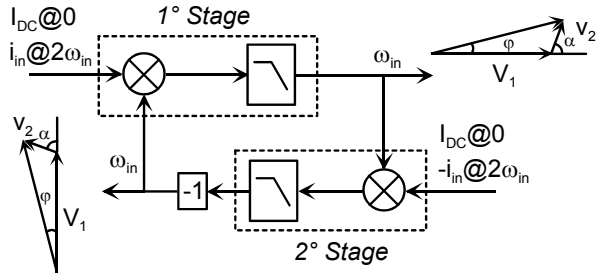

Fig. 2. The injection locking mechanism in the two stages ring oscillator.

current. The loop adjusts the phasors, by settling the angle α, in order to give an additional shift φ, with respect to the state in which no current is injected. It is easy to see that when a differential signal, i_{in} and $-i_{in}$ is forced in the two stages, their outputs are still in quadrature.

It is possible to evaluate the maximum value of frequency deviation, $\Delta\omega$, from ω_0 at which the divider can operate, [6]. If SL is the magnitude of the slope, evaluated at ω_0, of the phase vs. frequency characteristic of $T(j\omega)$, it results $SL = \varphi/\Delta\omega$. If we define the injection strength $m = v_2/V_1 = i_{in}/I_{DC}$, Fig.2 suggests that, with a good approximation, is $\varphi_{max} \cong m$, which in turn gives $\Delta\omega_{max} \cong m/SL$. The lock range increases with m, and is inversely proportional to SL. The magnitude of the slope can be simply evaluated from (1). Recalling that the expression for the free running frequency, ω_0, is $\omega_0 = (\omega_P\,\omega_Z)^{1/2}$, it results:

$$SL = \left|\left(\frac{d\varphi}{d\omega}\right)_{\omega_0}\right| = \frac{2}{\omega_p + \omega_z} \qquad (2)$$

For a given ω_0, this value is much smaller than the corresponding one in an LC tank oscillator, namely $2Q/\omega_0$. In fact, first, the arithmetic mean $(\omega_p + \omega_z)/2$ is always larger than the geometric mean, ω_0. Second, the factor 2Q is usually greater than one. The lock range is accordingly larger in an injection ring oscillator.

Note that quadrature accuracy also benefits from a low value of SL. The quadrature error is due to the mismatch between the values of ω_0 in the two stages. For a difference $d\omega_0$, a corresponding variation $d\varphi$ must thus occur. That can be achieved only by changing the angle α between the vectors V_1 and v_2. This shift $d\alpha$, is the quadrature error. From the phasors in Fig.2 we obtain that:

$$\varphi = \tan^{-1}\frac{m\cdot\sin\alpha}{1+m\cdot\cos\alpha} \Rightarrow d\alpha = d\varphi\,\frac{1+m^2+2m\cos\alpha}{m\left(m+\cos\alpha\right)} \qquad (3)$$

Since the magnitude of $d\varphi$ is approximately $|d\varphi| = SL\,|d\omega_0|$, also in this case a smoother slope SL is beneficial.

V. Experimental Results

A cascade of two dividers has been integrated in a STM 0.13μm CMOS technology. The two circuits have the same topology, the only difference is that in the second divider the bias current is almost halved with respect to the first one, following the reduction of the operating frequency. Post-

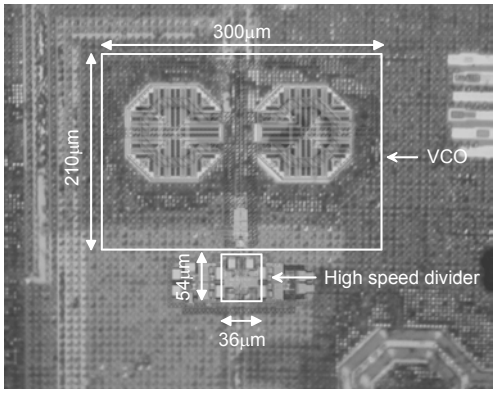

Fig. 3. Die photo.

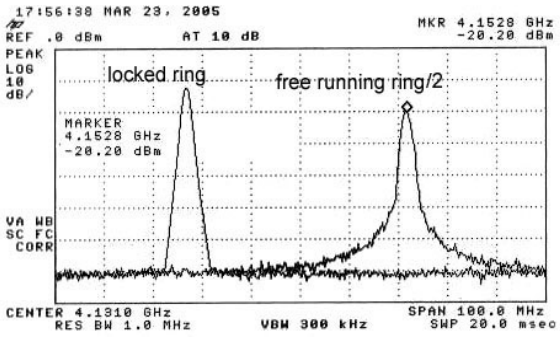

Fig. 4. Output spectrum (left) of the cascade of the two dividers driven by the VCO running at 14.64 GHz (the spectrum is shifted for sake of comparison), compared with the spectrum (right) of the first ring in free running, divided by two.

layout simulations show that the first circuit can operate with an input frequency varying between 7 and 19 GHz.

When no input signal is present, the first and the second dividers oscillate in free running at 8.8 and 5.5 GHz, respectively.

Fig. 3 shows a photo of the chip. Most of the area is filled by the inductors of a differential LC-tank VCO, integrated on the same die, to provide the differential driving signal. Only the signals from the VCO and from the second divider are available at the output. Moreover, for testing purpose, it is possible to switch-off the power supply of the VCO, in order to let the first circuit oscillate in free running mode. For comparison, two measured output spectra are superimposed in Fig. 4. The spectrum on the left side was measured when the divider chain is driven by the VCO. Its center frequency, shifted in the figure for comparison, is 3.66 GHz, corresponding to a VCO frequency four times higher, that is 14.64 GHz. The spectrum on the right side is the one of the first ring operating in free running, divided by two by the second ring. The measured free running frequency is 8.3 GHz, very close to the value obtained by simulations. The VCO output frequency spans between 11 and 15 GHz, thus it was possible to test the divider chain only in this interval. The measured locking range is in any case close to 31 %. Fig. 5 shows first the output phase noise when the VCO is switched off. It is the phase noise of the first ring, reduced of – 6 dB by the frequency division. As anticipated, this noise is very high, but it does not impair the overall noise performance. When the two dividers are injection-locked to the VCO it is the phase

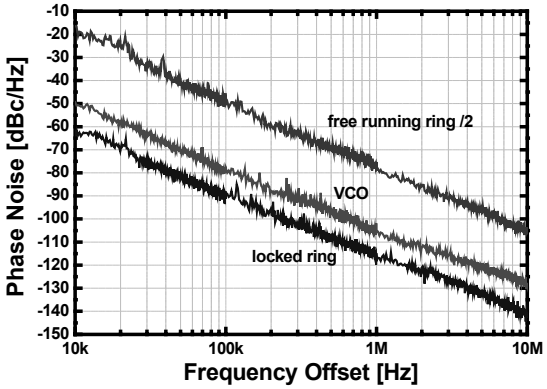

Fig. 5. Comparison between the phase noise of the VCO and the phase noise at the output of the two dividers. The difference is 12 dB, indicating that the dividers do not impair the noise performance.

TABLE I
MEASURED DIVIDERS PERFORMANCE

Power supply	1.2 V
Bias current – first divider	3 mA
Bias current – second divider	1.5 mA
Free running frequency – first divider.	8.3 GHz
Free running frequency – second divider	5.5 GHz
Input frequency range	11 – 15 GHz

noise of this circuit that appears at the output. In Fig.5 in fact, we also compare the measured phase noise of the VCO with the output of the two locked dividers. The 12-dB difference is in accordance with the frequency division by four, and confirms that the output phase noise is not affected by the ring phase noise, as expected. Table I summarizes the performance of the two dividers.

VI. CONCLUSIONS

The discussed frequency divider features one of the largest input frequency range presented in literature. The input signal spans between 11-15 GHz, about 31% of the center frequency. This measure is limited by the tuning range of the VCO, used as signal source, post layout simulations show even a larger locking range, 7-19 GHz. The key feature of the circuit is the reduced slope of the phase-frequency characteristic, that in this case is beneficial in term of tuning range and quadrature accuracy.

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