Fundamental Power Limits of SAR and $\Delta\Sigma$ Analog-to-Digital Converters

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***Abstract*—This work aims at estimating and comparing the power limits of $\Delta\Sigma$ and charge-redistribution successive-approximation register (CR-SAR) analog-to-digital converters (ADCs), in order to identify which topology is the most power-efficient for a target resolution. A power consumption model for mismatch-limited SAR ADCs and for discrete-time (DT) $\Delta\Sigma$ modulators is presented and validated against experimental data. SAR ADCs are found to be the best choice for low-to-medium resolutions, up to roughly 80 dB of dynamic range (DR). At high resolutions, on the other hand, $\Delta\Sigma$ modulators become more power-efficient. This is due to the intrinsic robustness of the $\Delta\Sigma$ modulation principle against circuit imperfections and non-idealities. Furthermore, a comparison of the area occupation of such topologies reveals that, at high resolutions and for a given dynamic range, $\Delta\Sigma$ ADCs result more area-efficient as well.**

I. Introduction

With about 100 implementations, SAR and $\Delta\Sigma$ analog-to-digital converters account for 60% of the ADCs presented at the International Solid-State Circuits Conference (ISSCC) in the last decade. The reasons for such popularity can be found in the intrinsic power efficiency and amenability to scaling of SAR ADCs on one side, and in the robustness against circuit imperfections of $\Delta\Sigma$ converters on the other. Figure 1 shows the resolution versus bandwidth plot of state-of-the-art SAR and $\Delta\Sigma$ converters published at ISSCC in the years 2006–2015 [1]. Two distinct regions can be clearly identified. Pushed by technology scaling, SAR ADCs dominate those applications (e.g. high-speed IO links) requiring above 100-MHz bandwidth with low-to-medium resolutions (below 60 dB). On the other hand, $\Delta\Sigma$ ADCs are the optimal choice for lower speed applications (below 1 MHz) with more than 12-bit effective resolution (e.g. audio and high-resolution biomedical systems). In between, lays a region equally populated by these two converter architectures, which corresponds to the requirements of several applications such as wireless and wireline communications and medical imaging. Although previous works have studied the fundamental power limits of SAR converters and discrete-time $\Delta\Sigma$ ADCs [2], [3], a thorough analysis of the real limits of both topologies, and a specific comparison between these two popular architectures are missing. This work presents an in-depth investigation of the power consumption of SAR and $\Delta\Sigma$ converters in order to justify the trend observed in Fig. 1. Theoretical power models are presented, then validated against experimental data from [1] and compared. SAR ADCs are found more power-efficient at low resolutions, where the consumption is dominated by the power required to drive the capacitor array. On the other hand, DT $\Delta\Sigma$ modulators are more efficient at high resolutions, where their consumption is mainly determined by the power spent in the operational-transconductance-amplifier (OTA) stages.

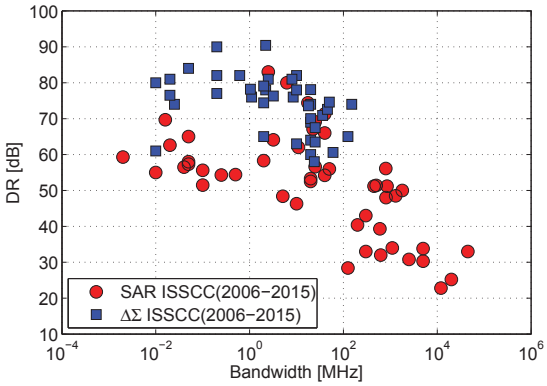

Fig. 1. Resolution vs. bandwidth of SAR and $\Delta\Sigma$ ADCs from [1].

This paper is organized as follows. Section II and Section III present the SAR and the $\Delta\Sigma$ ADC power consumption models, respectively. Section IV validates the proposed models against experimental data and compares the two architectures in terms of power efficiency. In Section V the two converters are compared in terms of area and, finally, conclusions are drawn in Section VI.

II. SAR ADC Power Consumption Model

Figure 2 schematically depicts the model of a generic SAR ADC, where the capacitive array works as sample-and-hold during the sampling phase and as digital-to-analog converter (DAC) during the conversion phase. The minimum power required to perform the analog-to-digital conversion in a Nyquist-rate SAR converter is the one spent to sample the input signal on the capacitance C of the feedback DAC. Considering C discharged at the beginning of the sampling phase, this contribution is

$$P_{s,SAR} \cong CV_{FS}V_{DD}f_S = CV_{DD}^2 f_S, \tag{1}$$

where f_S is the sampling frequency, and V_{FS} the converter full-scale range, assumed equal to the power-supply voltage V_{DD} for simplicity. The DAC capacitance has to be sized to fulfill two different requirements, since both noise and non-linearity due to capacitive mismatch can limit the converter resolution. In the former case, imposing that the input-referred thermal noise contribution, kT/C, does not limit the achievable dynamic range, the minimum value of the array capacitance turns out to be

$$C_{min,noise} \cong 8kT \cdot DR/V_{DD}^2. \tag{2}$$

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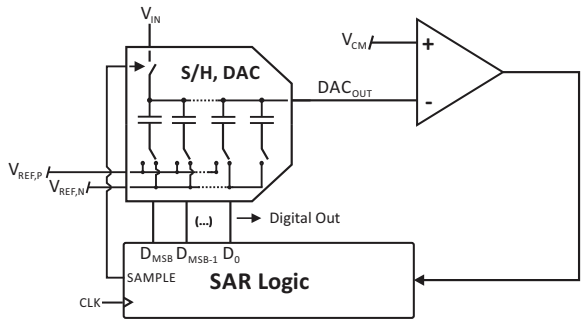

Fig. 2. Schematic diagram of a charge-redistribution SAR ADC.

Substituting (2) into (1), the sampling power consumption due to the thermal the noise limit is

$$P_{s,noise} = 8kTf_S \cdot DR. \tag{3}$$

However, in a SAR ADC, the mismatch between the unit capacitors of the capacitive DAC can limit the converter accuracy yielding differential- and integral-non-linearity (DNL and INL). The resulting effect is distortion that can impair the signal-to-noise-and-distortion-ratio (SNDR), thus the resolution. Employing digital calibration techniques it is possible to reduce the impact of mismatch-dependent non-linearity, however, at the price of increased area, power, and design complexity. For this reason, the effect of calibration is not taken into consideration in the present analysis. To mitigate the effect of capacitive mismatch, which can be considered a statistical source of error, the size of the array capacitance has to be chosen large enough to avoid a non-monotonic characteristic, and to have a DNL standard deviation, σ_{DNL}, well below the LSB. A typical design criteria [4], [5] is to set the worst-case σ_{DNL}, which occurs at the mid-code, so that $3\sigma_{DNL,max}<0.5$, and thus to size the DAC unit element, C_u, to be greater than a minimum value dependent on technological parameters of the capacitors and on the chosen DAC topology [6]. Considering that the standard deviation of the unit capacitor can be expressed in terms of the Pelgrom mismatch coefficient, k_c, and the specific capacitance, c_{spec},

$$\sigma\left(\frac{\Delta C}{C_u}\right) = k_c \cdot \sqrt{\frac{c_{spec}}{2C_u}}, \tag{4}$$

and that the for a conventional binary weighted (CBW) single-ended array topology $\sigma_{DNL,max} = 2^{N/2} \cdot \sigma\left(\frac{\Delta C}{C_u}\right)$ [5], the minimum value of the unit capacitance results

$$C_{u,min} = 18 \cdot 2^N (k_c^2 c_{spec}). \tag{5}$$

Since in a N-bit CBW array $C \cong 2^N C_u$, the sampling power resulting from (1), once the mismatch limit sizing is considered, is

$$P_{s,mis.} \cong 18 \cdot 2^{2N} (k_c^2 c_{spec}) V_{DD}^2 f_S. \tag{6}$$

The two power limits given by (3) and (6), normalized to the signal bandwidth $BW{=}f_S/2$, are plotted in Fig. 3 as a function of the dynamic range, and considering in (6) that the dynamic range is function of the number of effective bits, being $DR_{dB} \cong 6.02N - 1.76$ [3]. As reference technology, a 65-nm CMOS process has been considered, with k_c=0.5%, c_{spec}=1 $fF/\mu m^2$ and V_{DD}=1 V. It is evident that capacitive mismatch, rather than thermal noise, imposes the size of the sampling capacitance, thus setting a minimum limit to the power consumption of SAR converters. This result is different from the one obtained in [3] where only the noise limit was considered in the DAC sizing.

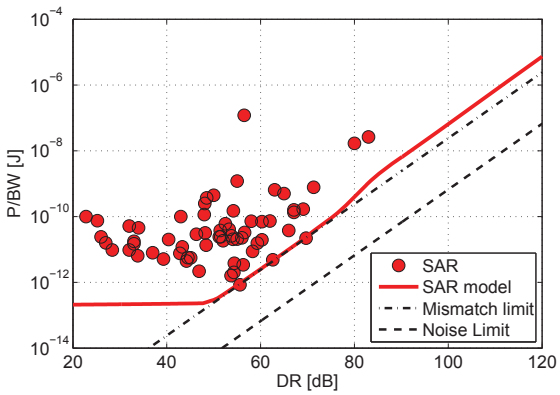

Fig. 3. Estimated normalized power vs. resolution of SAR ADCs together with real data (circles) from [1].

However, the sampling power is not the only contribution to the power consumption in SAR ADCs. Further contributions are given by the SAR logic circuit, the DAC switching procedure performing the binary searching algorithm, and the comparator. While the contribution due to the logic circuit is in general negligible [5], [6], especially if advanced technologies are used, the power needed to switch the capacitive array during the conversion cycle depends on the adopted switching algorithm [6]. In general, this power is a fraction of the overall sampling contribution and depends on the binary search algorithm. While the conventional scheme [6] entails a comparable contribution, smart switching procedures allow to greatly reduce its impact. For example, adopting the set-and-down scheme or the merged capacitor switching algorithm [7], the switching power consumption is about 25% and 4% of the sampling power, respectively.

As far as the comparator is concerned, efficient implementations of SAR ADCs usually adopt a dynamic comparator whose power consumption is determined by the charge and discharge of its load capacitor. Its value is set by the resolution constraints, but it is usually of few femtofarads [8]. In addition, such circuits are intrinsically digital, being turned only when the input signals have to be compared and then swiftly disabled, and thus their contribution can be neglected [4], [5]. However, it is worth pointing out that for high resolutions (DR>80 dB), as the LSB becomes smaller, both offset and kickback noise (i.e. the capacitive feedthrough from the comparator) become major design issues, imposing the use of a static comparator rather than an efficient dynamic topology [9]. A typical implementation is the well known continuous time preamplifier followed by a latch. Being an analog circuit, its static power consumption is no longer negligible since the bias current must be sized to keep its noise below the LSB. Considering only the dominant noise contribution of the CMOS input pair, and assuming the transistors biased in sub-threshold region, the requirement results

$$3 \cdot V_{rms,noise} \cong 3 \cdot \sqrt{\frac{8kTn^2U_T}{I_B}\frac{\pi}{2}BW_{preamp}} < \frac{V_{DD}}{2^N}, \tag{7}$$

where $n \cong 1.5$ is the subthreshold slope, U_T the thermal voltage, I_B the bias current, and BW_{preamp} the preamplifier bandwidth. The latter should be large enough to guarantee the comparator settling during each bit evaluation period. As a rule-of-thumb, this bandwidth can be set equal to $10Nf_S$. From (7), the static comparator power consumption can be

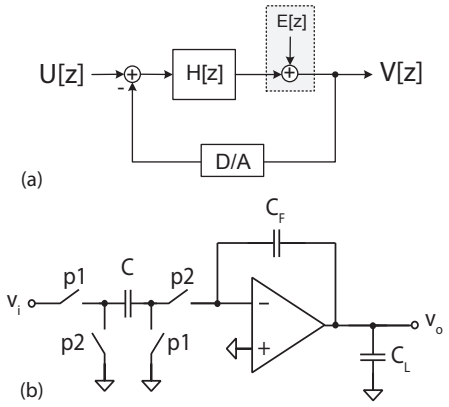

Fig. 4. (a) Block diagram of a single-loop $\Delta\Sigma$ modulator. (b) DT integrator.

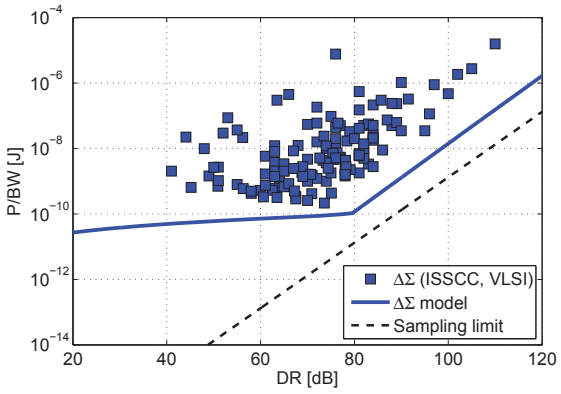

Fig. 5. Estimated normalized power vs. resolution of $\Delta\Sigma$ modulators together with to real data (squares) from [1].

evaluated as

$$P_{comp,static} \cong 0.5 \cdot V_{DD} I_B \cong \frac{60\pi N 2^{2N} f_S kTn^2 U_T}{V_{DD}}, \quad (8)$$

where the factor 0.5 accounts for the possibility to enable the comparator only during the conversion phase, thus for approximately half of the sampling period.

In conclusion, the power consumption limit for SAR converters is mainly determined by the sampling contribution given by (6) and, for high resolution (DR>80 dB), also by the static power consumption of the preamplifier-based comparator given by (8). The power consumption estimated from the proposed model and normalized to the signal bandwidth is plotted in Fig. 3, together with the experimental data from [1]. The estimated power limit (solid line) encloses all the measured data, the agreement being very good especially for medium resolution (50-70 dB). At very low resolutions, the sampling limit (dash-dotted line) underestimates the experimental data mainly because the real DAC capacitance is chosen to be larger than the value imposed by noise and mismatch because of technology limit [2] or to avoid the impact of parasitics. The plateau visible in the solid line of Fig. 3 has been obtained considering a minimum DAC capacitance of 100 fF. Finally, note that the use of a static comparator increases the power limit due to the sampling contribution at high resolution.

III. $\Delta\Sigma$ Modulator Power Consumption Model

The minimum power required to charge the sampling capacitor C in a $\Delta\Sigma$ modulator can be obtained from (1) with the additional effect of the oversampling ratio, OSR=$f_S/(2BW)$, yielding

$$P_{s,\Delta\Sigma} \cong CV_{DD}^2 f_S = 8kTf_S \cdot DR/OSR. \quad (9)$$

$P_{s,\Delta\Sigma}$ is proportional to the desired ADC resolution, as in a Nyquist-rate converter, and is inversely proportional to OSR. For simplicity, it has been assumed here a single-ended implementation, with a full-scale range equal to the power supply V_{DD}. To this minimum power, a second contribution dependent on the particular $\Delta\Sigma$ realization has to be added. For our analysis, we considered a single-loop third-order $\Delta\Sigma$ modulator (Fig. 4(a)), which represents a reasonable trade-off between performance and design complexity, in its discrete-time implementation. DT modulators are better suited for such an investigation because it is relatively simple to relate the power consumption to the desired resolution. The power of a single-loop DT $\Delta\Sigma$ modulator is dominated by the integrators, and in particular by the OTA of the first stage (Fig. 4(b)). The integrators following the first one are normally biased at a lower current, a popular design choice being to bias the second and third OTA at half the current of the first stage as their imperfections are mitigated by the gain of the preceding stages. The quantizer power can be neglected to a first order approximation, especially in single-bit implementations.

In any switched-capacitor (SC) system, the OTA output must settle in less than half a clock cycle to the final value within a certain accuracy. The required integrator unity-gain-bandwidth (UGBW) can be related to the transconductance g_m of the OTA input pair and to the equivalent capacitance C_{EQ} effectively loading the amplifier. The latter depends on how the SC integrator is implemented, and is assumed here for simplicity to be a multiple of the sampling capacitor, i.e. $C_{EQ} = \beta C$. From [10], it results

$$UGBW(rad/s) \cong 1.4(N+1)f_S = g_m/C_{EQ}, \quad (10)$$

where N represents the target ADC accuracy (i.e. DR in bit). The input pair is normally biased in the middle of weak inversion, with a constant transconductor efficiency $g_m/I_D \approx 15\,V^{-1}$, so to obtain a linear control of the transconductance via the bias current and to maximize the OTA efficiency. Assuming for simplicity a single-stage OTA topology (i.e. telescopic-cascode), the power in the first OTA results

$$P_{OTA} \cong 2V_{DD}\frac{g_m}{(g_m/I_D)} \cong \frac{2V_{DD}}{(g_m/I_D)} C_{EQ} \cdot 1.4(N+1)f_S. \quad (11)$$

Once the sampling capacitor is sized to achieve the desired DR from (9), i.e. $C = 8kT \cdot DR/\left(OSR \cdot V_{DD}^2\right)$, the OTA power consumption given by (11) overwhelms the sampling contribution and the modulator power consumption results

$$\frac{P_{\Delta\Sigma}}{BW} \cong \frac{4}{(g_m/I_D)}\frac{\beta}{V_{DD}} 1.4(N+1)8kT \cdot DR. \quad (12)$$

In (12), the modulator power has been again normalized to the signal bandwidth, i.e. BW=$f_S/(2 \cdot OSR)$, to fairly compare $\Delta\Sigma$ and SAR ADCs, eliminating the dependence from the OSR. The $\Delta\Sigma$ normalized power is shown in Fig. 5 as function of the resolution. For this plot we assumed a fully differential implementation, with V_{DD}=1 V, C=C_F=C_L, and $\beta = 3$. At high resolutions the modulator power is governed by (12). At low DR, the sampling capacitor cannot be made indefinitely small as (9) would permit, therefore a minimum value of the sampling capacitor of 300 fF has been assumed due to mismatch and practical considerations. In order to validate the model, in Fig. 5 theoretical predicted values are compared to the actual power/resolution of $\Delta\Sigma$ modulators from [1]. A

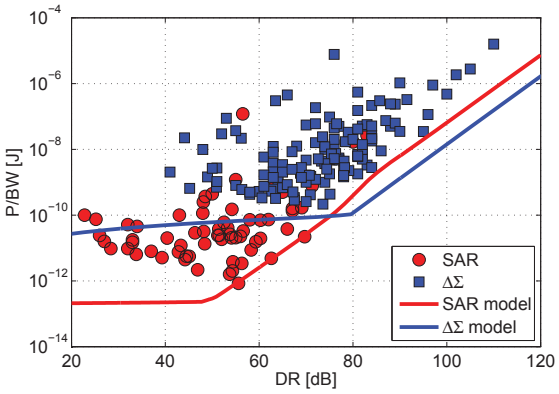

Fig. 6. Estimated normalized power vs. resolution of SAR and $\Delta\Sigma$ ADCs together with real data (circles and squares, respectively) from [1].

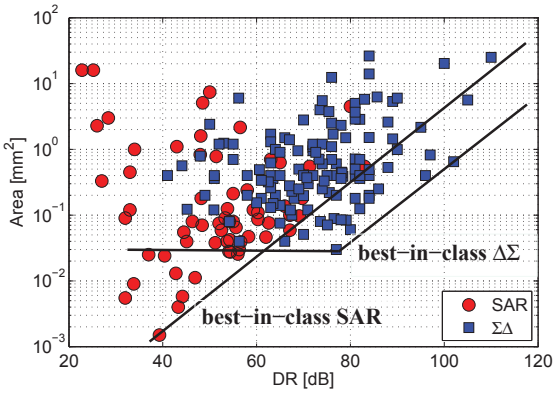

Fig. 7. Area vs. resolution of $\Delta\Sigma$ and SAR ADCs from [1].

very good matching between predicted and measured data is observed despite the simplicity of the proposed model.

IV. Power Efficiency Comparison

Figure 6 shows the comparison between the estimated power normalized to signal bandwidth and experimental data for both architectures, proving a good fitting of the power models despite the rough assumptions made. As experimental data highlight, at low resolutions SAR ADCs appear to be more efficient than $\Delta\Sigma$ converters, while at high resolutions the trend is inverted, with SAR ADCs losing efficiency mainly due to mismatch limitations. This implies that the impact of mismatch becomes more severe degrading the linearity when high DR is required, and motivates the use of an array capacitance larger than the limit imposed by noise requirements. It can be noticed that by adopting proper calibration techniques and with the improved matching performance of more advanced technology processes, this difference may be lowered. However, it must be pointed out that as the resolution increases, also the comparator design becomes less efficient, requiring a static rather than dynamic implementation, and that in general calibration techniques not only require power but also area, which is an important issue in integrated circuit design. The better power efficiency shown by $\Delta\Sigma$ converters at high resolutions can be explained with the intrinsic robustness of this architecture against circuit imperfections such as the comparator noise and offset that are attenuated like the quantization noise.

V. Area Comparison

In the previous sections it has been shown that, due to technological limits of SAR ADCs, there is an advantage in terms of efficiency adopting a $\Delta\Sigma$ architecture when a high resolution has to be achieved. Also area occupation is a clear advantage of $\Delta\Sigma$ modulators with respect to SAR converters. In fact, as shown in Fig. 7, $\Delta\Sigma$ ADCs outperform SAR converters in terms of area for moderate-to-high resolutions, i.e. for a dynamic range greater than roughly 70 dB, as the best-in-class area/resolution curves suggest. This can be explained considering that $\Delta\Sigma$ modulation offers a straightforward way (i.e. dynamic weighted averaging) to attenuate the impact of the sampling capacitor mismatch, without relying on the intrinsic matching of the capacitive array or resorting to on-chip digital calibration techniques, as in SAR ADCs. Area is often a key parameter in many of the applications in which such ADCs are required (multichannel sensors ASICs, audio applications, etc.). This difference is in general not affected by the scaling and, on the contrary, is enlarged if calibrated SAR ADCs are considered, due to the typical complex digital circuits and sometimes memory that are required to mitigate the inaccuracy of the analog blocks.

VI. Conclusions

This paper has presented a power consumption model for mismatch-limited SAR ADCs and for DT $\Delta\Sigma$ modulators. Comparison between these two architectures confirms the power efficiency of SAR ADCs at low-to-medium resolutions, making them the ideal candidates for a range of applications ranging from low-resolution biomedical to wireless communications. On the other hand, for resolution above roughly 80 dB, DT $\Delta\Sigma$ modulators become more power-efficient, as a result of their greater robustness against circuit imperfections. Moreover, compared to SAR ADCs, $\Delta\Sigma$ modulators exhibit an area benefit at high resolutions, that makes them the natural choice for high-precision applications.

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