High Count-Rate 8 × 8 SPAD Arrays for Quantum Key Distribution

C. Garofalo, M. Raimondi, K. Herrera Pesantes, H. Haka, A. Tosi, F. Villa

Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan, Italy

caterina.garofalo@polimi.it

The increasing computational power of quantum computers represents a threat to the security of stored and transmitted data [1]. Unconditional security is provided by quantum and post-quantum communication methods, such as Quantum Key Distribution (QKD). In this framework, the European Space Agency (ESA) is actively pursuing the integration of ground and satellite-based systems to implement quantum-secure communication infrastructures. However, the main challenge is maximising the key rate, limited by the performance of single-photon detectors implemented in the receivers.

Following the detector described in [2], we developed new 8 × 8 SPAD arrays in a 3D-stacked 40 nm CMOS technology by STMicroelectronics, achieving a deadtime below 500 ps, thus guaranteeing a count rate higher than 2 Gcps (Giga counts per second). Such detectors are designed to meet satellite-to-ground communication fundamental requirements, including high Photon Detection Efficiency (PDE), low Dark Count Rate (DCR), and an afterpulsing probability below 0.1%.

Figure 1 shows the fabricated chip, which hosts two 8 × 8 SPAD arrays, namely Trial A and Trial B. Pixel pitch is 10.17 µm, and a microlens array increases the photon collection efficiency. Moreover, the arrangement of the SPADs in two arrays ensures that 64 pixels behave as a unique detector with enhanced photon count rate. The SPADs' outputs of each array are connected to OR-trees and then routed to the output pads. The chip features 4 pairs of Low-Voltage Differential Signaling (LVDS) output pads, shared between the two trials. Photon detections are encoded either in a rising or a falling edge of the output signal, meaning that the 2 GHz count rate can be achieved with four outputs operating at 250 MHz each. Trial A combines its 64 SPAD outputs in a 3-stage OR-tree, which is routed to a frequency divider, distributing the pulses to the 4 output pads. Trial B is constituted of 4 independent quadrants, each connected to a 2-stage OR-tree feeding a toggle flip-flop connected to one of the outputs. The pulse pile-up is reduced by the presence of a pulse shrinker that reduces the duration of the signal propagating in the OR-tree to 250 ps.

The chip has been characterised, and the presented results are obtained at 23 V bias voltage, corresponding to 5.2 V excess bias. The measured PDE (Figure 2) at the target wavelength of 800 nm is 39.6%, reaching a maximum of 49.8% at 600 nm. The median DCR is 300 counts per second (cps) per pixel, corresponding to 2.9 cps/µm^2. The SPADs showing a DCR exceeding 10 times the trial's median value have been defined as hot pixels. Disabling such pixels, corresponding to less than 2% of the detectors, the overall DCR is approximately 20 kcps. The estimated deadtimes (Figure 3) highlight that Trial A achieves a notable count rate of 1.82 Gcps. Trial B achieves 2.38 Gcps per independent quadrant. The afterpulsing probability has been estimated from the DCR measured at different SPADs' deadtimes. This probability is below 1% at 7.5 ns pixel deadtime and is further reduced to below 0.1% for deadtimes longer than 9.5 ns. The single SPAD exhibits a timing jitter of 230 ps Full-Width at Half-Maximum (FWHM), which can be reduced to 62 ps (FWHM) by increasing its excess bias to 7.2 V.

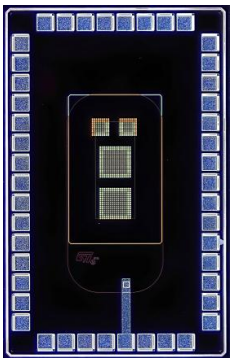

Figure 1 Chip in 3D40 technology implementing two 8 × 8 SPAD arrays

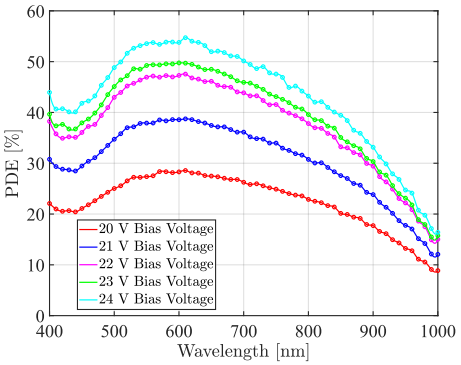

Figure 2 PDE at different wavelengths from 400 nm to 1000 nm, measured at different bias voltages

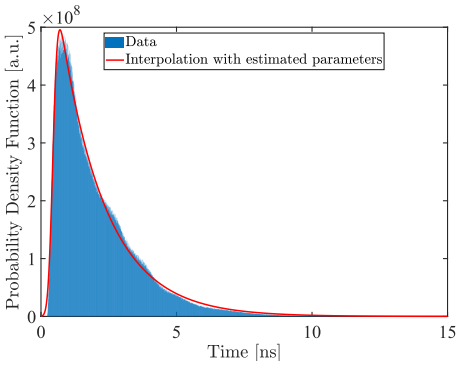

Figure 3 Example of deadtime estimation from the distribution of the times intercurred between two consecutive photon detections

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References:

[1] B. Yan et al., "Factoring integers with sublinear resources on a superconducting quantum processor", 2022, arXiv. doi: 10.48550/ARXIV.2212.12372.

[2] M. Raimondi et al., "2 GHz single photon avalanche diode detector for quantum key distribution applications", Photonics for Quantum 2025. SPIE, p. 46, July 18, 2025. doi: 10.1117/12.3063215.