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A 72fs-Total-Integrated-Jitter Two-Core Fractional-N Digital PLL with Digital Period Averaging Calibration on Frequency Quadrupler and True-in-Phase Combiner

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***Abstract*—This work presents a low-jitter and low out-of-band noise two-core fractional-N digital bang-bang phase-locked loop. Two novel techniques are introduced to efficiently suppress the quantization noise (QN) of the digitally-controlled oscillator (DCO) and to achieve an optimal trade between power consumption and PLL noise. The digital period averaging technique, working in background of the main system, enables the use of a low-power XOR based quadrupler for clocking $\Delta\Sigma$ modulator dithering the DCO tuning word. The true-in-phase combiner circuit implements a digitally-assisted power-combination of two PLL outputs, to optimally reduce the impact of the PLL noise sources. The prototype, implemented in a standard 28-nm CMOS process, has a core area of 0.47 mm^2 and synthesizes frequencies from 8.5 to 10.5 GHz, while dissipating 36 mW. The measured rms jitter (integrated from 1 kHz to 100 MHz and including spurs) is 72 fs for near-integer channels, with a worst case fractional spur of -59.7 dBc, while the measured out-of-band noise is -140.7 dBc/Hz at 10 MHz offset.**

***Index Terms*—5G, bang-bang phase-locked loop, low-jitter, low-spot noise, quantization noise.**

I. Introduction

LOW noise local-oscillator (LO) circuits are becoming crucial elements for various types of wireless systems, such as 5G transceivers and FMCW radars. In the first case the data-rate is improved by increasing the order of the constellation diagram, at the expense of tighter requirements on the error vector magnitude, which is ultimately limited by the LO integrated jitter. For example, the 5G new radio in the upper millimeter-wave frequency band demands for an integrated jitter less than 90 fs [1], which is a challenging task to fulfill in scaled CMOS technologies. On the other hand, performance of FMCW radars is mainly dependent on the LO out-of-band phase-noise (PN), which could hinder the detection of two close targets with large target cross-section ratios [2], [3].

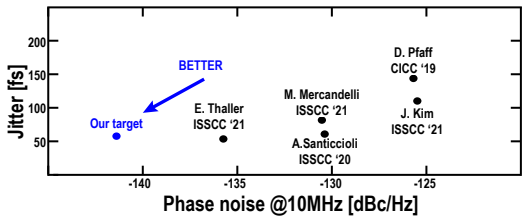

Fig. 1. Performance of recently published digital PLLs: jitter vs. PN at 10MHz offset normalized at 8.6GHz carrier.

The adoption of digital phase-locked-loops (PLLs) for these applications is becoming popular in recent literature [2], [4]–[17], as they can provide lower power consumption and lower silicon area occupation with respect to their analog counterparts [1], [18]–[23], while being able to naturally embed digital calibrations to compensate the impairments of deeply scaled CMOS technologies. While the integrated jitter of digital PLLs have been pushed below 90 fs by several works in literature, the spot-noise level, instead, is still limited to -136 dBc/Hz at 10 MHz offset [1](Fig. 1).

The out-of-band PN level of a PLL (either analog or digital) is generally limited by the oscillator design. For analog PLLs the only limitation stems from the random-walk phase-noise of the oscillator (Fig. 2). To circumvent this limitation, multi-core oscillators [4], [18] or multi-core PLLs [5] architectures were proposed to ideally achieve a 3dB PN reduction per each doubling of the number of cores at the expense of larger power consumption. However, in practice, the ideal PN reduction has never been fully achieved. This is particularly critical for re-configurable multi-core oscillators, where the need of dynamically scaling power consumption based on the required phase-noise performance, demands for the use of dedicated coupling networks introducing additional losses [18], [24], [25]. For digital PLLs instead, in addition to DCO thermal noise, the limited frequency granularity of the digitally con-

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[1]To the best of the authors' knowledge.

trolled oscillator (DCO) induces a quantization noise (QN) at the DCO digital-to-analog domain crossing, which worsens the out-of-band PN. In principle, the QN impact can be mitigated by increasing the DCO frequency resolution, but this comes at the cost of a larger number of bits, entailing higher design complexity and larger area occupation [26]. Furthermore, other solutions as [27]–[29] suffer from large frequency resolution variability over PVT spreads and tuning range. Alternatively, a $\Delta\Sigma$ modulator dithering the DCO tuning word could be exploited to high-pass shape the QN power spectrum, which is then filtered off by the DCO frequency-to-phase integration. Unfortunately, despite the advantages of this approach, if the $\Delta\Sigma$ modulator is clocked with the already available low-frequency PLL *ref* signal the problem would not be completely solved, as a large bump in the out-of-band PN would still be present, due to the limited bandwidth on which the QN power is spread (Fig. 2). Using a higher reference frequency would be a solution, but high-frequency off-chip crystal oscillators are expensive and not suitable for mass production. To avoid this problem, prior works in literature generated an internal higher frequency $\Delta\Sigma$ oversampling clock either by a frequency multiplication of the *ref* signal based on an auxiliary PLL or by frequency division of DCO signal [4], [30]. In the first case pulling phenomena between the auxiliary and the main PLL worsen the performances. Instead, in the second case, the use of an auxiliary fixed-modulus divider [4] fed by the DCO signal to generate the $\Delta\Sigma$ clock induces a large power consumption overhead. To circumvent this limitation, it may be possible to use the high-frequency inter-stage signals inside the MMD within the PLL loop. However, these signals feature large period errors [31], which corrupt the $\Delta\Sigma$ quantization noise spectrum, as discussed in the following section. In [30], instead, a fixed modulus pre-scaler in front of the MMD is used to generate the $\Delta\Sigma$ clock, however, this solution has the drawback of increasing the quantization error in fractional-N mode, thus requiring a larger range for the digital-to-time converter (DTC) used to re-align the divider and reference signals in state-of-the art low-noise fractional-N PLLs [18], [32]. Additionally, the divider-based oversampling approach may generate metastability issues related to the crossing of two non-synchronous clock domains within the PLL loop filter, thus requiring dedicated techniques to address them [30], [33].

This work introduces a two-core digital bang-bang PLL (BBPLL) [9] able to achieve a spot-noise level below -140 dBc/Hz at 10 MHz offset and an rms jitter of 72fs leveraging: (i) a low-power XOR based quadrupler for the generation of the oversampled $\Delta\Sigma$ clock, enabled by the use of a background duty cycle correction technique denoted as digital period averaging (DPA) and (ii) a digitally-assisted power-combiner circuit, denoted as true-in-phase combiner (TIPC), which combines the outputs of the two PLL cores achieving the ideal PN reduction without impairing the amplitude of the output RF signal. This paper is organized as follow. Section II quantifies the contribution of QN in the adopted PLL architecture and introduces the proposed quadrupler-based oversampling technique, together with the DPA background calibration. Section III discusses the operation of the proposed TIPC circuit, while Section IV reports the experimental measurements on the prototype, comparing the results with the state of the art. Conclusions are drawn in Section V.

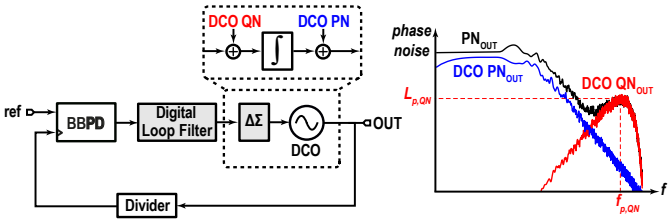

Fig. 2. Limitations to the out-of-band PN in digital PLLs. DCO PN_{OUT} and DCO QN_{OUT} are the contributions of the DCO PN and QN to the output PLL PN_{OUT}, respectively.

II. Frequency Quadrupler for QN Suppression

A. Impact of DCO quantization noise

In a generic digital PLL, the PN spectrum of the QN generated by an n^{th} order $\Delta\Sigma$ modulator placed at the DCO digital-to-analog domain crossing interface can be derived as [34]:

$$\mathcal{L}_{QN}(f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{f}\right)^2 \frac{2^{2n}}{f_{ck}} sin^{2n}\left(\pi\frac{f}{f_{ck}}\right) sinc^2\left(\frac{f}{f_{ck}}\right), \tag{1}$$

where Δf_{res} is the DCO frequency resolution and f_{ck} is the $\Delta\Sigma$ clock frequency. In the above formula the presence of the $sinc()$ function stems from the digital-to-analog domain crossing operation, while the $sin^{2n}()$ function highlights the n^{th} order noise shaping high-pass filtering of the $\Delta\Sigma$ modulator. In our design, a 2^{nd} order $\Delta\Sigma$ modulator is used while the DCO was designed to have a frequency resolution of about 200kHz [2] with a DCO frequency $f_{out} = 8.5$ GHz. If the $\Delta\Sigma$ modulator is clocked with the already available 125 MHz PLL *ref* signal, the DCO QN would highly worsen the PLL out-of-band PN. Based on equation (1), the phase-noise peak $L_{p,QN}$ of the QN bump, illustrated in Fig. 2, and the frequency of the peak $f_{p,QN}$ can be derived as [3]:

$$f_{p,QN} = 0.31\, f_{ck}, \quad L_{p,QN} = 4.7\,\frac{\Delta f_{res}^2}{f_{ck}^3}. \tag{2}$$

In our design $f_{p,QN}$ =38.5 MHz and $L_{p,QN}$ =-130 dBc/Hz. Additionally, the presence of the DCO QN also worsens the

[2]Notice that the use of a $\Delta\Sigma$ modulator in a digital PLL greatly relaxes the specifications on the required DCO frequency resolution [35]. According to (1), where $n = 0$ represents the case in which no $\Delta\Sigma$ modulator is used (i.e., the loop filter digital word is simply truncated), the QN induced by the implemented 200kHz resolution would cause a $1/f^2$ noise equal to -125.7dBc/Hz at 10MHz offset, about 15dB larger than the implemented DCO PN at the same frequency. To avoid DCO PN degradation, about a factor of 20 smaller DCO frequency resolution would be needed.

[3]Considering the employed 2^{nd} order $\Delta\Sigma$ modulator, (2) is derived by equating to zero the first derivative of (1).

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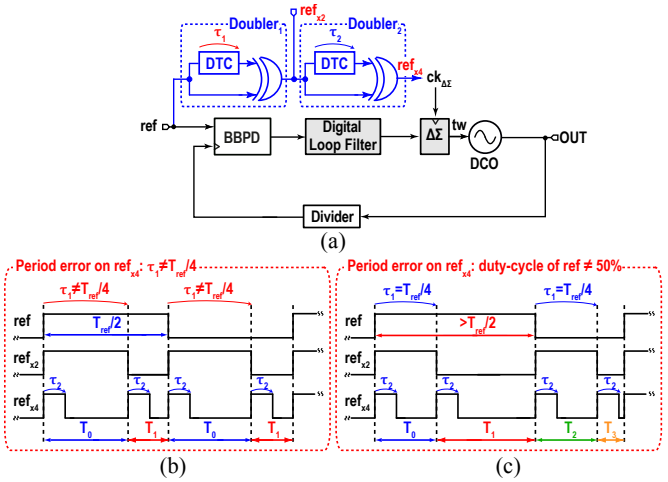

Fig. 3. Quadrupler based oversampling (a) and sources of the output period errors (b)-(c): (b) delay on the first doubler branch $\tau_1 \neq T_{ref}/4$; (c) input of the frequency quadrupler with a duty cycle different from 50%.

PLL integrated jitter performance. The QN jitter contribution can be derived as [4]:

$$\sigma^2_{\Delta t_{QN}} = \frac{\int_{-\infty}^{+\infty} \mathcal{L}_{QN}(f)\, df}{4\pi^2 f^2_{out}} = \frac{\Delta f^2_{res}}{f^2_{out} f^2_{ck}} \frac{1}{12}, \quad (4)$$

leading $\sigma_{\Delta t_{QN}} \approx 54fs$ in our design. For a sub-90 fs PLL, this contribution would shift the minimum requirement on the integrated jitter due to random noise sources (i.e. excluding the QN contribution) to about 70 fs, thus posing extra challenges in the design of the PLL building blocks.

Equations (2) and (4) highlight that the QN impact on spot-noise and jitter is inversely proportional to the cube and the square of the $\Delta\Sigma$ clock frequency f_{ck}, respectively. Therefore, adopting a clock frequency which is 4 times higher than the *ref* frequency, i.e. $f_{ck} = 4f_{ref}$, the jitter variance contribution is reduced by a factor of 16, while the QN peak lowers 18dB. For these reasons, a frequency quadrupler was selected for the generation of the oversampled $\Delta\Sigma$ clock, and its design is discussed in the next sections.

B. Quadrupler Based Oversampling

The proposed frequency quadrupler is implemented as a cascade of two XOR-based doublers generating the signal ref_{x4} starting from *ref*, as shown in Fig. 3. This approach provides several advantages over the prior solutions discussed in Section I. First, differently from architectures based on frequency division of the DCO output, this approach has an higher power efficiency, since it avoids the use of high-speed frequency dividers. At the same time synchronization between the ref_{x4} an *ref* clock domains is not an issue, since the

[4]For a generic n^{th}-order $\Delta\Sigma$ modulator, it is

$$\sigma^2_{\Delta t_{QN}} = \frac{\Delta f^2_{res}}{f^2_{out} f^2_{ck}} \frac{n+1}{36n} \binom{2n-2}{n-1}. \quad (3)$$

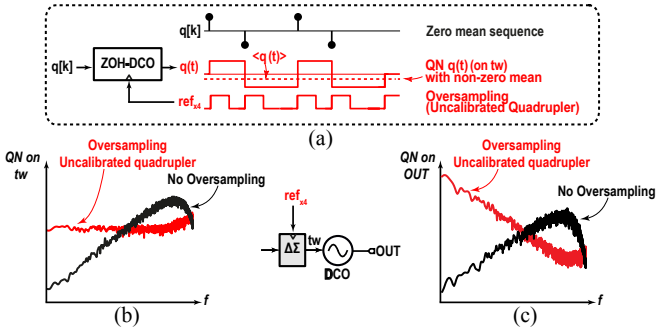

Fig. 4. (a) Model of the digital to analog interface between the $\Delta\Sigma$ modulator and the DCO. Impact of the period error impact on the clock driving the $\Delta\Sigma$ modulator: (b) noise on the input tuning word driving the DCO (c) resulting PN at the DCO output.

edges of the two waveforms are aligned [5]. With respect to frequency multiplication based on auxiliary PLLs, this solution is automatically insensitive to pulling, since it avoids the use of oscillators which could suffer from coupling with the main PLL DCO. It is important to notice that such a quadrupler architecture implements an exact multiplication by 4 of its input only if the delay implemented by the digital-to-time converter (DTC) in the first doubler, highlighted as τ_1 in Fig. 3(a), is precisely set to $T_{ref}/4$, which is however difficult to guarantee over PVT variations without a dedicated calibration technique [6]. This could be understood from Fig. 3(b), which highlights that if τ_1 departs from $T_{ref}/4$ than the duty cycle of the waveform ref_{x2} is not 50 %, causing the periods of the ref_{x4} waveform to be not uniform, i.e. the periods denoted as T_0 and T_1 in Fig. 3(b) are different [7]. Another source of non-ideality comes from the *ref* signal itself. Figure 3(c) shows that, even when $\tau_1 = T_{ref}/4$, if the *ref* signal duty cycle is different from 50%, the periods of ref_{x4} still suffer from non-uniformity, resulting in four different intervals T_0,T_1,T_2 and T_3. Figure 3 also shows that the delay τ_2 implemented by the DTC in the second XOR-based doubler only affects the duty cycle of ref_{x4}, i.e. it only affects the relative position of the falling edge within the ref_{x4} periods. Being the DCO $\Delta\Sigma$ modulator clocked with the rising edge of ref_{x4}, the value of the delay τ_2 is not critical, and therefore it could be implemented as a fixed delay, chosen to guarantee the minimum duty-cycle required by the digital section over PVT variations. In our system the delay τ_2 was instead obtained using a DTC with a fixed control word for debug purposes.

Unfortunately, any period error of the ref_{x4} waveform degrades the effectiveness of the oversampling technique in suppressing the DCO QN. Figure 4(a) depicts the model of the digital-to-analog interface at the DCO input, where the crossing between the two domains is represented by a zero-order-hold (ZOH) operation in the time domain. The $\Delta\Sigma$ modulator

[5]The only timing mismatch being represented by the non-zero delay of the XOR gates, which is negligible with respect to the waveform periods. It is worth to notice that synchronization problems generally arise when two clock domains with non-integer frequency ratios should be synchronized. The proposed solution implements a frequency multiplication, therefore it is naturally immune to such a problem.

[6]As an example, considering process corners, the delay of an inverter could vary by as much as 50% depending on the implementation and technology.

[7]In this picture the ref signal is supposed to have 50% duty cycle.

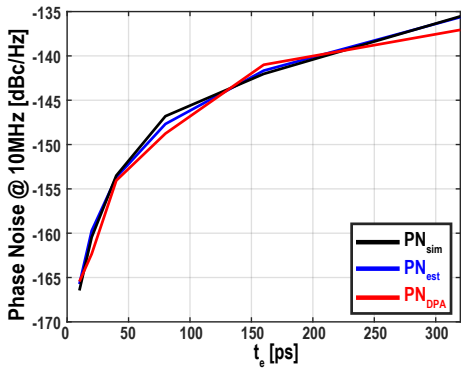

Fig. 5. Comparison between simulated PN values, PN_{sim}, and values PN_{est}, estimated with (5) at 10MHz offset as a function of a period error t_e. The red line PN_{DPA} is instead the simulated PN induced by the quadrupler with DPA calibration using DTCs with LSB $t_{LSB} = t_e$.

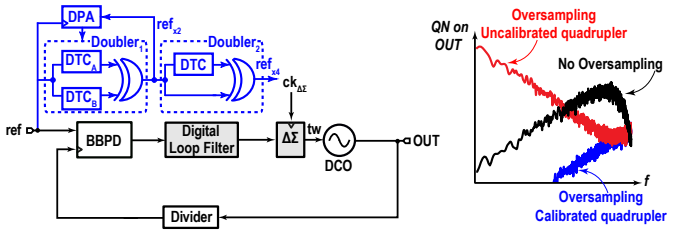

Fig. 6. Quadrupler based oversampling with background DPA calibration.

produces a dithering sequence to modulate the DCO tuning word $tw[k]$, which is a quantized version of the $\Delta\Sigma$ modulator input sequence with addition of high-pass shaped quantization noise $q[k]$. Due to the ZOH block, the QN sequence, $q[k]$ is converted into its time-domain counterpart, $q(t)$, by holding the $q[k]$ values by time durations equal to the ref_{x4} periods (Fig. 4(a)). Being high-pass shaped, the QN sequence $q[k]$ has no DC frequency content (Fig. 4(a)), and therefore can be regarded as a sequence with zero average value. However, if the period of the ref_{x4} waveform is not constant, the $q[k]$ samples will be held constant for different time durations, thus resulting in a non-zero average of the $q(t)$ signal. It follows that the power-spectral-density (PSD) of q(t) in Fig. 4(b) shows a low-frequency plateau that will be converted into an additional $1/f^2$ noise at the PLL output through the DCO frequency-to-phase integration (Fig. 4(c)). On the other hand, note that, despite the oversampling frequency is not constant, the peak of the output PN due to the QN bump disappears (Fig. 4(c)), being shifted to higher frequencies. In the Appendix, the additional random-walk noise contribution is derived as a function of the period error t_e on the ref_{x4} waveform. It is:

$$\mathcal{L}_{RW,QN}(f) = \frac{4}{3}\frac{\Delta f_{res}^2 t_e^2}{T_{ck}}\frac{1}{f^2}. \quad (5)$$

Figure 5 compares the predicted random-walk additional noise at 10 MHz offset from (5) with the one obtained from numerical simulations of the PLL output PN spectrum[8],

[8]Simulation of the simplified case in Fig. 3(b). In this situation, the ref signal has a 50% duty cycle, and the period error t_e is caused by a delay τ_1 of the first doubler DTC different from $T_{ref}/4$ ($t_e = \tau_1 - T_{ref}/4$)

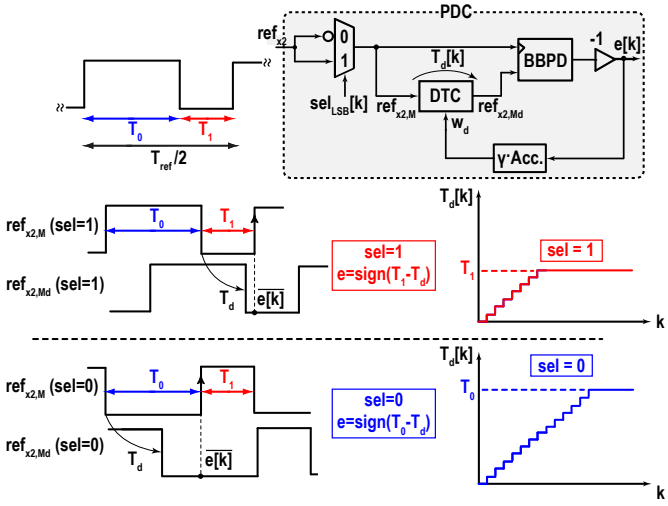

Fig. 7. Period detector circuit (PDC) and operation.

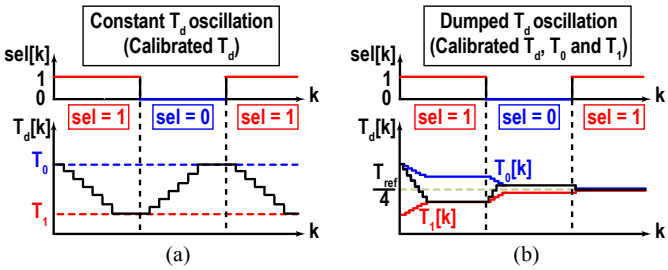

Fig. 8. Basic principle of the simplified DPA calibration: (a) a square wave on sel causes the delay T_d (left) to oscillate between T_0 and T_1 bounds; (b) by dumping of the T_d oscillation both intervals become eventually equal.

demonstrating the effectiveness of (5). Figure 5 also shows that, in order to push the additional random-walk PN 10 dB below the PN of the designed DCO $\mathcal{L}_{dco}(10MHz) \approx$-140dBc/Hz, the period error should be lower than 60 ps, which would be tough to guarantee considering practical PVT variations.

C. Simplified Digital Period Averaging Calibration

Being difficult to achieve a 60 ps delay accuracy over a $T_{ref}/4 = 2$ ns delay or, equivalently, a duty cycle error below 0.75% on the *ref* signal, this section introduces the DPA background calibration technique to correct the main two non-idealities of the XOR-based quadruplers discussed in Section II-B thus allowing to track PVT variations. The first XOR-based doubler is modified by adding a DTC per each branch, as shown in Fig. 6. The DPA algorithm works in background and continuously tune the DTC delays to set all periods of ref_{x4} equal to $T_{ref}/4$. Unlike other frequency-quadrupler calibration schemes based on auxiliary PLL [19], the DPA block extensively relies on the use of a period-detector circuit (PDC), which is composed of a low-power DTC, a bang-bang phase detector (BBPD) and a digital accumulator in feedback (Fig. 7). The behavior of the PDC and the DPA calibration can be initially addressed for the simplified case where the *ref* signal has a 50% duty cycle. i.e. only one of the two main non-idealities are present. In this condition, despite ref_{x2} features a correct period equal to $T_{ref}/2$, it could exhibit a non 50%

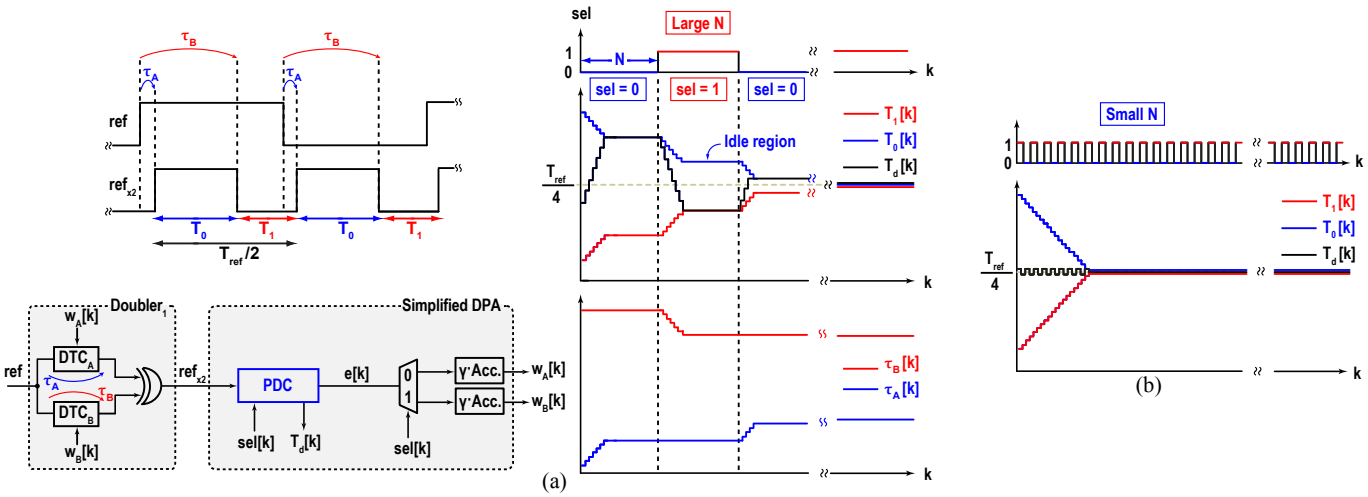

Fig. 9. (a) Simplified digital period averaging system and settling of the DTCs' delays τ_A and τ_B and of the intervals T_0 and T_1 of ref_{x2} for a large value of N, which is the number of ref cycle allocated for each iteration of sel. Idle regions in (a) are avoided by decreasing N as in (b).

duty cycle (as discussed in Section II-B), i.e. the two time intervals T_0 and T_1 in Fig. 7 are different. By feeding the signal *ref*$_{x2}$ to the PDC, as shown in Fig. 7, and setting the selection mux signal *sel* = 1, the BBPD output signal $e[k]$ can be used to provide a comparison between the time interval T_1 and the delay T_d of the DTC inside the PDC block (Fig. 7). In particular, in this condition, $e[k] = Q(T_1 - T_d)$ where $Q()$ is the sign function. Thanks to the digital accumulator on feedback, the PDC is actually a type-I system, and therefore the signal $e[k]$ should be 0, on average, at steady state. In practice, this loop, shifts the delay T_d of the DTC until it matches the value of T_1, as shown in Fig. 7. Analogously, when *sel* = 0, the delay T_d tracks the value of the time interval T_0 (Fig. 7). By applying a square wave signal to *sel*, the value of the delay T_d would continuously oscillate between T_0 and T_1 (Fig. 8). The basic idea of the simplified DPA is to try to dump these oscillations in the time-domain by progressively shrinking the difference between T_0 and T_1 in such a way to make them collapse to a common steady state value, thus guaranteeing[9] $T_0 = T_1 = T_{ref}/4$ as in Fig. 8. Figure 9(a) shows how to implement this concept. Notice that the delay τ_A of DTC$_A$ in the first doubler sets the position of the ref$_{x2}$ rising edge while the delay τ_B of DTC$_B$ sets the position of its falling edge. Therefore, acting on τ_A and τ_B is an effective way to modify the two time intervals T_0 and T_1. The simplified DPA block, shown in Fig. 9(a), leverages this property and modifies τ_A and τ_B based on the values of the signal *sel* and $e[k]$. Figure 9(a) also illustrates the operation of the simplified DPA. When *sel* = 0, the delay T_d approaches the value of T_0. During this transient, the signal $e[k]$ at the PDC output is integrated, and fed to DTC$_A$ to increase the delay τ_A. In this way, the value of the time interval T_0 during the transient would progressively shrink. Thanks to this additional path, at the end of the transient, i.e. when $T_d = T_0$, the net difference between T_0 and T_1 is reduced with respect to its initial value. Analogously, when *sel* = 1, the signal $e[k]$ is integrated and fed to DTC$_B$ to increase the delay τ_B and the corresponding time interval T_1, resulting, again, in a reduction of $T_0 - T_1$ at the end of the transient (i.e. when $T_d = T_1$). It is clear that, after each iteration of the *sel* square wave, the difference between T_0 and T_1 would be progressively reduced, until they eventually become equal. It is worth to notice that the settling time of this algorithm is dependent on the period of *sel* signal iterations, denoted as N in Fig. 9(a). As the algorithm temporarily stops when T_d reaches its final value within each iteration (see the idle regions in Fig. 9(a)), the convergence of the algorithm can be sped-up by adopting a lower value of N, resulting in straight line transients as in Fig. 9(b).

[9]This is guaranteed by the fact that $T_0 + T_1 = T_{ref}/2$ in this simplified case, as shown in Fig. 8.

D. Generalized Digital Period Averaging Calibration

This section is devoted to generalize the simplified DPA algorithm to handle the case in which the *ref* signal has a non 50% duty cycle, i.e. to address the two main non-idealities of XOR-based quadruplers discussed in Section II-B. In this general case, the *ref*$_{x4}$ signal would feature four different periods or equivalently, the *ref*$_{x2}$ time durations denoted as T_0, T_1, T_2 and T_3 in Fig. 10 will be all different. The four edges of the waveform *ref*$_{x2}$ are denoted, instead, as (A), (B), (C) and (D). The DPA is based on the use of a generalized PDC (GPDC) architecture shown in Fig. 10. This circuit guarantees that, by properly selecting the 2 bits *sel* signal, the delay T_d of the DTC converges to the chosen *ref*$_{x4}$ period, thus extending the functionality of the PDC. To explain the operation of the GPDC it is useful to split *sel* into its MSB sel_{MSB} and LSB sel_{LSB}, respectively. Consider the case in which sel_{LSB} = 1, with the corresponding waveforms shown in Fig. 10. The BBPD in the GPDC samples the T_d-delayed version of *ref*$_{x2}$ on the rising edges of ref_{x2}. Since *ref*$_{x2}$ has two rising edges within a *ref* period (edge (C) and edge (A)), the BBPD output e_{PD} assumes two possible values, namely, $e_{PD,1} = Q(T_1 - T_0)$ on edge (C) and $e_{PD,3} = Q(T_3 - T_d)$ on edge (A). To discriminate between those two values, a resampling flip-flop is added at the BBPD output. Its clock ck_{PD} is generated by a phase discriminator circuit depending

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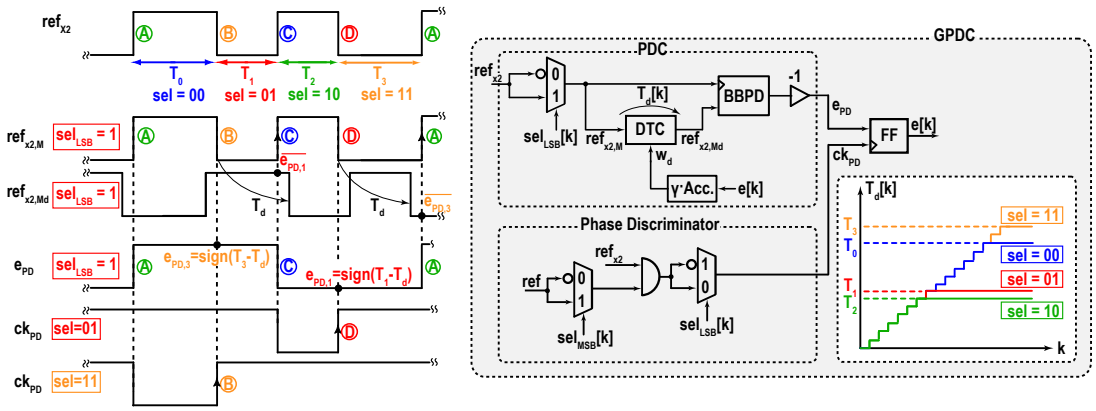

Fig. 10. Generalized period detector circuit (GPDC) operation (left), architecture and principle (right).

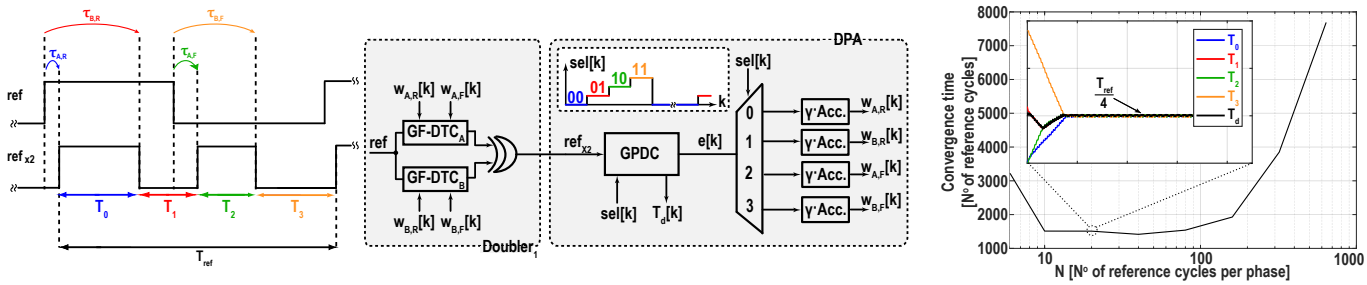

Fig. 11. (a) Digital period averaging architecture and (b) simulated convergence time for a certain number N of reference period per phase.

on the values of *sel*. When sel =01, ck_{PD} has a rising edge synchronous to the edge (D), thus allowing to resampling e_{PD} in such a way that $e[k] = e_{PD,1}$. In case sel =11 $e[k] = e_{PD,3}$ is selected instead. A similar discussion can be made in the case sel_{LSB} = 0, allowing to choose between $e[k] = e_{PD,0} = Q(T_0 - T_d)$ or $e[k] = e_{PD,2} = Q(T_2 - T_0)$. Once the proper $e[k]$ is chosen, it is fed to the DTC, in order to make T_d converge to the chosen period, similar to the PDC.

If the signal *sel* is periodically switched between its possible four values (Fig.11(a)) the delay T_d would continuously oscillates between the four possible values T_0, T_1, T_2 and T_3. By designing the DPA in such a way to dump this oscillation, the convergence of these values to $T_{ref}/4$ will be guaranteed, similarly to what discussed in the previous section. To this aim, the feedback signals are used to act on the DTCs within the doubler. Note that this time, DTC_A and DTC_B in Fig. 11(a) are able to separately control the delays on the rising and falling edges of their input signal according to the values of two control words [10]. In this way the doubler delivers a ref_{x2} waveform with four edges that can be independently shifted depending on the four control words. To avoid unwanted transitions when the control is switched to perform the two different delays, on the rising and falling edges, a Glitch-Free (GF)-DTC architecture is employed, whose implementation is described in Section II-E.

The GPDC output $e[k]$, after demultiplexing, is fed to one of the four accumulators controlling the four delays of the DTCs, which, like in the simplified DPA, control the edge at the beginning of the considered interval. The net result is that the four intervals are averaged to the same value, and being their sum fixed by the reference period (Fig. 11(a)), they converge to the same $T_{ref}/4$ value within an error set by the LSB of the DTCs. Figure 11 (b) shows the convergence time with respect to the number N of reference periods allocated per each phase of sel. For N <80 and N >10 the convergence time reaches a flat region where the transient of the four periods becomes a straight line without idle regions[11]. The actual N value was therefore chosen within this interval without criticalities leading the DPA calibration to equalize the periods of the x4 reference waveform with a resolution set by the LSB of the DTCs.

Figure 5 shows the impact on the PN at 10MHz offset induced by the finite LSB resolution. Since the residual period error of the DPA is comparable to t_{LSB}, the simulated phase noise, PN_{DPA}, follows the estimate PN_{est} in (5) using t_e=t_{LSB}. The results in Fig. 5 also suggest that the $1/f^2$ noise is only related to the power of the period error. Therefore, the DTCs of the DPA do not need any $\Delta\Sigma$ dither, thus simplifying the digital implementation. Moreover, to keep this contribution below -150dBc/Hz the DTCs resolution t_{LSB} should be lower than 60ps, as derived at the end of Section II-B. In a 28nm CMOS technology, this value can be easily obtained over PVT variations with a DTC based on an inverter chain.

[10]Both the delays and the control words of DTC_A and DTC_B employ as notation the subscripts R and F for rising and falling edges respectively.

[11]The change of the signal sel may induce an invalid GPDC output $e[k]$ in the first reference cycle after the sel signal switching. However, as the invalid $e[k]$ sample only affects 1 over N reference cycles, its effect is averaged out for large values of N (N > 10), while it causes an increase of the GPDC calibration time for small N values (N <10), as shown in Fig. 11(b).

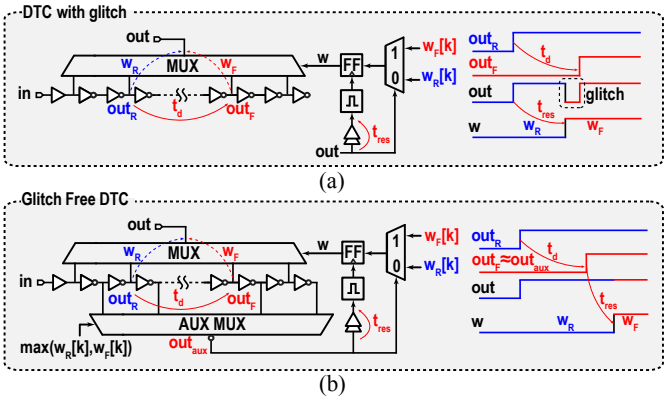

Fig. 12. Comparison between (a) the typical inverter chain based DTC architecture and (b) glitch-free DTC circuit.

E. Glitch-Free DTC

To target a compact implementation of DTC_A and DTC_B in Fig. 11(a), an architecture based on a chain of inverter cells was adopted, as shown in Fig. 12(a). The DTC delay can be controlled through a multiplexer by selecting the proper inverter output within the chain with the control signal w. To independently set the DTC delays on the rising and falling edges of the input signal in, w should assume two different values, w_R and w_F, within the input signal period. This can be in principle achieved with the scheme in Fig. 12(a), where the DTC output out drives a multiplexer to select between w_R and w_F and a resampling stage comprising a pulser and a t_{res}-delay stage to avoid meta-stability. Unfortunately, despite its simplicity, this circuit would feature glitches at the out signal whenever w_R and w_F are largely different. As shown in Fig. 12(a), when w is changed from w_R to w_F and $w_F >> w_R$, the sudden change of w causes the output signal to immediately switch from out_R to out_F. If the delay t_d between out_R and out_F is larger than t_{res}, out_F would have a value different from out_R at the switching instant, therefore causing a glitch on the out signal (Fig. 12(a)). This is solved with the proposed glitch-free (GF)-DTC shown in Fig. 12(b). In this architecture, the control w is generated by controlling the resampling stage and the input mux with the signal out_{aux}, which is provided by an auxiliary multiplexer connected to the DTC inverter chain as in Fig. 12(b). The auxiliary multiplexer control signal is generated as the maximum of the digital words w_R and w_F. In this way, the switching instant of the w signal always occurs after the edges of both out_R and out_F, therefore avoiding glitches on out, as shown in Fig. 12(b).

III. True-in-Phase Combiner for PN Suppression

As discussed in Section I, the oscillator PN is one of the limiting factors for spot noise and jitter in a PLL. Unfortunately, the minimum PN obtainable with a generic oscillator based on a parallel LC tank is limited by the available supply voltage. To overcome this limitation, previous solutions were based on LC oscillators coupled by reconfiguration switches [18], [24], [25] in order to arbitrarily trade additional power consumption with lower PN, thus being able to rearrange the system from a low-power mode (single-core) to a low-jitter mode. However, the PN of resistively-coupled architectures

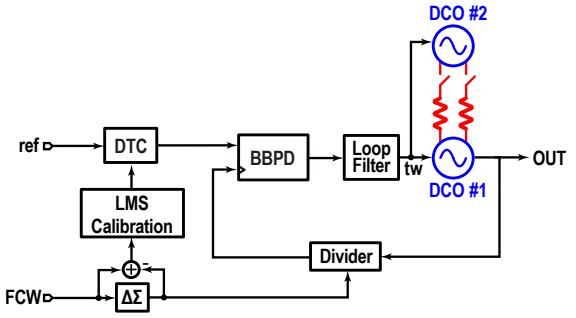

Fig. 13. PLL based on multi-core oscillators.

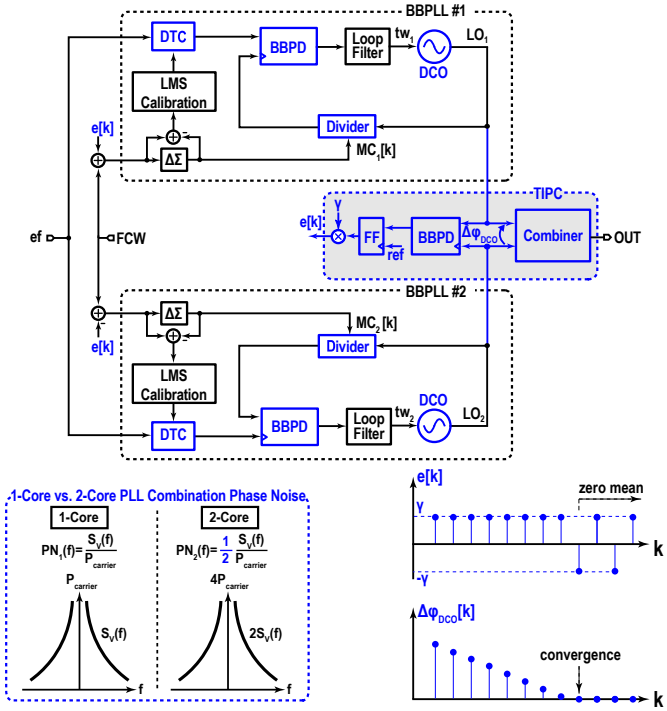

Fig. 14. Multiple PLL combination with true-in-phase combiner (TIPC).

(Fig. 13) may not exactly scale down by -3dB by doubling the number of oscillator cores, thus affecting the power-efficiency of this approach. This is due to mismatches between the resonant frequencies of the coupled tanks, which induce a current to flow into the coupling resistive network, thus worsening the PN performance [24] [12] . Therefore, to improve PN scaling the switch size should be increased, but this comes at the cost of a tuning range reduction.

An additional issue of multi-core oscillators is that their design complexity dramatically increases with the number of cores. In fact, to avoid any mismatch between the cores, they should be accurately placed and connected in order to avoid any asymmetry. However, this becomes extremely challenging when a multi-core oscillator is embedded within a practical PLL circuit, where a large number wires of the

[12]In other topologies without explicit coupling network, such as the circular oscillator in [36], passive networks are anyhow present to quench the undesired oscillation modes. Also in these cases shifts of the tanks' components from the nominal values cause some power to be delivered by the transconductors to other modes, thus introducing additional losses, similar to the general case of resistively-coupled oscillators.

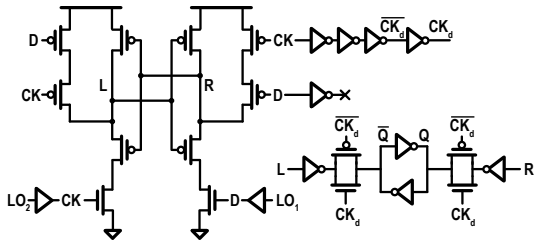

Fig. 15. BBPD architecture.

DCO tuning word tw must be symmetrically connected to each core individually (Fig. 13).

Finally, it is worth noticing that employing a multi-core oscillator architecture in a PLL would result in almost a two-fold increase in the PLL power consumption (and area occupation) since this figure is generally dominated by the LC oscillator contribution. However, it is clear that the other PLL noise sources would be unaffected using this approach, meaning that the two-fold increase in power consumption is not associated to a two-fold reduction of the overall noise [13].

These limitations can be overcome by combining the output of two independent PLLs (Fig. 14). In this case, the sum of the two carriers perturbed by uncorrelated noise sources, causes a 3dB reduction of the PN contributions of both the DCOs and the other noise sources in each PLL, such as those from phase detectors, dividers, and digital to time converters[14].

Since the tuning words of the two DCOs within the different cores of the multi-PLL architectures are independently set by each loop, this architecture is intrinsically insensitive to resonance frequency mismatches of the two core tanks. Therefore, the overall design is greatly relaxed since the asymmetries in the layout are not as critical as for multi-core oscillator architectures and the DCO tuning word routing is eased. In addition, a multi-core PLL can be easily reconfigured to dissipate lower power by simply turning off one of the implemented cores, without PN impairments due to coupling network.

Nevertheless, the two PLL outputs may suffer some misalignment due to mismatches and PVT variations on the two paths, leading to a lower output amplitude, thus degrading power efficiency and increasing the impact of noise from the following stages. In this work, this problem is solved by introducing a digitally assisted combiner, denoted as true-in-phase combiner (TIPC) in Fig. 14. The block produces an error signal, $e[k]$, using a BBPD, whose output is first resampled to reduce the switching frequency of the subsequent digital circuits, and then multiplied by a small gain, γ. This, in practice, implements a narrow-band filtering operation on the BBPD output, thus reducing the contribution of possible noise sources of the TIPC circuit. To align the two PLLs outputs, unlike [5] that requires large-range (thus noisy) DTCs, the TIPC differentially adds $e[k]$ to the frequency control word of the two PLLs. Since an integration exists between the divider input and the phase of the output waveforms, the TIPC loop implements a type-I control, thus eventually canceling out the mean of $e[k]$. In this way, the true in phase combiner realignes and combines the two PLL outputs to ensure both PN reduction of all the PLL noise sources and maximum output power over PVT variations.

Both the BBPD in the TIPC and the BBPDs in the two PLLs have the same architecture shown in Fig. 15, which guarantees a symmetric load on the two paths and ultra-low time offset (<100fs). It follows that the amplitude reduction of the power combiner output signal due to the resulting misalignment between the two PLLs is negligible. Thanks to the scaled CMOS process this architecture works within the output frequency range over PVT variations. Differently from the BBPD in the reference path, the BBPD in the TIPC auxiliary loop works around 10GHz. However, it is sized with much smaller transistors since no critical jitter requirements are posed by the TIPC auxiliary loop. Therefore, the resulting power dissipation is of only 70μW.

IV. Implementation and Measurements

Figure 16 shows the block diagram and the die micrograph of the implemented two core PLL architecture. The background calibrated frequency quadrupler generates both the clocks of the $\Delta\Sigma$ modulators in the two loops to suppress the quantization noise of the DCOs. Fractional-N operation is enabled by driving the dividers with a $\Delta\Sigma$ modulator and canceling their QN with a DTC-based least mean square (LMS) cancellation loop [12]. To achieve low-jitter and low fractional spurs in fractional-N mode, the implemented DTC exploits several circuit-level approaches to reduce non-linearity and memory effects [32], such as the use of resampling flip-flops of the DTC input code to avoid DTC delay dependences on previously applied inputs and dummy switches to reduce charge injection within the DTC capacitor bank. At system-level, the DTC range reduction technique described in [12], [18] was exploited (for simplicity it is not shown in Fig. 16). The DCOs have a class-B topology with tail resonator to minimize flicker noise conversion [38], [39]. This system was implemented in a 28 nm CMOS process, while dissipating 36 mW, excluding the input and output buffers, and occupying an active area of 0.47mm^2. The reference frequency is 125MHz and it is fed to the two PLLs using an external SAW oscillator, while the output PLL frequency ranges from 8.5 to 10.5GHz.

To demonstrate the effectiveness of the DPA calibrated quadrupler in reducing the quantization noise, Fig. 17 shows the measured PN and jitter of a single core PLL at 8.6GHz in integer-N channel operation. Turning on the oversampling and the DPA calibration, the integrated jitter from 1kHz to 100MHz reduces from 86 to 68 fs, while the large quantization noise bump reduces by 18dB. The extra power dissipation was only 130μW. The jitter reduction from 86 to 68 fs corresponds to suppress a noise contribution of about 53fs, which is in line with the value estimated in Section II-A based

[13]In practice, it can be derived that the PLL jitter would drop by 1.5 dB, since only the DCO noise contribution would be halved.

[14]A similar 3dB reduction may be obtained in a single PLL core by doubling the power dissipation of each building block. However, pursuing this approach, the performance of some critical analog blocks may worsen due to the larger local current spikes. For example, the DTC would experience larger supply ripples on its local supply network thus worsening its linearity and therefore PLL spectral purity in fractional-N mode [37]

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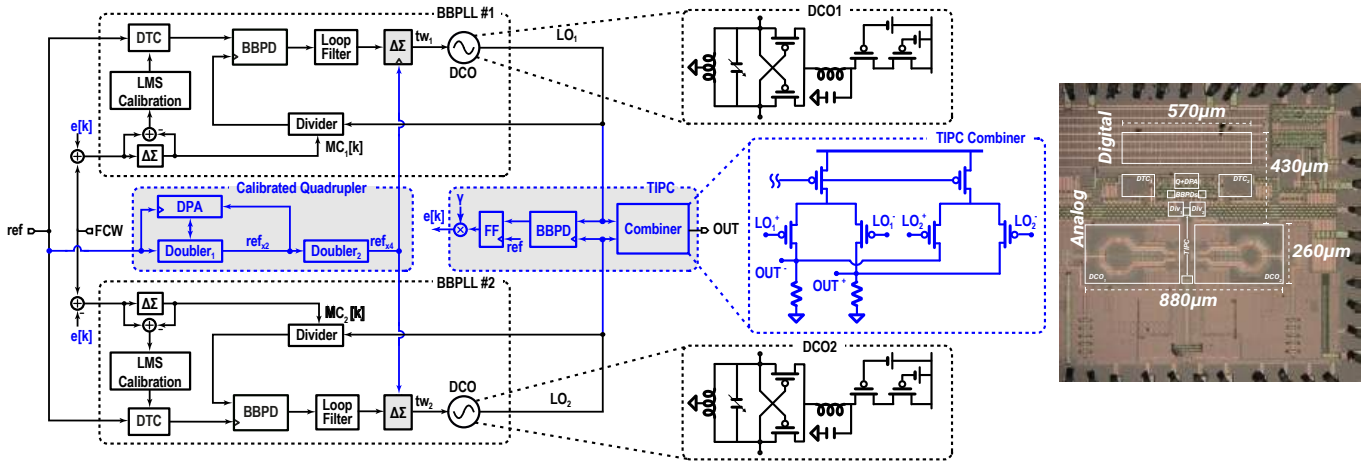

Fig. 16. Implemented architecture and die micrograph.

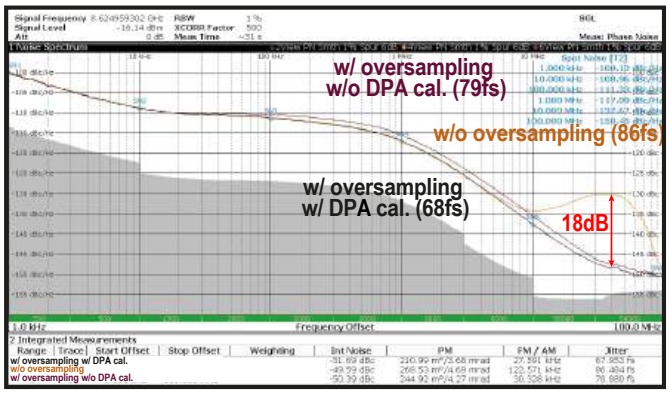

Fig. 17. Measured integer-N phase noise performances of the implemented single-core PLL.

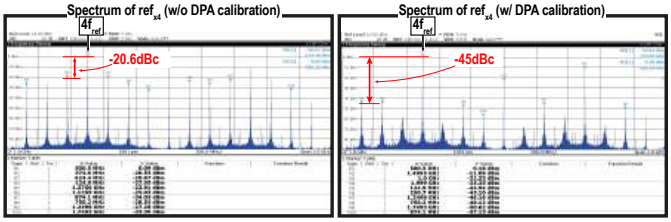

Fig. 18. Spectrum of the quadrupler output with and without the DPA calibration.

on (1). Disabling the DPA calibration while keeping clock multiplication, the PLL jitter increases up to 79fs due to the extra $1/f^2$ noise induced by the clock period errors of the $\Delta\Sigma$ modulator.

The correct calibration of the DPA can be checked by looking to the sub-harmonics of the x4 reference clock (Fig. 18). Using the DPA, the maximum spur with respect to the 500MHz carrier reduces from -20.6 to -45 dBc. The last value is in agreement with the 12 ps resolution in the typical corner of the DTCs embedded in DPA unit.

The performance in integer-N mode were reported in [9]. Figure 19 shows instead the PN spectrum in fractional-N mode, at a 1.9kHz offset frequency from the integer-N 8.6 GHz channel. The total integrated jitter, including the power of spurs, reduces from 89.4 to 71.8 fs. The measured worst case fractional-N spur, shown in Fig. 20, is equal to -59.7 dBc, while the far-out spectrum is dominated by the -70.2 dBc reference spur at 125MHz offset.

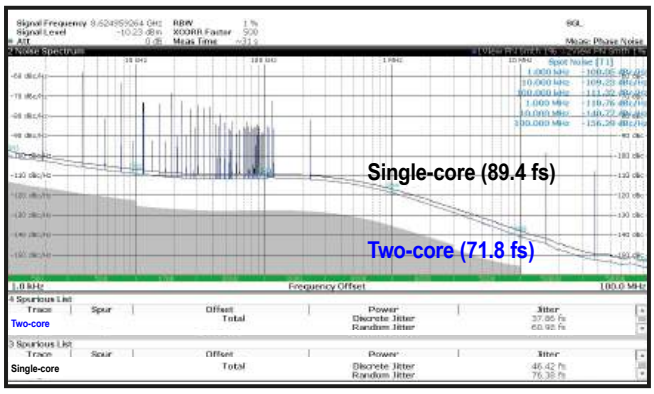

Fig. 19. Measured fractional-N phase noise of the implemented single and two-core PLL and measured spectrum of the two-core PLL.

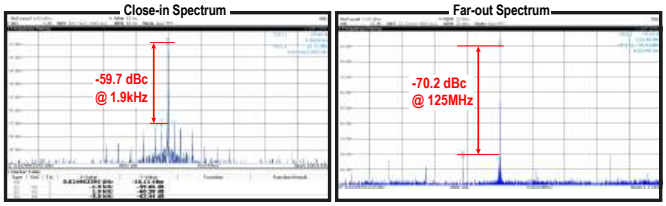

Fig. 20. Measured fractional-N spectrum of the two-core PLL.

The table in Fig. 21 compares the measured performances at 8.6 GHz with the state-of-art.

V. Conclusions

This work presents a two-core 8.5-to-10.5-GHz fractional-N BBPLL achieving a spot-noise level of -140.7 dBc/Hz at 10 MHz offset, which at least 4dB better than other digital PLLs, while retaining a low-integrated jitter of 72 fs. The proposed DPA background calibration enables the use of a low-complexity and power efficient XOR-based quadrupler for the generation of the oversampled DCO $\Delta\Sigma$ clock for quantization-noise suppression. The proposed TIPC, instead, allows to achieve a phase-noise reduction by combining the outputs of two PLL cores, exhibiting a 1.9 dB jitter reduction, which outperforms previous multi-core architectures.

	This Work	S. Karman RFIC '21	W. Wu JSSC '21	E. Thaller ISSCC '21	J. Kim ISSCC '21	M. Mercandelli ISSCC '21
PLL Architecture	Digital BBPLL	Digital BBPLL	Analog	Digital SS-PLL	Digital SS-PLL	Digital S-BBPLL
Type	Fractional-N	Fractional-N	Fractional-N	Integer-N	Fractional-N	Fractional-N
Number of Cores	2	2	2	2	1	1
Output Frequency Range [GHz]	8.5 to 10.5	18.9 to 22.3	5 to 7	12.1 to 16.6	14 to 16	12.9 to 15.1
Reference Frequency [MHz]	125	100	76.8x2	245.76	150	250
Total Jitter Int-N $\sigma_{int.}$ [fs]	54.6	N/A	N/A	49.9	N/A	71.4
RN Jitter Frac-N $\sigma_{frac.}$ [fs]	61.0	174.2	80	N/A	N/A	79.5
Total Jitter Frac-N σ_{spurs} [fs]	71.8	N/A	93.2[1]	N/A	104	107.6
1-to-2 Cores Jitter Reduction [dB]	1.9	1.47	1.2	N/A	N/A	N/A
Integration Bandwidth [Hz]	1k-100M	10k-10M	1k-40M	10k-100M	1k-100M	10k-100M
Fractional Spur [dBc]	-59.7	-45	-72.4	N/A	-61	-50.4
Reference Spur [dBc]	-70.2	-63.7	-72	-75.1	N/A	-73.2
Phase Noise @10MHz[5] [dBc/Hz]	-140.7	-132.5	-139.7	-136	-125.8	N/A
Power Dissipation [mW]	36	37.1	14.2	56	7.3	10.8
$FoM_{Int.}$[2] [dB]	-249.7	N/A	N/A	-248.6	N/A	N/A
FoM_J[3] [dB]	-248.7	-239.5	-250.4	N/A	N/A	-251.7
FoM_S[4] [dB]	-247.4	N/A	-251.5[1]	N/A	-251	-249
Active Area [mm^2]	0.47	0.65	0.31	0.5	0.21	0.21
CMOS Process [nm]	28	55	14	16	65	28

[1]1-core [2]$FoM_{Int.} = 10\log_{10}[(\text{Power}/1\text{mW})\cdot(\sigma_{int}/1\text{s})^2]$ [3]$FoM_J = 10\log_{10}[(\text{Power}/1\text{mW})\cdot(\sigma_{frac}/1\text{s})^2]$

[4]$FoM_S = 10\log_{10}[(\text{Power}/1\text{mW})\cdot(\sigma_{spurs}/1\text{s})^2]$ [5]Normalized @ 8.625GHz carrier

Fig. 21. Performance summary and comparison with prior art.

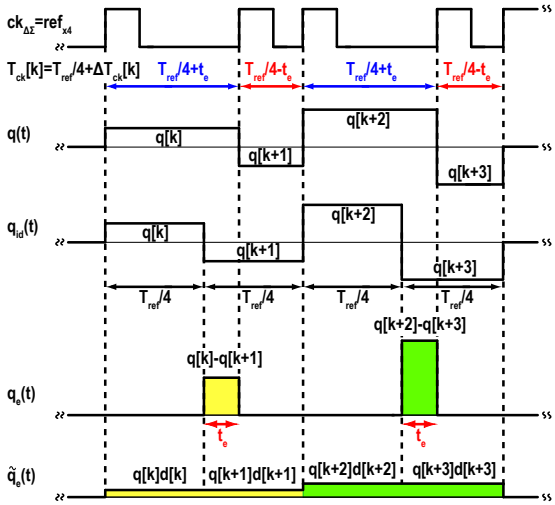

Fig. 22. Effect of the $\Delta\Sigma$ period error on the QN $q(t)$. The latter can be approximated by the sum of the ideal high-passed $q_{id}(t)$ with the additional error $\tilde{q}_e(t)$, which produces an additional low-frequency noise.

APPENDIX A
$\Delta\Sigma$ MODULATOR DISTORTION

The low-frequency noise plateau induced by the $\Delta\Sigma$ modulator QN distortion in Fig. 4, which translates into a $1/f^2$ noise at the DCO output, can be estimated considering the simplified case in Fig. 3(b). In this situation, the ref signal has a 50% duty cycle, and the periodic period error $\Delta T_{ck}[k]$ (Fig. 22) is due to a delay τ_1 of the doubler DTC different from $T_{ref}/4$ ($t_e = \tau_1 - T_{ref}/4$). As a consequence, the area of each pulse is changed, thus affecting the average of the $\Delta\Sigma$ QN sequence $q[k]$ on the time waveform $q(t)$ in Fig. 22. The low-frequency $1/f^2$ noise, can be estimated by decomposing $q(t)$ as the sum of the ideal high-passed $q_{id}(t)$, which would be the only source of QN with an ideal constant clock period, plus the additional $q_e(t)$, which is the source of the low-frequency error, as it is shown in Fig. 22. To simplify the derivation but to still maintain the same low-frequency spectral component, $q_e(t)$ can be approximated by $\tilde{q}_e(t)$, which is based on a train of *constant-width* rectangular pulses $g(t)$, whose amplitude is the $\Delta\Sigma$ QN $q[k]$ modulated by a factor $d[k] = \Delta T_{ck}[k]/T_{ck}$

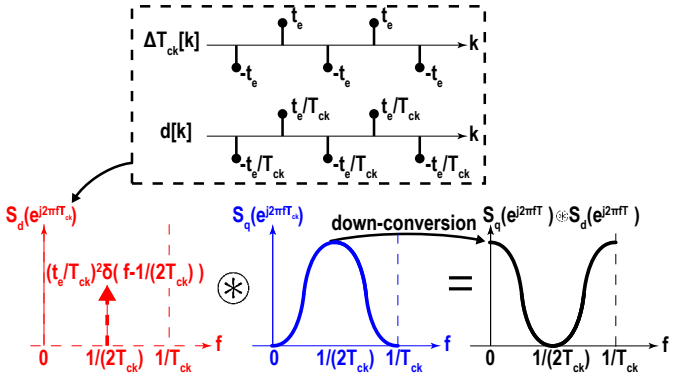

Fig. 23. Spectrum folding due to the circular convolution $S_q(e^{j2\pi fT_{ck}}) \circledast S_d(e^{j2\pi fT_{ck}})$.

guaranteeing the same area between the pulses of $q_e(t)$ and $\tilde{q}_e(t)$ (Fig. 22). It is

$$\tilde{q}_e(t) = \sum_{k=-\infty}^{\infty} q[k]d[k]g(t - kT_{ck}). \tag{6}$$

where T_{ck} is the mean of the $\Delta\Sigma$ clock period. According to [40], the spectrum of the pulse amplitude modulated signal $\tilde{q}_e(t)$ is

$$S_{\tilde{q}_e}(f) = \frac{S_{q\cdot d}(e^{j2\pi fT_{ck}})}{T_{ck}} S_g(f) \tag{7}$$

where $S_{q\cdot d}(e^{j2\pi fT_{ck}})$ is the power spectral density (PSD) of the discrete sequence $q[k]d[k]$, while $S_g(f)$ is the one related to the T_{ck}-rectangular pulse. According to the Parseval theorem, (7) can be rewritten as

$$S_{\tilde{q}_e}(f) = \frac{S_q(e^{j2\pi fT_{ck}}) \circledast S_d(e^{j2\pi fT_{ck}})}{T_{ck}} S_g(f), \tag{8}$$

where the operator $\circledast$ is the cyclic convolution on a period $1/T_{ck}$. Figure 23 shows both the $1/T_{ck}$-periodic discrete PSD $S_d(e^{j2\pi fT_{ck}})$, which has one tone at $1/(2T_{ck})$ with an amplitude $(t_e/T_{ck})^2$, and the high-passed $S_q(e^{j2\pi fT_{ck}})$ of the QN $q[k]$ induced by a 2^{nd} modulator with resolution Δf_{res}, [34]:

$$S_q(e^{j2\pi fT_{ck}}) = \frac{\Delta f_{res}^2}{12} 16 sin^4\left(\pi \frac{f}{f_{ck}}\right). \tag{9}$$

It follows that the low frequency component on $\tilde{q}_e(t)$ is caused by the down-conversion of high frequency component of $S_q(e^{j2\pi fT_{ck}})$ around $1/(2T_{ck})$ down to 0, as depicted in Fig. 23. The last missing PSD in eq. (7) is the one related to the rectangular pulse $g(t)$, which is

$$S_g(f) = T_{ck}^2 sinc^2\left(\frac{f}{f_{ck}}\right). \tag{10}$$

Therefore, the additional low-frequency trend of $q(t)$ can be traced in the zero value of (8), that is

$$S_q(0) = S_{q_e}(0) \approx S_{\tilde{q}_e}(0) = \frac{\frac{\Delta f_{res}^2}{12} 16 \cdot \left(\frac{t_e}{T_{ck}}\right)^2}{T_{ck}} T_{ck}^2. \tag{11}$$

As a consequence, the resulting effect on the output PN is

$$\mathcal{L}_{RW-QN}(f) = \frac{S_{\tilde{q}_e}(0)}{f^2} = \frac{4}{3}\frac{\Delta f_{res}^2 t_e^2}{T_{ck}}\frac{1}{f^2}. \tag{12}$$

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