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Organic Electronics Picks Up the Pace: Mask-Less, Solution Processed Organic Transistors Operating at 160 MHz

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Organic printed electronics has proven its potential as an essential enabler for applications related to healthcare, entertainment, energy, and distributed intelligent objects. The possibility of exploiting solution-based and direct-writing production schemes further boosts the benefits offered by such technology, facilitating the implementation of cheap, conformable, bio-compatible electronic applications. The result shown in this work challenges the widespread assumption that such class of electronic devices is relegated to low-frequency operation, owing to the limited charge mobility of the materials and to the low spatial resolution achievable with conventional printing techniques. Here, it is shown that solution-processed and direct-written organic field-effect transistors can be carefully designed and fabricated so to achieve a maximum transition frequency of 160 MHz, unlocking an operational range that was not available before for organics. Such range was believed to be only accessible with more performing classes of semiconductor materials and/or more expensive fabrication schemes. The present achievement opens a route for cost- and energy-efficient manufacturability of flexible and conformable electronics with wireless-communication capabilities.

The development of new applications in the fields of healthcare, energy, distributed sensing, and entertainment will require the integration of electronic functionalities into everyday objects. Organic electronics has gained its place among the promising technologies to this purpose, owing to a set of distinctive features:[1] first, it is compatible with flexible substrates, which allows its integration with objects characterized by non-conventional form factors; second, it enables the use of deposition techniques derived from the graphic arts and gives access to cost-efficient manufacturing; third, selected organic materials are biocompatible, allowing for a high degree of integration between electronics and biology. The impressive progress in this field has been driven by: i) the enhancement of a set of figures of merit, primarily the charge mobility of the semiconductors, now well exceeding amorphous silicon and rivaling low temperature deposited metal oxides;[2] ii) the strengthening of cost- and energy-efficient fabrication strategies, with the notable examples of printing[3,4] and laser processing,[5–7] which are now suitable for the micron-scale patterning of functional materials on a large area; iii) the demonstration of a set of proof-of-concept applications, including green/biodegradable electronic devices,[8] electronic skins, and conformable patches for personal healthcare[9–12] or flexible organic microprocessors.[13]

However, in order to widen the set of applications that can be envisioned, a set of functionalities is still lacking. Among these, wireless communication between distributed electronic sensors/actuators and data-processing devices, or fast addressing capabilities for large-area arrays of sensors or light-emitting devices. The implementation of these functionalities would enable flexible large-area displays or sensor arrays and the creation of distributed wireless networks of electronic devices within the Internet of Things framework.[14] So far, this set of applications has been considered out of reach for organic electronics.

A fundamental requirement to this goal is the realization of organic transistors, the basic building block of electronic circuits, operating at frequencies well above several tens of MHz. Such performance should also be obtained with the sole use of mask-less and scalable fabrication processes, in order to retain the manufacturability edge of organic devices.[15]

One of the most widely adopted figures of merit to quantify the maximum operation frequency of single transistors and allow comparison among different technologies is the transition frequency f_t, namely the frequency for which the ratio between the small-signal drain and gate currents is unity.[16] To date, the highest f_t obtained for an Organic Field-Effect Transistor (OFET) is 27.7 MHz .[17] Since f_t is proportional to the bias voltage, some

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authors have used the voltage-normalized transition frequency f_t/V as a more convenient figure of merit to assess the relative performance of transistor technologies.[5,18,19] In this case, the highest f_t/V value achieved for OFETs is 2.23 MHz V^{-1},[20] achieved by virtue of a metal-oxide/self-assembled monolayer dielectric with high areal capacitance (700 nF cm^{-2}), a sub-micron channel length defined via high-resolution silicon stencil masks and extremely low contact resistance (29 Ω cm) between gold electrodes and a small-molecule organic semiconductor. These results, however, together with the wide majority of the works on high-frequency OFETs, included masks and/or evaporation steps in the process flow.[21–24] Such an approach, while allowing the access to improved performances by virtue of enhanced control over the deposition of the functional layers, poses a number of difficulties in terms of the future scalability to cost-efficient mass production. The sole use of mask-less direct-writing or solution-based techniques largely complicates the achievement of high-frequency operation, an issue also testified by the very limited number of attempts in the past.[5,25–28]

As of now, despite the technologies and materials exhibiting the performances required for high-frequency operation in excess of several MHz and approaching the 100 MHz range (i.e., charge mobility approaching 1 cm^2 Vs^{-1} and patterning resolutions below 1 µm) are in principle available, further progress has been hampered by a set of critical aspects that have been often overlooked. Primarily, the achievement of high effective charge mobility in downscaled transistors requires to obtain normalized contact resistances ($R_c W$) below 1 kΩ cm (or less, depending on the other physical parameters and bias point of the transistor), which have been rarely demonstrated.[19] This aspect is intertwined with the need for reduction of the capacitive parasitism related to the gate-to-source and gate-to-drain geometrical overlap, which, in the frame of the current-crowding injection model, also affects charge-injection in a non-trivial way.[15] Finally, the design of efficient strategies for the dissipation of the generated heat becomes of paramount importance in order to prevent the destructive breakdown of the device and to allow for continuous-mode operation: downscaled OFETs with channel lengths in the order of the µm, sustaining a current per unit width in excess of 1 mA mm^{-1} and voltages in the range of few tens of volts, need to dissipate efficiently a power density in the range 10 to 100 Wmm^{-2}, which can easily lead to thermal breakdown of the device. The latter is not surprising, considering that the constituting materials, in particular plastic substrates, are characterized by a very low thermal conductivity, making heat dissipation highly inefficient. Recently, it was proposed that, for some applications (e.g., switching power converters, pulsed-mode data transfer), this can be circumvented by operating the transistor in pulsed mode, which allowed to reach a record f_t of 40 MHz at a bias of 8.6 V in such operation regime.[29] However, fully exploiting the possibilities offered by a high-frequency organic technology requires continuous-mode operation, which in turn requires the adoption of efficient dissipation strategies.

Here we show that a route for the realization of high-frequency OFETs operating at a record-high f_t of 160 MHz and f_t/V of 4 MHz V^{-1} can be implemented with a combination of scalable laser-based direct-writing techniques and solution-based deposition of organic polymers. We carefully selected a set of solutions to the problems illustrated above that complies with the requirement of a fully mask-less and solution-based process flow: these include laser-based patterning of metallic inks with a micron-scale resolution, the modification of the electrodes with a self-assembled monolayer for the achievement of low contact resistance and the adoption of a substrate with high thermal conductivity. With this result, we prove that operational frequencies in excess of 100 MHz can be achieved with organic transistors. Moreover, we do not only show a working organic transistor with the highest f_t to date and the highest f_t/V for continuous operation, but we also demonstrate that a route for the achievement of this performance with scalable, mask-less, and solution-based techniques is available, and that the future implementation of cost- and energy-efficient mass manufacturing of high-performance organic electronic applications is credible.

We realized high-frequency OFETs in a bottom-contact, top-gate architecture with the layout schematized in **Figure 1**a, carefully selecting the architecture, materials, and processes in order to overcome a variety of limitations to high-frequency operation.

Our fabrication process relies on the flow illustrated in Figure 1b. We selected femtosecond-laser sintering as a direct-writing patterning technique for the realization of micron-scale conductive electrodes for OFETs. Such an approach was successfully adopted in the past for the realization of metallic grids[30] and OFETs,[7,31,32] including high-frequency, direct-written, and printed OFETs,[27,33] also on plastic substrate.[5] The choice of the proposed fabrication scheme is advantageous for a variety of future implementations into a wide set of applications, by virtue of its digital nature and compatibility with different substrate materials.

However, devices of the kind we realize in this work, when fabricated on plastic, are prone to suffer from thermal runaway or breakdown (described later in the text), due to the significant amount of power density in the channel region of the device and to the limited thermal dissipation properties of plastics (commonly exhibiting thermal conductivity in the range 0.1–0.5 Wm^{-1} K^{-1}). To comply with the need for efficient thermal dissipation of such generated heat, we adopted here a highly thermally-conductive substrate of aluminum nitride (AlN), exhibiting a thermal conductivity in the order of 170 Wm^{-1} K^{-1}.

To fabricate our OFETs, we first coat our substrate with an Ag-nanoparticle ink, then we locally induce the agglomeration of the metal nanoparticles into conductive structures via laser sintering.[5] Then, the unprocessed part of the ink is washed out with an organic solvent, leaving high-resolution conductive patterns with a thickness of 70 nm on the substrate. These structures will constitute the source and drain electrodes of the realized OFETs, yielding a channel length $L = 1.2$ µm, a channel width $W = 800$ µm, an electrode width $L_c = 1.7$ µm. To promote an efficient charge injection from such electrodes into the semiconductor, we then induce the self-assembly of a monolayer of dimethylamino(benzenethiol) (DABT) on the surface of the metallic patterns.[34] Then, we adopt the widely-studied and good electron transporting semiconducting co-polymer poly[*N*,*N*'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene), P(NDI2OD-T2), and deposit a thin layer of such material via off-centered spin-coating from a solution in toluene. Such a selection of deposition technique and solvent yields a semiconducting layer with enhanced charge transport properties thanks to the promotion of aggregates

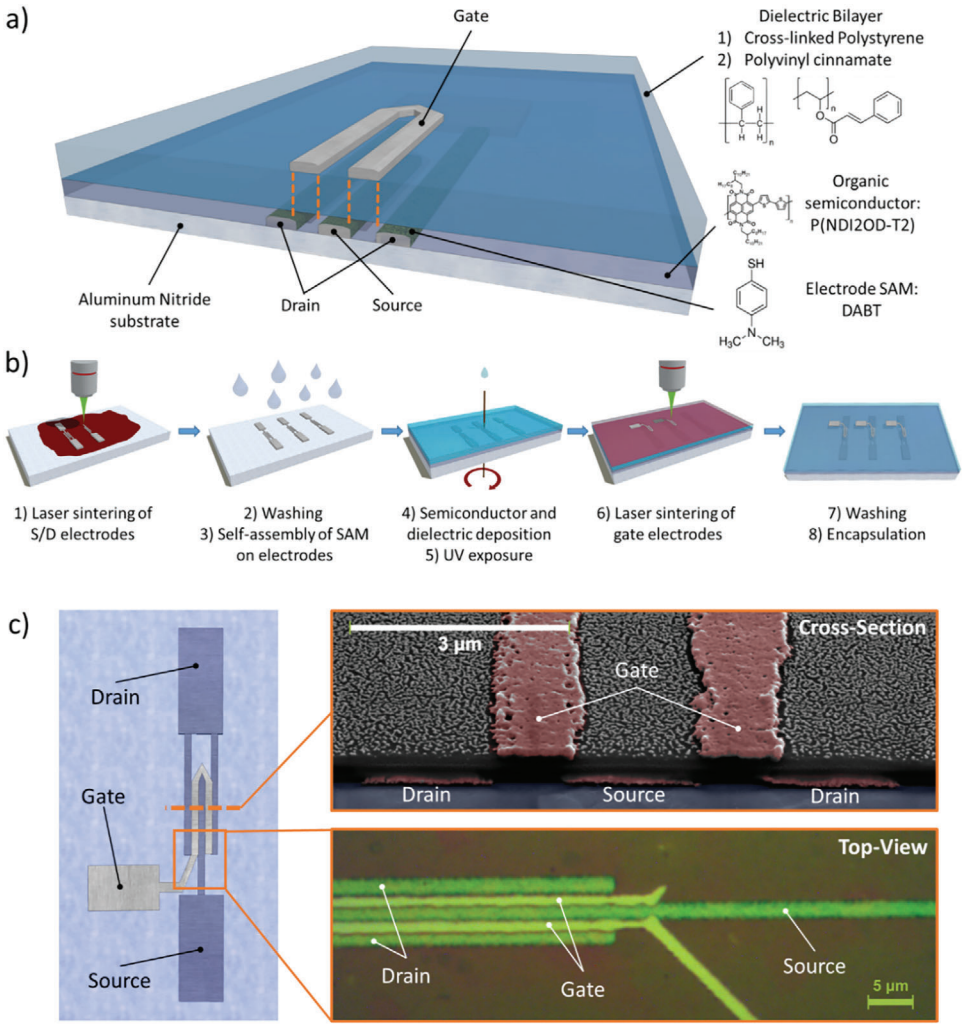

Figure 1. a) 3D sketch of the realized OFET architecture (not in scale), alongside with the adopted materials. b) Scheme of the device fabrication process. c) Sketch of the realized device (not in scale), with a top-view micrograph of the active region (bottom right, rotated by 90°) and a cross-sectional SEM image of the active area and the electrodes (top right). The particulate residuals on the top layer, at the sides of the gate electrode, are part of a gold coating specifically deposited for the imaging, not present in the measured devices.

formed in the solution, which in turn yields the formation of a layer of aligned polymer nanofibrils.[35,36] We then adopted a bilayer dielectric: we first deposit a 40-nm-thick layer of polystyrene blended with an azide-based crosslinker (1,11-Diazido-3,6,9-trioxaundecane) and we cross-link such layer via UV-light exposure at a wavelength of 256 nm. On top of the polystyrene interlayer, we spin-coat a 300-nm-thick layer of poly(vinyl cinnamate), which is then analogously photo-crosslinked. The complete dielectric bilayer exhibits an areal capacitance $C_{diel} = 8.54$ nF cm^{-2}, calculated using the literature value of 3.4 for the dielectric constant of poly(vinyl cinnamate) and a value of 2.6 for cross-linked polystyrene (determined from our measurements on capacitor devices). The top gate electrode is then realized via laser sintering in correspondence of the transistor channel, keeping the overlap with source and drain electrodes low, to comply with the need of reducing the overlap capacitive parasitism. This is the first time laser sintering[31] is used for the fabrication of gate electrodes on polymer dielectrics in top-gate structures. Encapsulation of the device to prevent degradation induced by the exposure to the ambient environment concludes the fabrication; further details are reported in the Supporting Information.

A top-view representation of the final device is shown in Figure 1c alongside with a magnified micrograph of the active region of the transistor, which highlights the fine alignment between the top gate electrode and the channel area. We confirmed such alignment, associated with a low capacitive parasitism, with cross-sectional SEM imaging of the device (Figure 1c), which allows to estimate the size of the geometrical overlap between electrodes in the range ≈ 0–250 nm (Figure S1, Supporting Information).

We measured the DC transfer (**Figure 2**a) and output characteristics (Figure S3, Supporting Information) of our transistors, verifying a correct operation up to a bias voltage of 40 V, with a maximum gate leakage current in the order of the nA, with respect to a channel current in the order of a few mA. This proves

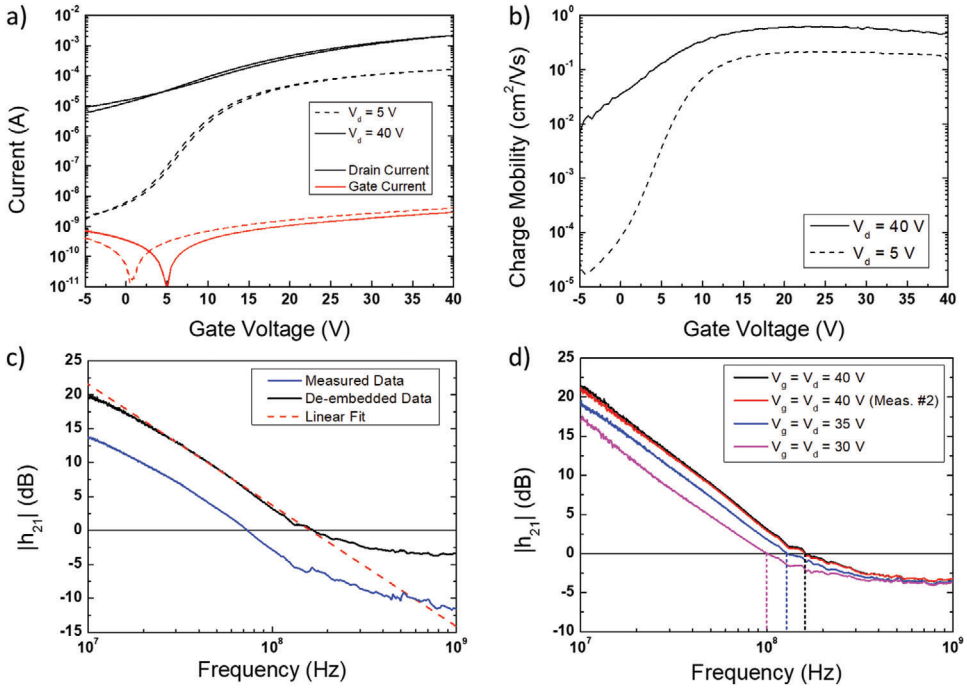

Figure 2. a) Measured transfer curve and b) apparent charge mobility for our high-frequency OFET. c) h_{21} for the same device, extracted from the S-parameter measurement at $V_g = V_d = 40$ V. d) Consecutive measurements of h_{21} for another, nominally identical device, at different bias voltages in the range 30 to 40 V (de-embedded data). No appreciable degradation effects are visible after two consecutive measurements at a bias of 40 V.

that laser processing on top of a multilayer stack of organic materials, including a semiconductor and a dielectric, is compatible with the fine patterning of high-resolution conductive electrodes without damage to the underlying materials.

We then highlight how the integration of a substrate with a high thermal conductivity in our process allows ideal DC operation of the device and prevents the thermal breakdown. In particular, in the case of OFETs with the same architecture and comparable fabrication process, realized on a glass substrate (which exhibits a lower thermal conductivity in the order of 1 Wm^{-1} K^{-1}), when the generated power per unit area approaches the range 20–30 W mm^{-2}, the devices start to suffer from thermal degradation, the current driven by the device saturates/drops with respect to the increase of the gate voltage and severe hysteresis appears in the transfer curve (Figure S4, Supporting Information). Contrarily, for the devices of this work, even at the bias point corresponding to the maximum generated power per unit area P_{th} (I_d = 2.18 mA, V_d = 40 V and P_{th} = 90 W mm^{-2}), correct operation of the device is preserved and no signs of thermal degradation are visible.

We calculated the apparent charge mobility of our devices in the linear (μ_{lin}) and saturation regimes (μ_{sat}) versus gate voltage (Figure 2b). The ideality of the DC operation of the transistors is confirmed by the flatness of the curves in the fully accumulated regime above 10 V, with a slight roll-off that can be attributed to some residual impact of the contact resistance. The maximum values for the apparent charge mobility are μ_{lin} = 0.22 cm^2 V^{-1} s^{-1} and μ_{sat} = 0.62 cm^2 V^{-1} s^{-1}. We extracted the width-normalized contact resistance $R_c W$ and the intrinsic charge mobility μ_i of our devices, which we estimate to be $R_c W$ = 300 Ω cm and μ_i = 1 cm^2 V^{-1} s^{-1} in the saturation regime at a bias point of $V_g = V_d$ = 40 V (see Supporting Information for details). Such a value of R_c is not only a key requirement in order to access frequency regimes in excess of 100 MHz,[15,19] but is among the best reported values for OFETs in general and is extremely low when considering the case of transistors realized via direct-writing, solution-based methods and optimized for low geometrical overlap of electrodes and high-frequency operation.[37–39]

We then measured the AC characteristics of our device by means of S-parameters, using a setup already described in our previous work,[27] calibrated with a Short-Open-Load-Through (SOLT) procedure and corrected with a 12-term error model. From the measured S-parameters, the parasitic contributions of the pads and interconnections are de-embedded from the measurement with a one-step procedure[40] and the hybrid parameter h_{21} is extracted (Figure 2c), allowing to identify f_t according to h_{21} (f_t) = 0 dB, which yields an unprecedented f_t of 160 MHz at a bias voltage of 40 V for OFETs in the case of the best device (Figure 2c, linear fit). In terms of the voltage-normalized transition frequency f_t/V, we reached a figure as high as 4 MHz V^{-1}, also in this case the highest value reported for an OFET. Such extracted f_t performance is robust with respect to thermal degradation effects: measurements on a nominally identical device results in a practically identical f_t of 158 MHz, which remains stable after a second, consecutive measurement of h_{21} at V_g = 40 V (Figure 2d, black and red lines) and after further measurements at gate biases of 35 and 30 V (Figure 2d, blue and purple lines).

As a crosscheck of the consistency of the AC performance, we extracted the values for the gate/drain and gate/source capacitances C_{gd} and C_{gs} for $V_g = V_d$ = 40 V, alongside with the total gate capacitance $C_g = C_{gd} + C_{gs}$ (Figure S5, Supporting Information). The total gate capacitance, at first order, can be estimated

as follows:

$$C_g \cong C_{diel} W \left(\frac{2}{3} L + 2L_{ov} + 2d \right) \quad (1)$$

where L_{ov} is the geometrical overlap between gate and source (or drain) electrode and $2d$, for low-overlap structures of the kind presented here, accounts for the contribution of the fringing field in the form of an "equivalent overlap length", equal to the thickness of the dielectric d.[15]

According to this formula, and with L_{ov} in the range 0–250 nm, the total gate capacitance C_g can be estimated to be in the range 101–135 fF, which is in good agreement with the value extracted from our measurement (140–150 fF above 30 MHz, Figure S5, Supporting Information). The transconductance and output resistance can be estimated from the DC curves respectively as $g_m = \frac{dI_d}{dV_g}$ and $r_o = (\frac{dI_d}{dV_d})^{-1}$, evaluated at the transistor bias $V_g = V_d = 40$ V, yielding $g_m = 0.115$ mS and $r_o = 25.3$ kΩ. These values obtained from the DC characterization are in agreement with the S-parameters measurements ($g_m = 0.115$ mS and $r_o = 22$ kΩ at 10 MHz, Figure S6, Supporting Information). In addition, we verified that g_m is not altered by the de-embedding procedure, confirming the consistency of the obtained results (Figure S6, Supporting Information).

The measured f_t can be compared to the theoretical value estimated from the transistor DC electrical parameters and geometrical dimensions, according to:

$$f_t = \frac{g_m}{2\pi C_g} \quad (2)$$

With the range of values for C_g calculated above and with the range of values for g_m extracted from DC, the theoretical f_t is calculated to be in the range ≈ 140–180 MHz, which is consistent with our measured value. By including our additional analysis on the contact resistance (see Supporting Information), the measured f_t can also be related to the value predicted by more refined theoretical models in recent reports,[15,19] which include not only the effects of the fringing electric field for low-overlap structures (already accounted for by Equation (1)) but also the effects associated with charge injection physics in staggered OFETs with small electrode overlap. The application of such a model consistently returns, for the parameters of the transistors of this work, a predicted f_t in the range 138–146 MHz (see Supporting Information), which is not dissimilar to our measured result.

Overall, high-frequency operation at 160 MHz of solution-processed OFETs is demonstrated via an S-parameter measurement and further validated by the agreement of the extracted transistor small-signal AC parameters with the ones calculated through physical and geometrical considerations. This experimental demonstration agrees with and complements the theoretical roadmaps described in recent works.[15,19]

Contrarily to the widespread assumption that organic electronics is relegated to very low-frequency operation, we have shown here that organic FETs can operate at an f_t of 160 MHz and f_t/V of 4 MHz V^{-1}. This value of f_t is by far the highest reported for any organic transistor to date, while f_t/V is the best reported for organic transistors capable of sustaining continuous biasing (Table S1, Supporting Information). The significance of this achievement is further reinforced by the sole adoption of direct-writing and solution-based fabrication methods, which have traditionally complicated the achievement of high-performance figures of merit, as well as finely-controlled patterning of functional materials at the micron scale.

This result lays its foundations on three key aspects, which must be satisfied at the same time: i) a high patterning resolution to achieve micron-scale electrodes, ii) an efficient charge injection from the electrodes to the semiconductor to reduce contact resistance well below 1 kΩ cm, and iii) the suppression of thermal breakdown.

The OFET AC performance demonstrated in this work was achieved both by devising a set of strategies to overcome the bottlenecks to high-frequency operation and by combining them into a fabrication scheme solely using scalable techniques. First, the high patterning resolution necessary both to downscale the transistor dimensions and to contain the capacitive parasitism has been achieved by using laser sintering, which allowed the fine alignment of micron-sized electrodes via direct writing. Second, the charge injection from the contacts, which must be very efficient for downscaled architectures with low overlap between gate and bottom electrodes, has been promoted by inducing the self-assembly of an amine-based monolayer. This approach allowed to achieve width-normalized contact resistance $R_c W = 300$ Ω cm, which is among the best reported values for solution-processed, direct-written OFETs in general. This achievement is further reinforced by the fact that it is associated with an architecture optimized for high-frequency operation, whose low electrode overlap is well-known to be detrimental for charge injection. Third, thermal breakdown/degradation has been avoided by using an appropriate thermally-conductive substrate. The latter result highlights an unprecedented need for substrate materials for OFETs, combining flexibility and sufficient thermal conductivity, thus indicating a clear path to be further pursued in the future.[41–44]

In conclusion, we have demonstrated that high-frequency operation in excess of 100 MHz is accessible to organic-based electronics. The result we show here represents a suitable complement and validation to a set of recent reports that theoretically detailed a feasible roadmap towards high-frequency operation or organic transistors.[15,19] Within the roadmap detailed in such works, our achievement of an $R_c W$ of 300 Ωcm in high-frequency devices based on printed polymers constitutes one of the key enablers.

These achievements challenge the conventional, well-known tradeoff between the higher electrical performances of inorganic materials (e.g., silicon, metal-oxides, carbon nanotubes) with the advantageous mechanical properties and the cost- and energy-efficient processability of organics. Our findings, overall, outline a credible route towards the adoption of organics in an expanded set of applications, including remote healthcare, distributed sensing, design and entertainment, requiring the availability of a technology integrating large-area electronics with wireless-communication capabilities, realized via cost- and energy-efficient production schemes.

Experimental Section

For the experimental section, please refer to the Supporting Information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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