Variability Effects in Nanowire and Macaroni MOSFETs – Part I: Random Dopant Fluctuations

Alessandro S. Spinelli, *Senior Member, IEEE,*
Christian Monzio Compagnoni, *Senior Member, IEEE,* and Andrea L. Lacaita, *Fellow, IEEE*

***Abstract*—In this paper and in the related Part II we investigate variability effects on the threshold voltage of nanowire and Macaroni MOSFETs, focusing on random dopant fluctuations (RDF) and random telegraph noise, to assess their dependences on device radius, channel length, and doping. In Part I we address threshold voltage fluctuations induced by RDF and show that different trends emerge with respect to planar devices, being dependent on whether the conduction is bulk- or surface-dominated. Macaroni devices with thin silicon regions can improve RDF, while moving from inversion- to accumulation-mode devices results in a worsening of this parameter.**

***Index Terms*—Nanowire MOSFET, Macaroni MOSFET, variability, random dopant fluctuations**

I. Introduction

THE unrelenting increase in integration density and performance of silicon chips calls for faster and less power-hungry devices with respect to conventional planar MOSFETs, which has led first to the exploitation of innovative materials within the conventional MOSFET architecture and later to the pursuit of radical changes in the device architecture itself. The latter step has resulted in the move toward three-dimensional (3D) devices, whose era was ushered by FinFETs [1], used in state-of-the-art microprocessors since 2012 [2], [3], and is now fully represented by the nanowire (NW) transistor [4], [5]. These devices exhibit significant advantages with respect to their planar counterpart (low power dissipation, mobility enhancement [6] and better short-channel effects [7]), in spite of an increase in source-drain resistance [8], [9] and lower flexibility in the on-state current tailoring.

A related field in which the transition to 3D devices has occurred is the non-volatile NAND Flash memory one. NAND Flash have long become a main technology driver, and experienced the scaling limitations of the MOS technology even before logic transistors, because of their tighter reliability requirements [10] and related constraints to gate oxide scaling [11]. After reaching the 15 nm planar node around 2014, all major NAND manufacturers switched to 3D NAND based on vertical channel devices, now stacking up to 128 layers [12], [13]. The elementary cell is a hollow silicon NW transistor filled with dielectric material, sometimes referred to as a Macaroni MOSFET [14].

In both NW and Macaroni devices, variability at the atomic level plays a key role in limiting the performance. In particular, random dopant fluctuations (RDF) in NWs has been addressed by several studies [15]–[23], but a full analysis of the RDF dependence on device parameters has not been addressed so far. This is even more true when the work is extended to Macaroni devices, for which we have found no study. Such an investigation is worthwhile because RDF plays a non-negligible role [24] when compared to other variability sources such as metal grain granularity [25] and roughness in the gate and wire geometry [26]–[28]. Moreover, RDF can be regarded as an ultimate variability source, not related to the manufacturing technology.

Trap-related phenomena such as random telegraph noise (RTN) in NWs have been also investigated experimentally [29]–[32] and numerically [33], although in this case as well, little emphasis has been given to a statistical analysis of the RTN amplitude.

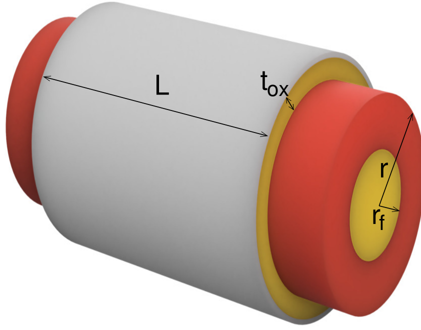
This work aims at presenting a comprehensive view of threshold voltage fluctuations induced by RDF and RTN in NW and Macaroni devices for logic and memory applications via 3D numerical simulations, highlighting major trends and pointing out the differences with the planar case. The study is broken down into two parts: Part I deals with RDF while Part II [34] discusses RTN, and is an extended version of what has been presented in [35], with a higher statistical set (i.e., a better accuracy in parameter extraction) and a wider range of investigated devices and conditions. Interpretation of results is also entirely new.

II. Simulation framework

We performed 3D numerical simulations of cylindrical NW and Macaroni devices as a function of different design parameters, using a commercial software [36]. A schematic of the device structure with relevant parameters and values is shown in Fig. 1. Since our aim was to describe devices for logic and memory applications, some trade-offs in the parameters had to be made. This is why the value of the gate oxide thickness $t_{ox} = 1$ nm is compatible with logic applications but completely unrealistic for non-volatile memories. On the other hand, some doping values and device structures might be regarded as not totally appropriate for the former. This however does not constitute a real problem when the relative trends are identified. For example, it has been already shown that a linear relationship holds between t_{ox} and device characteristics such as the rms value of the V_T distribution [19], [37].

The typical doping profile used in simulations is depicted in Fig. 2: discrete dopants (both donors and acceptors) are

The authors are with the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milan 20133, Italy (e-mail: alessandro.spinelli@polimi.it; christian.monzio@polimi.it; andrea.lacaita@polimi.it).



L	$20-40$ nm
t_{ox}	1 nm
r	$5-20$ nm
r_f	$5-15$ nm
N_A	$10^{17}-10^{19}$ cm^{-3}
N_D	10^{18} cm^{-3}

Fig. 1. Schematic of the Macaroni device structure (red = silicon; amber = oxide). Oxide was stripped over source/drain regions. Relevant device parameters and values are shown in the table.

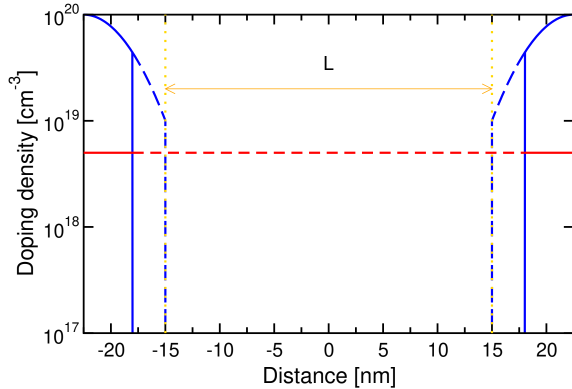


Fig. 2. Typical doping profile used in simulations. Solid lines show regions where a continuous doping profile was adopted. Dashes mark regions where atomistic doping was implemented.

considered in the silicon region extending for 3 nm per side beyond the gate edges (dashed lines), while a continuous doping (solid lines) was used in regions close to the source and drain contacts. Random dopant number and positions were drawn in a Monte Carlo (MC) fashion from a Poisson statistics having average value and spatial distribution given by the continuous profile [38]–[41]. No source/drain dopant penetration below the gate was considered, in order to avoid channel length modulation by the channel dopants. Up to $5-10$ thousand devices were then simulated for each condition, employing a drift-diffusion approach with density-gradient corrections to account for quantum effects at the silicon-oxide interfaces and at the Coulomb wells. To focus on percolation and electrostatic effects, a low drain bias of 50 mV and a constant mobility $\mu_n = 100$ cm^{2}V^{-1}s^{-1} were also used. Following NAND operation, threshold voltage V_T

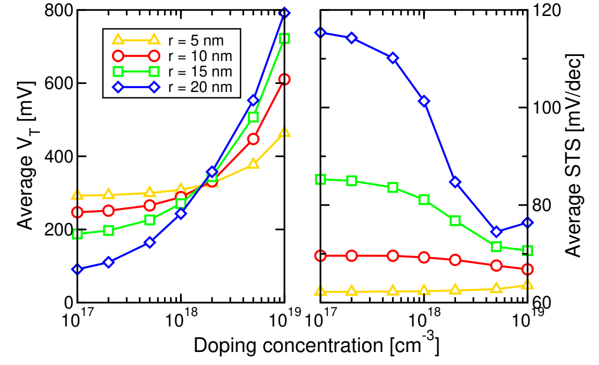


Fig. 3. Average V_T and STS as a function of doping, for different NW devices.

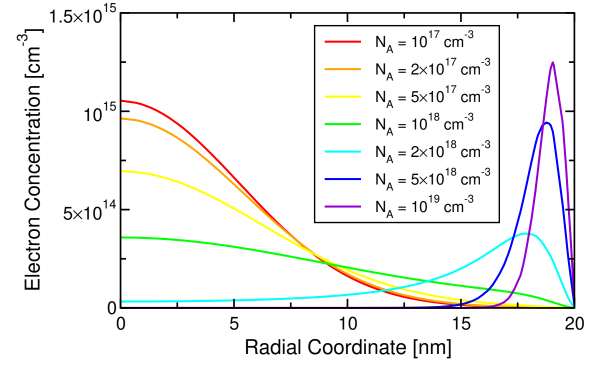


Fig. 4. Average radial electron concentration at threshold in the $r = 20$ nm NW device, for different values of N_A.

was extracted in the subthreshold region, according to

$$I(V_T) = K\frac{A}{L}, \quad (1)$$

where $K \approx 1.91 \times 10^{-7}$ A/μm is a constant, A the device area and L the gate length. Since the current is expected to be proportional to such quantities in the subthreshold regime [42], a radius- and length-independent V_T is expected.

III. NW Devices

A. Average Data

We begin our investigation of NW devices with a look at the average data for V_T ($\overline{V_T}$) and subthreshold slope STS as a function of doping and for different values of silicon radius r, reported in Fig. 3. While an increase of $\overline{V_T}$ with N_A is expected, a non-negligible dependence on r is also apparent, which is not straightforward, given that our definition of V_T should be r-independent. For low doping, $\overline{V_T}$ decreases for larger values of r due to short-channel effects, as indicated by the increase in STS. For high doping, however, an opposite trend arises.

To gain some insight into this result, we observed the average electron concentration at threshold in the $r = 20$ nm device, for different values of N_A (Fig. 4). Results make clear that the conduction is non-uniform over the area: the electron concentration crowds at the channel center for low dopings, where short-channel effects are more effective in lowering the

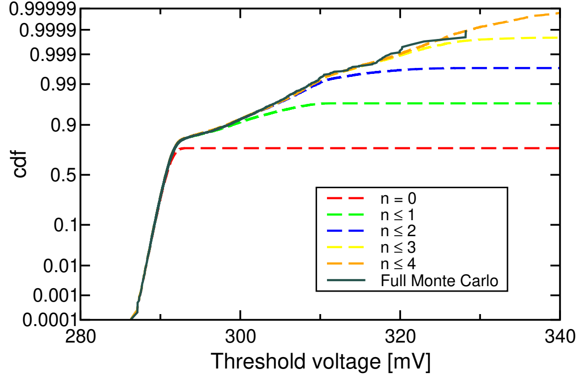


Fig. 5. V_T cdfs for the NW device with $r = 5$ nm and $N_A = 10^{17}$ cm^{-3}. Dashed lines show the cumulative probabilities of having 1, 2, 3,... atoms in the atomistic region.

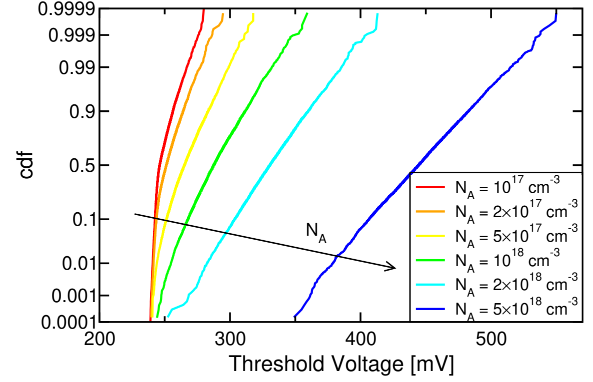


Fig. 6. V_T cdfs for the NW device with $r = 10$ nm, $L = 30$ nm for different channel doping densities N_A ranging from 10^{17} to 5×10^{18} cm^{-3}.

barrier, but shifts toward the edge of the area for high dopings, owing to the increased band bending determined by the depletion charge. In such a regime, which is similar to surface conduction in planar MOSFETs having width $W = 2\pi r$, the current is proportional to r and not to r^2, meaning that a higher $\overline{V_T}$ is needed to match the criterion set by (1). Note also that when electron conduction is indeed uniform over the device area (N_A somewhere between 10^{18} and 2×10^{18} cm^{-3}), V_T does not depend on r.

B. V_T Spread

We now shift our attention to the V_T spread induced by RDF and consider the cumulative distribution function (cdf) for V_T in the narrower device with $r = 5$ nm, at the lowest doping density investigated, $N_A = 10^{17}$ cm^{-3} (average number of acceptors in the atomistic region ≈ 0.28). MC results shown in Fig. 5 (grey curve) clearly feature a bimodal behavior made up of a low-V_T part with small dispersion and a tail with a much higher spread. To clarify this result, we can break down the V_T probability $p(V_T)$ using the conditional probability:

$$p(V_T) = \sum_n p(V_T|n)\ p(n), \qquad (2)$$

where $p(V_T|n)$ is the V_T distribution when n acceptor dopants are placed in the atomistic region and $p(n)$ is the Poisson probability of having such number of acceptors in the atomistic region. It is now sufficient to run simulations with a fixed number of acceptors to reconstruct $p(V_T)$, ganing an additional insight into the dopant contributions to the final cdf (note that (2) holds also for the cdf). Results obtained in this way are also shown in Fig. 5, where the dashed curves show the V_T cdf when 0 or up to 1, 2, 3 and so on dopants are considered. Note the good matching between the full MC results and this approach. Moreover, the (red dashed) curve related to $n = 0$ alone can be seen to fully reproduce the low-V_T tail of the MC cdf, suggesting that this part is due to those devices which happen to have zero acceptor atoms in the silicon region below the gate. In this case, the V_T fluctuation is given by RDF induced by donors located in the atomistic source/drain regions.

The high-V_T tail of the distribution is instead dictated by the devices with non-zero dopants below the gate. A first observation is that such a curve does not follow a pure Gaussian law (i.e., a straight line in the plot), but rather presents different slopes, corresponding to the different values of n. Such a shape of the V_T distribution complicates somewhat the extraction of a single rms value for V_T, σ_{V_T}. Because of its usefulness, however, in the following we will fit the entire tail region with a single Gaussian distribution to extract σ_{V_T}, neglecting the inaccuracies resulting from the slope variations. It is worth pointing out that different distributions have been proposed for V_T [23], [43], but the differences with respect to a simpler Gaussian become apparent only for much larger statistics.

We have then investigated the doping dependence of the V_T cdf. Results are reported in Fig. 6 for NWs with $r = 10$ nm and channel doping N_A ranging from 10^{17} to 5×10^{18} cm^{-3}. Note that the spread of V_T increases as doping is raised, which is an expected trend, as the greater number of percolation centers means more variability in the conduction. For high dopings, moreover, a single Gaussian behavior is recovered, as the probability of having no dopant vanishes. Note also the small shift toward higher V_Ts in the zero-dopant limit as N_A increases: this is related to the increased resistivity of the source/drain regions due to counter-doping by the acceptors.

Fig. 7 shows σ_{V_T} as a function of the channel doping for NWs having $r = 5, 10, 15$ and 20 nm. To make full sense of the results, we begin with the narrower devices, with $r = 5$ and 10 nm. Here, σ_{V_T} follows a power law $N_A^{0.3}$. A similar dependence, but with a stronger exponent equal to 0.4, has been already reported for planar devices and explained in terms of electron percolation through the ionized acceptors [37]. We believe that both the 3D nature of electron conduction and the fully depleted nature of these devices could account for such a difference. Also worth mentioning is the fact that our dependence is different from what reported in [44], a factor that may be ascribed to the much lower doping values there investigated, with the uncertainties in the extraction of the variance already discussed. A similar dependence in the investigated doping range has been reported by [23]. The variability contribution given by source/drain dopants only is smaller than 3 mV and does not affect the result.

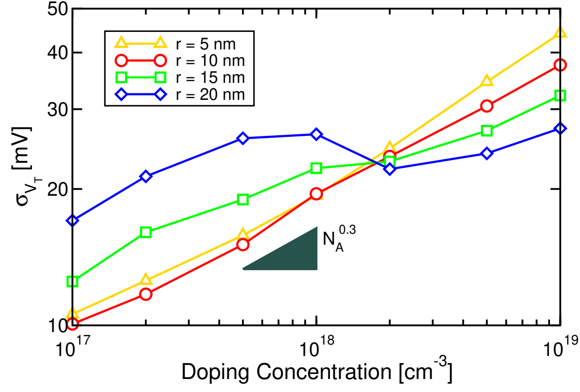


Fig. 7. V_T rms value σ_{V_T} as a function of N_A for different NW devices having $L = 30$ nm.

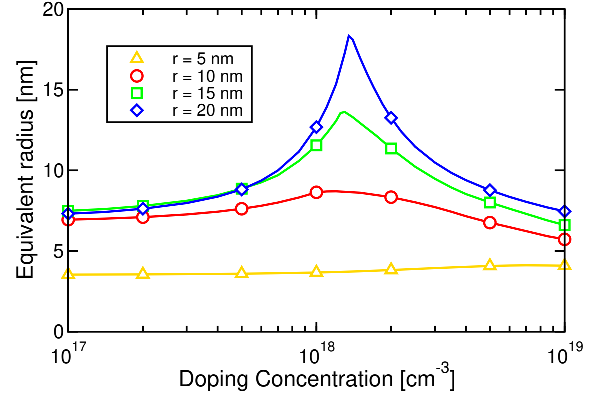


Fig. 9. Equivalent radius of the investigated device. Additional simulations were conducted to obtain the reported curves.

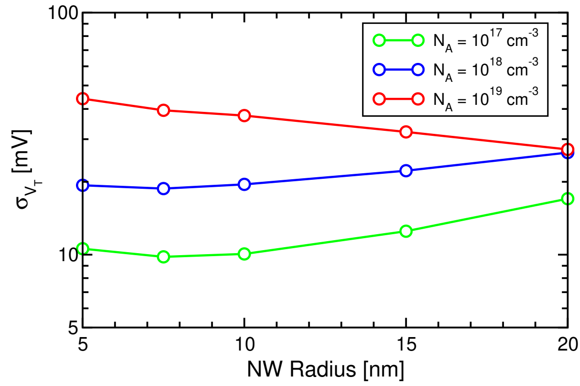


Fig. 8. V_T rms value σ_{V_T} as a function of r for different NW devices having $N_A = 10^{17}$, 10^{18} and 10^{19} cm^{-3}.

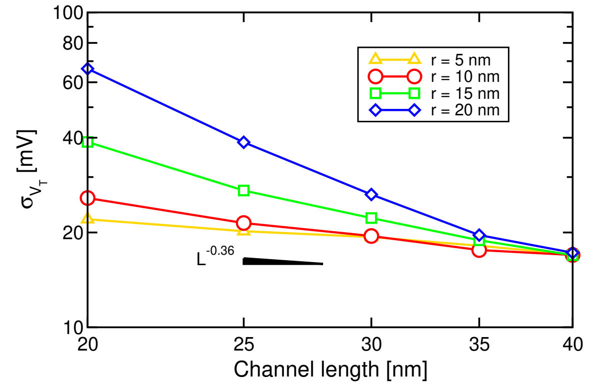


Fig. 10. σ_{V_T} as a function of L for NW devices having $N_A = 10^{18}$ cm^{-3}.

We now consider the more complex behavior featured by the wider NW devices and notice that the roll-off of the $r = 20$ nm device from the $N_A^{0.3}$ power law takes place at the very same doping levels at which the electron distribution changes from bulk to surface (see Fig. 4). This suggests that not-too-narrow NW devices should be regarded as 3D bulk devices for low dopings only (where σ_{V_T} follows the $N_A^{0.3}$ power law), and as 2D (i.e., planar-like) devices for high dopings. In the latter regime, σ_{V_T} decreases with r, in analogy with its decrease with W in planar devices [37]. The reported data for σ_{V_T} remain unaffected (except for a few percent) even if a lognormal distribution is used to fit the data.

The dependence on r is explicitely reported in Fig. 8, for three doping levels: for high doping, σ_{V_T} decreases in larger devices as already discussed. However, the dependence can be approximated by an $r^{-0.34}$ law, which is milder with respect to the $r^{-0.5}$ trend expected for a planar-like device [37].

The σ_{V_T} trend with r for low dopings is a bit subtler: in principle, a decrease in larger devices might be expected even for bulk conduction, but the picture here is complicated by the non-uniform conduction over the area set by short-channel effects (see Fig. 4). To address the issue, we computed an *equivalent radius* r_{eq} of the average radial electron distribution n as

$$\pi r_{eq}^2 n_{max} = 2\pi \int_0^r x n(x) dx, \quad (3)$$

where n_{max} is the peak electron concentration. Results are shown in Fig. 9 (additional simulations were run to construct the curves): going from the 5 to the 10 nm NW for $N_A = 10^{17}$ cm^{-3} results in an increase of both the number of percolation centers (raising σ_{V_T}) and of r_{eq} (i.e., of the percolation area, lowering σ_{V_T}). This results in a very small dependence of σ_{V_T} on r. If we further increase r, however, the area occupied by the electrons does not increase, because of short-channel effects. This explains the higher σ_{V_T} in the $r = 15$ and 20 nm NWs. At $N_A = 10^{18}$ cm^{-3}, r_{eq} has increased in larger devices (see also Fig. 4), percolation is eased and σ_{V_T} flattens even more. Eventually, n is pushed toward the interface, r_{eq} drops, and we fall into a 2D-like behavior.

This analysis can help to explain the dependence on L, with reference to NWs with $N_A = 10^{18}$ cm^{-3}. Results in Fig. 10 confirm that σ_{V_T} decreases in longer-channel devices, in analogy with planar structures. Note again that similar values are obtained for $r = 5$ and 10 nm, that follow approximately an $L^{-0.36}$ dependence. Larger devices, instead, depart from this trend as L decreases, short-channel effects gain importance

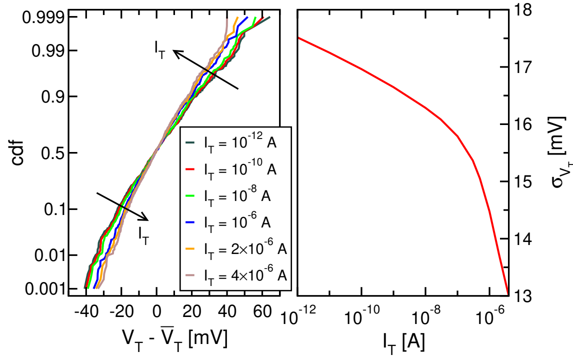


Fig. 11. Left: V_T cdf for different threshold currents I_t for the NW device with $r = 10$ nm and $N_A = 10^{18}$ cm^{-3}. Right: σ_{V_T} as a function of I_T for the same device.

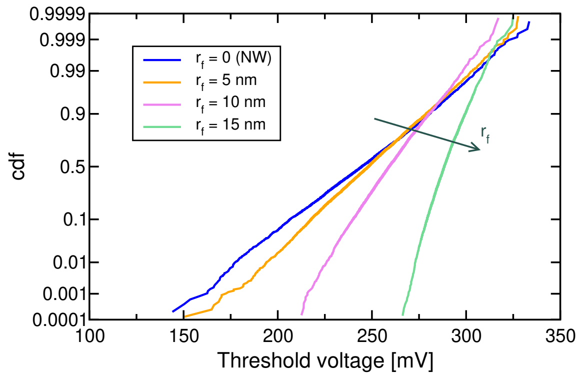


Fig. 12. V_T cdfs for Macaroni devices having $r = 20$ nm and $N_A = 10^{18}$ cm^{-3}.

and r_{eq} decreases. As a reference, the $r = 20$ nm NW follows an $L^{-2.17}$ dependence for $L \leq 35$ nm.

Finally, we looked at the dependence of RDF on the current level used for the extraction of V_T, reported in Fig. 11 for the 10 nm NW with $N_A = 10^{18}$ cm^{-3} (for better comprehension, the cdfs are plotted versus the difference from the average V_T). Note that σ_{V_T} decreases as the threshold current is raised [19], because of the decrease of the screening length of the ionized dopants. Such a dependence is relatively small below threshold, but increases as the on state is approached. In this latter regime, however, the impact of mobility becomes more relevant and the results should be validated with a fuller model.

IV. Macaroni devices

In the 3D Flash memory field, Macaroni devices rather than NWs are employed, because of the better electrostatic control and tighter V_T and STS distributions [14], [45], [46]. These structures are basically hollow NWs, in which conduction takes place in the annular region around a central zone filled with a dielectric, called *filler*. We have therefore investigated the extent of RDF in such devices taking as a reference an outer radius of the silicon channel $r = 20$ nm, for $N_A = 10^{18}$ cm^{-3} and $L = 30$ nm. Fig. 12 shows the results for the V_T cdf when the filler radius r_f is $5, 10$ and 15 nm, together with the NW data ($r_f = 0$). Clearly, the

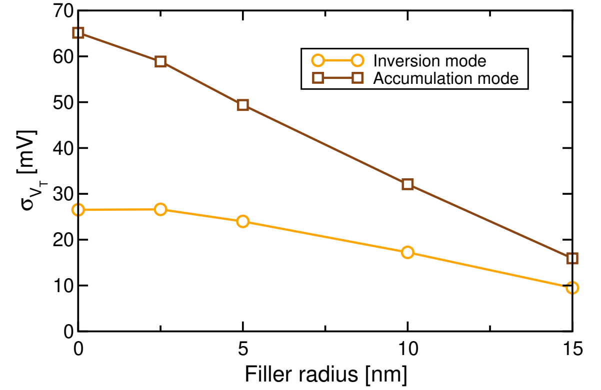


Fig. 13. σ_{V_T} as a function of the filler radius in inversion- and accumulation-mode Macaroni devices having $r = 20$ nm and $N_A = 10^{18}$ cm^{-3}.

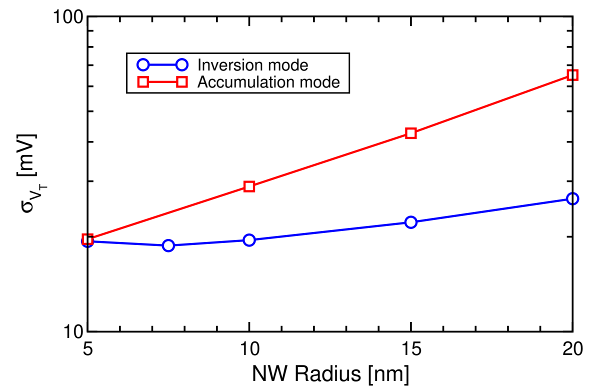


Fig. 14. σ_{V_T} as a function of r for inversion- and accumulation-mode NW devices having doping density of 10^{18} cm^{-3}.

V_T distribution becomes tighter as the silicon region narrows, which constitutes another advantage of devices with a thin silicon region. Actual values of σ_{V_T} are reported in Fig. 13 (orange curve): note that its value is weakly affected for small values of r_f and starts decreasing when r_f approaches $r/2$. The behavior is again related to the better electrostatic control exerted by the gate for larger values of r_f.

V. Accumulation-mode devices

Junctionless NW and Macaroni devices working in accumulation mode have long been proposed for logic devices [47], [48] and for the cell strings of 3D NAND Flash [49], simplifying the manufacturing process. As a final step of our analysis, we investigate the RDF impact on such devices. To this aim, we considered the $L = 30$ nm case where an atomistic donor doping at $N_D = 10^{18}$ cm^{-3} is used in place of the acceptor doping adopted until now. Source/drain region doping was left unaffected.

Fig. 14 shows results for σ_{V_T} extracted for NWs working in accumulation ($N_D = 10^{18}$ cm^{-3}) or inversion mode ($N_A = 10^{18}$ cm^{-3}). Clearly, accumulation-mode NWs suffer from a worse RDF effect with respect to their inversion-mode counterpart, as pointed out by [23], [50]. This can be explained by the same framework used to interpret the previous results: accumulation-mode NWs have worse short-channel effects

with respect to inversion-mode ones (the STS for the 20-nm devices are about 101 mV/dec when operated in inversion mode and 124 mV/dec in accumulation mode), meaning that the charge is more crowded toward the channel center (i.e., r_{eq} is smaller), leading to a larger σ_{V_T}. This also explains why data for the narrower devices, where $r_{eq} \approx r$, are the same for both regimes. The latter data appear in agreement with what reported in [51], though the device geometry and doping are not exactly coincident.

Data for Macaroni devices are reported in Fig. 13. Even in this case, the accumulation mode results in a worse RDF with respect to the inversion one, with the two merging for thin silicon regions, where the nature of the channel doping becomes insignificant.

VI. Conclusions

We have investigated the effect of RDF on the V_T variability in NW and Macaroni devices, via 3D numerical simulations. Results differ depending on whether electron conduction takes place in the bulk or at the device surface. In the former regime, attainable for low and medium doping or in thin devices, σ_{V_T} follows different laws with respect to the the planar case. Macaroni are shown to demonstrate lower variability with regard to NWs, while accumulation-mode devices exhibit worse performance than inversion-mode ones.

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