



## Article

# Fault-Tolerant Multiport Converter for Hybrid Distribution Systems: Configuration, Control Principles and Fault Analysis

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**Abstract:** Multiport converters (MCs) are widely adopted in many applications, from renewable energy sources and storage integration to automotive applications and distribution systems. They are used in order to interface different energy sources, storage devices and loads with one single, simple converter topology in contrast to the traditional approach, which can require different solutions made by two-port converters. MCs allow for a reduction in the number of components and cascaded conversion stages with respect to an equivalent system of two-port converters, resulting in reduced complexity, dimensions and costs, as well as in improved reliability and enhanced efficiency. Nevertheless, some aspects related to the design of MCs are still worth further discussion when MCs are applied to hybrid AC/DC distribution systems. First, most converters are developed for one specific application and are not modular in structure. Furthermore, many of the proposed solutions are not equally suitable for AC and DC applications and they can introduce significant issues in hybrid distribution systems, with earthing management being particularly critical. Even though most available solutions offer satisfying steady-state and dynamic performances, fault behavior is often not considered and the possibility of maintaining controllability during faults is overlooked. Building on these three aspects, in this paper, a new MC for hybrid distribution systems is presented. An innovative circuit topology integrating three-phase AC ports and three-wire DC ports and characterized by a unique connection between the AC neutral wire and the DC midpoint neutral wire is presented. Its control principles and properties during external faults are highlighted, and extensive numerical simulations support the presented discussion.

**Keywords:** multiport converters; AC/DC converters; DC/DC converters; distributed generation; storage devices; sliding mode control; fault analysis



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## 1. Introduction

The ongoing changes in distribution systems are creating new interest in innovative solutions to enhance system performance. In particular, hybrid AC/DC distribution systems are a promising solution for obtaining high performance in terms of dynamic stability, voltage quality and reliability; in this context, multiport converters (MCs) are considered with particular attention, in particular when an integrated electronic transformer can be adopted [1–23]. Indeed, these converters are particularly useful when it is necessary to interface different energy sources, storage devices, and loads with one integrated topology [5,7,10,13–15,18], while the traditional approach would require many two-port converters. For this task, MCs allow for a reduction in the number of components and cascaded conversion stages with respect to an equivalent system of two-port converters, resulting in reduced complexity, dimensions, and costs as well as improved reliability and enhanced efficiency [5,12–20,24]. MC centralized control allows for better system dynamics and higher power quality and continuity [5–12,20,25]. As all necessary communication

channels can be embedded in the converter itself, the control effectiveness does not depend on communication infrastructures to achieve efficient coordination among the different ports. Furthermore, it can be easily integrated in advanced grid management, including hierarchical control structures [26–28]. The wide interest in MCs is proven by a significant amount of research work available in the literature covering a wide range of applications, from renewable energy sources, distributed generation, storage device integration, and distribution systems [5,6,12,14,18–21,24,29–31] as well as automotive [13,15,32–34] and even high-voltage power systems [35–37]. As a consequence, MCs are identified as the ideal building block for high-performance distribution systems due to their properties in terms of controllability both under normal and fault conditions.

Two main categories of MCs can be recognized based on their circuit topologies: MCs based on a capacitive internal bus [5–11] and MCs based on an inductive internal bus [11–23]. Considering that the DC coupling can be realized by means of a high-frequency transformer, the second category is then split into three sub-categories: isolated MCs [12,13,18,19], non-isolated MCs [21–23], and MCs with a mix of isolated and non-isolated ports [14–16,20]. Furthermore, considering the wide range of possible applications, some MCs exhibit modular topologies [5–11,21–23], while others are designed with a specific number of ports and are not easily expandable [12–20]. From the control point of view, most MC controls are based on voltage-modulation techniques, often based on commutation phase-shift control [12–20], which is the standard for isolated converters comprising a high-frequency transformer. Some other studies, on the contrary, base their control algorithms on mean value quantities [5–7,21–23], manipulating the duty cycle through suitable current and voltage loops. However, few papers consider converter behavior and control under external or internal fault conditions [7,10,11,23,25].

When considering the application of MCs to low-voltage DC (LVDC) distribution systems, the following three issues should be examined and discussed in detail: modularity; the state of active and exposed conductive parts with respect to earth; and controllability under fault conditions.

A modular architecture is of high importance in distribution system applications; however, this issue is often overlooked in general designs for MCs. As an example, in [21] a family of converters based on an inductive link is discussed, which provided significant advantages in efficiency and in avoiding bulky capacitors; however, it was pointed out that it was not easy to extend the number of ports. In order to overcome such a limitation, a first study was presented in [10,11], where different topologies were compared and evaluated considering components, control algorithms, and fault behaviors for a possible application to LVDC systems.

The management of the state of active parts towards earth can be a critical issue for LVDC systems. In fact, when MCs and electronic power converters in general are used to interface two systems, whether they are both AC, both DC, or one AC and the other DC, a discontinuity in the state of active parts toward earth is introduced (e.g., the AC neutral wire and/or the DC middle point are interrupted). This issue, along with its effects on the management of the state of active parts towards earth, requires further discussion. Additionally, high-frequency common-mode disturbances and earth currents, both during standard operation and under fault conditions, cannot be addressed considering the AC and DC parts separately, as was highlighted in [37–40]. Some papers propose to introduce metallic isolation by mean of specific converters [41,42], which usually helps to avoid unnecessary disturbances while allowing for correct earthing management. However, this approach exhibits two major drawbacks: on the one hand, it requires many earthing policies, in that each section of the distribution system is isolated from the others. On the other hand, it requires unnecessary cascaded conversion stages, which increases power losses and system complexity, with these issues also driving interest towards MCs.

In addition, the controllability of the converter currents under external fault condition is of great importance for protection design and for their integration with the converter control algorithm. While a certain number of papers consider the eventuality of a fault

on the DC side of VSCs, both in high- [43–45] and low-voltage [46–48] applications, and provide extensive analysis of fault currents and converter behavior in fault conditions, the concept of fault current control is still not completely developed. Some papers introduce converter topologies and controls designed to be tolerant to DC-side faults on VSCs, both for high- [49–54] or low-voltage [7,23] applications, or devices capable of limiting short-circuit currents [55–58]. However, these approaches, even if effective, do not directly include fault management in converter control algorithms, limiting converter effectiveness in these regards.

In order to overcome all of the aforementioned issues, a new MC topology for hybrid distribution systems is introduced in this paper. In particular, two main contributions for MC applications are introduced in this paper. First, a new modular MC topology is presented in detail; its control principles, based on a direct current-tracking approach (for higher dynamic performances) are discussed; and an innovative control structure based on two control layers is proposed. Second, to overcome the lack of effective DC circuit breakers, which represents a traditional issue for DC systems, the proposed control approach was developed with particular attention to current controllability during faults, resulting in converters tolerant with respect to external faults, which can be integrated into the system's protection [25]. A set of numerical simulations is presented to support the presented discussion, including MC operation in steady-state conditions, under abrupt load/generation variations, and in the case of pole-to-pole faults on a port in order to highlight the strengths of the proposed MC topology and control. The presented results demonstrate that the proposed MC converter and its control algorithms can effectively manage different loads, providing a high-quality power supply not affected by abrupt load variations or faults on other ports. Additionally, the proposed MC was shown to behave as a fault-tolerant power hub that can be integrated into hybrid distribution system protection algorithms without the traditional limitations of power converters that may suffer damage from grid faults.

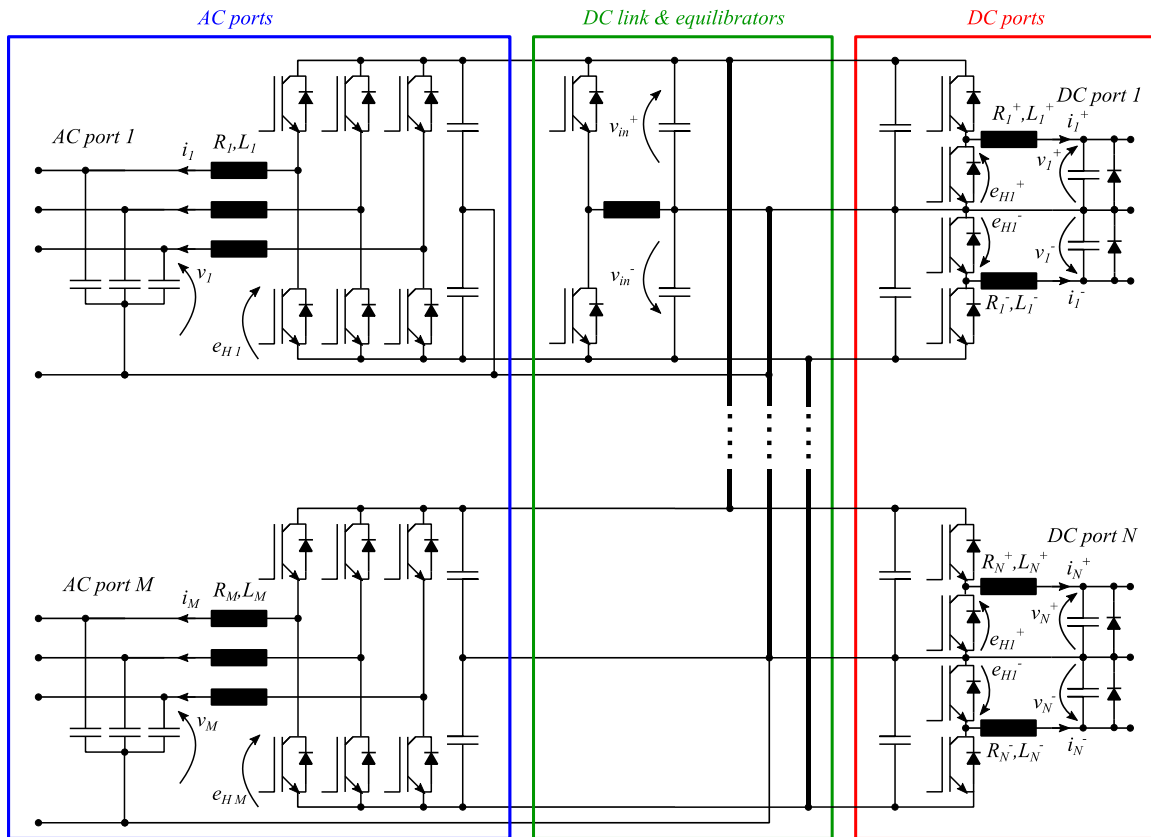
The rest of the paper is structured as follows: Section 2 presents the proposed configuration, along with some preliminary considerations of its topology and control principles. Section 3 presents a detailed discussion on the proposed control design, while the proposed converter fault sensitivity is discussed in Section 4. Section 5 presents the results of a set of numerical simulations aimed at validating the proposed control design. Lastly, final conclusions are drawn in Section 6.

## 2. Innovative MC Configuration

The proposed MC topology is based on an extension of the converter based on a capacitive internal DC link presented in [5] and further discussed in [11], taking advantage of the enhanced controllability and fault-insensitivity properties of this family of converters. The development of the innovative MC configuration presented here is driven by the rationale of providing a symmetrical structure with a common reference for AC and DC line voltages, thus unifying the AC neutral and DC middle point wires. This is a very significant feature for fault analysis and protection design, as the presence of a common neutral/midpoint wire keeps the fault response consistent among AC and DC ports, which is not the case with standard power converters, nor is it the case with the MC discussed in [5,11]. Thank to this solution, it is possible to have both AC and DC earthing with no functional problems; in addition, for each port, a low-impedance (virtually zero) reclosing path for common-mode currents is present, such that the issues related to common-mode (CM) disturbances discussed in [37–40] are strongly mitigated.

The proposed MC structure is shown in Figure 1, in general form, including M four-wire AC ports, an internal DC link with an arbitrary number of equilibrators, and N three-wire DC ports. The M four-wire AC ports can be used, indifferently, to connect the MC to an AC source, such as the public AC distribution network, or to fed AC loads. In the latter case, improved reliability can be obtained by integrating storage devices in the MC, realizing UPS functionality. The equilibrators maintain voltage balance between the

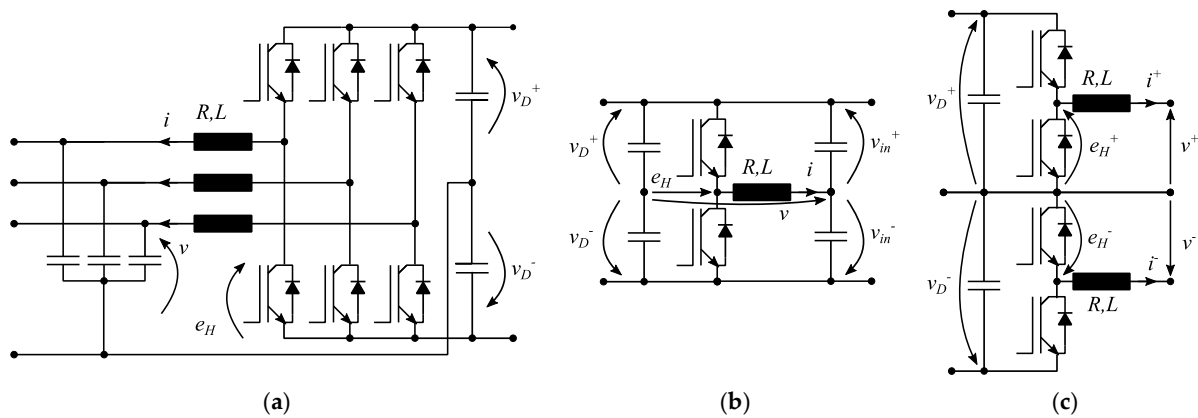
positive and negative internal DC busbars. Their function is not related to any particular port, hence their locations are purely arbitrary, and their number is defined on the basis of the expected level of unbalance in DC loads. Lastly, the three-wire DC ports have a two-fold scope: first, they allow for the distribution of two voltage levels, which provides greater flexibility for DC loads; second, the distributed neutral wire allows for unified earthing management among AC and DC ports. Moreover, analogous to its two-wire counterpart discussed in [11], the diodes are connected in parallel to the DC port capacitor to prevent the transitory negative voltages that can lead to capacitor damage and a loss of controllability [25].



**Figure 1.** Three-wire, capacitive-coupled MC topology.

Thanks to the proposed MC topology here proposed, only three module types are needed, as follows:

1. four-wire AC port module, represented in Figure 2a, including two semiconductors, each required to withstand the full DC link voltage;
2. equilibrator module, represented in Figure 2b, including two semiconductors, each required to withstand the full DC link voltage;
3. three-wire DC port module, represented in Figure 2c, including four semiconductors, each required to withstand one half of the DC link voltage.



**Figure 2.** Modules for: AC ports (a); equilibrators (b); and DC ports (c).

As a result, the circuit topology presented in Figure 1 is completely modular, allowing for flexible operation in the ever-changing modern distribution systems.

From a design perspective, since the maximum voltage that DC ports need to withstand is equal to one half of the maximum voltage that AC ports and equilibrators need to withstand, it seems unwise to use equal power electronic building blocks (PEBBs) for all ports. Indeed, due to circuit similarities between the proposed DC port structure and three-level, neutral-point-clamped (NPC) inverter legs, introducing three-level NPC AC ports and equilibrators may be a promising solution to further improve performance and modularity. Nevertheless, the advantages possibly granted by this solution rely on sizing and economic issues, which fall outside the scope of this paper.

From a control perspective, analogous to the control design reported in [11], the overall MC control discussed in detail in the following section comprises two layers: the lower one is constituted by the pseudo-sliding mode modulation of PEBB currents, while the higher control layer, based on an inverse dynamic approach, provides suitable current references for the lower one. This control design approach takes advantage of the stability and robustness properties of sliding mode controllers, the effectiveness of which, in power converter control, is well-known in the literature [59,60]. Additionally, the inverse dynamic technique used for the control higher level, ascribable to the feedback linearization family [61,62] and widely applied in robot manipulator control [63], provides the basis for the design of a suitable sliding manifold and avoids the need for a higher-order sliding mode controller. This general, layered control approach allows for the development of a totally modular control structure, with no need for predetermined port functionalities or a number of ports.

### 3. Two-Level Control Design

#### 3.1. Lower-Level Pseudo-Sliding Mode Control

The lower-level, pseudo-sliding mode control presented in the following is developed analogously to [11], where this control technique was selected for its superior dynamic performance, robustness, and simplicity. Consider the configuration reported in Figure 2a first and refer to the same figure for symbols. The sliding function (inductance flux error)  $\lambda$  can be defined according to:

$$\lambda = L(i - i^*). \quad (1)$$

Let  $f_{sw}$  be the switching frequency and, consequently,  $T_{sw} = 1/f_{sw}$  be the designed switching period. In addition, assume, as is common for power converter sliding mode control design, that: (a)  $v_D^+ > 0$  and  $v_D^- < 0$ ; (b) negligible resistive terms on high-frequency ripple ( $R \ll 2\pi f_{sw}L$ ); and (c)  $v_D^+$  and  $v_D^-$ ,  $v$  and  $i^*$  being suitable, Lipschitz-continuous functions with spectra are limited to frequencies much lower than the switching frequency  $f_{sw}$ .

Referring to Figure 2a and considering the inductor constitutive equation, the relation between the sliding function  $\lambda$  and the ideal switched voltage  $e_H$  is then formulated as:

$$\frac{d\lambda}{dt} = e_H - u_{eq}, \quad (2)$$

where the ideal switched voltage  $e_H$  possible instantaneous values are  $v_D^+$  and  $v_D^-$ . The equivalent voltage is expressed according to:

$$u_{eq} = v + L \frac{di^*}{dt} + Ri^*. \quad (3)$$

and represents the equivalent voltage, defined as the ideal continuous value of the discontinuous control variable  $e_H$  necessary to perform the desired control action [64], equal to the mean value of the switched voltage  $e_H$  in a sliding condition.

The controllability condition under which a sliding mode can be enforced is determined by considering that, to maintain sliding condition, it is necessary to be able to enforce a positive and negative derivative (2) on the sliding function  $\lambda$ , which results in:

$$v_D^- < u_{eq} < v_D^+. \quad (4)$$

The modulation algorithm used to enforce a sliding mode is based on a dynamic set of slanted thresholds [64], conceived to enforce a sliding mode with a fixed converter switching frequency. This is obtained considering a set of equally spaced time intervals  $T_k$ , such that:

$$T_{k+1} = T_k + \frac{T_{sw}}{2}. \quad (5)$$

In each time interval  $t \in [T_{k-1}, T_{k+1}]$ , the resulting control law is

$$e_H = \begin{cases} v_D^+ & \text{if } \lambda < (v_D^+ - u_{eq})(t - T_k) \\ v_D^- & \text{if } \lambda > (v_D^- - u_{eq})(t - T_k) \end{cases}, \quad (6)$$

which realizes the system of slanted thresholds proposed in [64].

Considering now the DC port configuration reported in Figure 2b, and referring to the same figure for symbols, proceeding analogously, the sliding functions (inductance flux error)  $\lambda^+$ ,  $\lambda^-$  can be defined as

$$\lambda^+ = L(i^+ - i^{+*}), \quad \lambda^- = L(i^- - i^{-*}), \quad (7)$$

and the relation between the sliding functions  $\lambda^+$ ,  $\lambda^-$  and the ideal switched voltage  $e_H^+$ ,  $e_H^-$  is formulated as

$$\frac{d\lambda^+}{dt} = e_H^+ - u_{eq}^+, \quad \frac{d\lambda^-}{dt} = e_H^- - u_{eq}^-. \quad (8)$$

The ideal switched voltage  $e_H^+$  possible instantaneous values are 0 and  $v_D^+$ , while the ideal switched voltage  $e_H^-$  possible instantaneous values are 0 and  $v_D^-$ . The equivalent voltages are expressed according to:

$$u_{eq}^+ = v^+ + L \frac{di^{+*}}{dt} + Ri^{+*}, \quad u_{eq}^- = v^- + L \frac{di^{-*}}{dt} + Ri^{-*}. \quad (9)$$

Consequently, controllability conditions, separately for each half of the module, result in

$$0 < u_{eq}^+ < v_D^+, \quad v_D^- < u_{eq}^- < 0, \quad (10)$$

and, in each time interval, the resulting control law is:

$$e_H^+ = \begin{cases} v_D^+ & \text{if } \lambda^+ < (v_D^+ - u_{eq}^+)(t - T_k) \\ 0 & \text{if } \lambda^+ > (-u_{eq}^+)(t - T_k) \end{cases}, \quad (11)$$

$$e_H^- = \begin{cases} 0 & \text{if } \lambda^- < (v_D^- - u_{eq}^-)(t - T_k) \\ v_D^- & \text{if } \lambda^- > (-u_{eq}^-)(t - T_k) \end{cases}.$$

### 3.2. Higher-Level Inverse Dynamic Control

The higher-level control is based on an inverse dynamic approach and relies on maintaining power balances to control internal and external voltages. For the sake of clarity, consider, with no loss of generality, an example case comprising  $N = 6$  ports, as shown in Figure 3, where port 1 is connected to an AC grid, which acts as an external power source; port 2 is connected to storage devices, which allows for high dynamic performance to be maintained regardless of grid dynamics, and realizes UPS functionality; port 3 is connected to an AC load; port 4 is connected to a PV source; ports 5 and 6 are connected to DC loads. Control-wise, the PV port is treated as a load since it requires a predetermined voltage obtained from an MPPT algorithm. Note that, due to the modular topology and control design concept, developing the control design for the present case study is a non-restrictive assumption, and it can be easily generalized to any number of ports. In particular, the control equations presented in the following enable the realization of voltage-controlled ports, power-controlled ports or current-controlled ports, covering all the functionalities usually required for distribution system applications and realizing a fully modular control layer where all ports performing the same functionality are controlled by the same control equation, while the centralized control is only required to manage the different power sources.

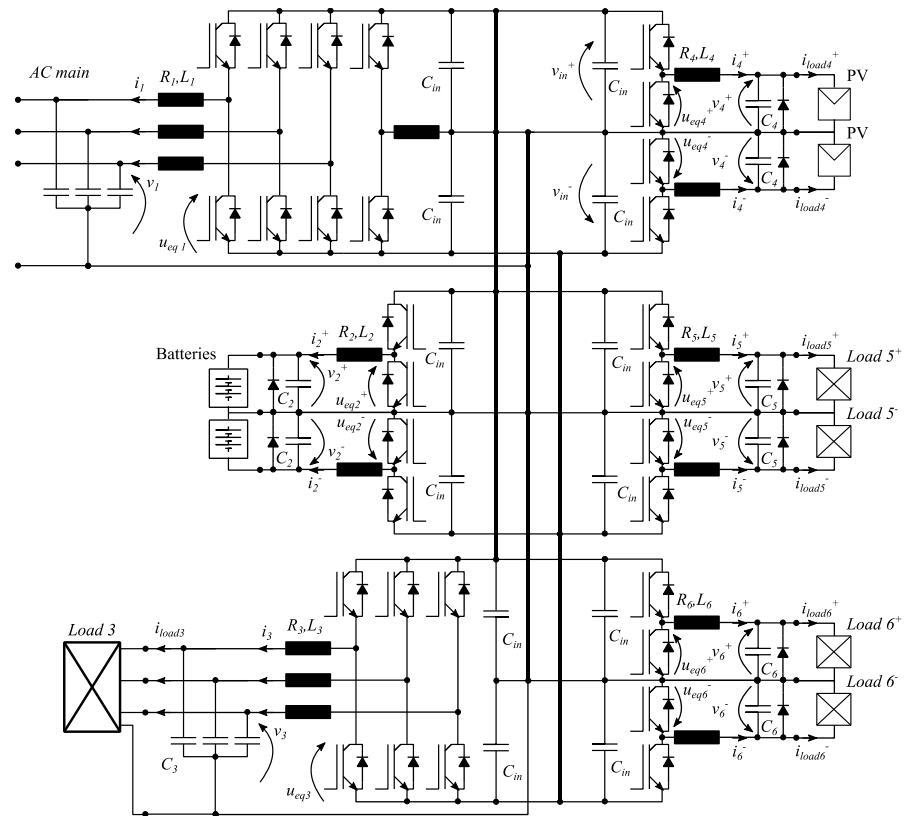


Figure 3. Three-wire, capacitive-coupled MC case study.

Let us consider voltage control first. Since the proposed MC is required to maintain the power balance among AC and DC ports, which may each have a different voltage level, the control is formulated in terms of port powers. Current references for the modulation algorithm are successively obtained as functions of reference powers and measured port voltages. Note that, as far as three-phase ports are concerned, the control equations are formulated in terms of a space vector for clarity and compactness; furthermore, in the following, the zero component is neglected, which implies that the converter produces balanced voltages. However, zero-component control can be realized with the same approach, if necessary.

According to the inverse dynamic control principles [63], let us define the voltage tracking error  $\varepsilon_i$  at the  $i$ -th port as:

$$\left. \begin{aligned} \varepsilon_i &= \mathbf{v}_i^* - \mathbf{v}_i & i &= 3, \\ \varepsilon_i^+ &= v_i^{+*} - v_i^+ \\ \varepsilon_i^- &= v_i^{-*} - v_i^- \end{aligned} \right\} i \in [4;6], \tag{12}$$

and the dynamic voltage error equation as:

$$\eta_i = f\left(\varepsilon_i, \int (\varepsilon_i)dt, \frac{d\varepsilon_i}{dt}, \dots, \frac{d^n \varepsilon_i}{dt^n}\right). \tag{13}$$

For each port, at capacitor terminals, the power balance can be formulated as:

$$\left. \begin{aligned} \mathbf{S}_i &= \frac{d}{dt} \left[ \frac{1}{2} C_i \left( \sqrt{\frac{2}{3}} |\mathbf{v}_i| \right)^2 \right] + \frac{3}{2} \mathbf{v}_i \cdot \mathbf{i}_{load\ i}^- & i &= 3, \\ P_i^+ &= \frac{d}{dt} \left[ \frac{1}{2} C_i (v_i^+)^2 \right] + v_i^+ \cdot i_{load\ i}^+ \\ P_i^- &= \frac{d}{dt} \left[ \frac{1}{2} C_i (v_i^-)^2 \right] + v_i^- \cdot i_{load\ i}^- \end{aligned} \right\} i \in [4;6], \tag{14}$$

being  $i_{load\ i}$  the current absorbed by the load connected to the  $i$ -th port. Considering (14), by tedious yet simple calculus, the derivatives of the tracking error are obtained as:

$$\left. \begin{aligned} \frac{d}{dt} (\mathbf{v}_i^* - \mathbf{v}_i) &= \frac{d}{dt} \mathbf{v}_i^* + j\omega \mathbf{v}_i + \frac{1}{C_i} \left( \mathbf{i}_{load\ i}^- - \frac{2}{3} \frac{\mathbf{S}_i^-}{\mathbf{v}_i} \right) & i &= 3, \\ \frac{d}{dt} (v_i^{+*} - v_i^+) &= \frac{d}{dt} v_i^{+*} + \frac{1}{C_i} \left( i_{load\ i}^+ - \frac{P_i^+}{v_i^+} \right) \\ \frac{d}{dt} (v_i^{-*} - v_i^-) &= \frac{d}{dt} v_i^{-*} + \frac{1}{C_i} \left( i_{load\ i}^- - \frac{P_i^-}{v_i^-} \right) \end{aligned} \right\} i \in [4;6]. \tag{15}$$

The dynamic voltage error equation should contain, in addition to the tracking error itself, the tracking error integral to enforce null static error, and tracking error derivatives up to the order necessary to obtain explicit dependence of the controlled variable  $\varepsilon_i$  from the control variable  $\mathbf{S}_i$  or  $P_i$ . From (15), it is observed that only one derivative term is needed, so that the dynamic voltage error equations are defined as:

$$\left. \begin{aligned} \boldsymbol{\eta}_i &= (\mathbf{v}_i^* - \mathbf{v}_i) + K_1 \frac{d}{dt} (\mathbf{v}_i^* - \mathbf{v}_i) + \frac{1}{K_2} \int (\mathbf{v}_i^* - \mathbf{v}_i) dt & i &= 3, \\ \eta_i^+ &= (v_i^{+*} - v_i^+) + K_1 \frac{d}{dt} (v_i^{+*} - v_i^+) + \frac{1}{K_2} \int (v_i^{+*} - v_i^+) dt \\ \eta_i^- &= (v_i^{-*} - v_i^-) + K_1 \frac{d}{dt} (v_i^{-*} - v_i^-) + \frac{1}{K_2} \int (v_i^{-*} - v_i^-) dt \end{aligned} \right\} i \in [4;6], \tag{16}$$

where  $K_1, K_2$  are time constants to be assigned to obtain the desired damping and dynamic response.



Consider now the system in a sliding condition, so that  $i_i = i_i^*$ , and, as a consequence,  $P_i = P_i^*$ . By substituting (15) in (16), it is possible to obtain the port reference power:

$$\left. \begin{aligned} \mathbf{S}_i^* &= \frac{3}{2} \mathbf{v}_i \left[ \left( C_i \frac{d}{dt} \bar{\mathbf{v}}_i^* + j\omega C_i \bar{\mathbf{v}}_i + \bar{\mathbf{i}}_{load\ i} \right) + g_{1i} (\bar{\mathbf{v}}_i^* - \bar{\mathbf{v}}_i) + g_{2i} \int (\bar{\mathbf{v}}_i^* - \bar{\mathbf{v}}_i) dt \right], \quad i = 3, \\ P_i^{+*} &= v_i^+ \left[ C_i \frac{d}{dt} v_i^{+*} + i_{load\ i}^{+*} + g_{1i} (v_i^{+*} - v_i^+) + g_{2i} \int (v_i^{+*} - v_i^+) dt \right] \\ P_i^{-*} &= v_i^- \left[ C_i \frac{d}{dt} v_i^{-*} + i_{load\ i}^{-*} + g_{1i} (v_i^{-*} - v_i^-) + g_{2i} \int (v_i^{-*} - v_i^-) dt \right] \end{aligned} \right\}, \quad i = [4;6], \quad (17)$$

where  $g_{1i} = C_i/K_1$ ,  $g_{2i} = C_i/(K_1K_2)$ . Note that (17) provides the reference power that realizes the control of the external port voltages with dynamics assigned by coefficients  $g_{1i}, g_{2i}$ . Furthermore, one can note that (17) is formally equivalent to a PI regulator with feed-forward/compensation terms: in (17), between square brackets, the first term between round brackets can be considered a feed-forward/compensation term, while the second and third terms are, respectively, proportional and integral terms.

After the control of  $v_3, v_4, v_5, v_6$  is defined, control references for ports 1 and 2 are designed in terms of port powers with the aim of controlling the MC internal bus voltage. In these regards, the global reference power that must be absorbed from ports 1 and 2 to maintain the internal bus voltage is defined as  $P_g^* = P_1^* + P_2^*$ . The internal DC bus voltage can hence be controlled by considering the power balance at the internal DC bus terminals, which, observing that the internal bus depicted in Figure 3 includes six couples of series-connected capacitors, results in:

$$P_g = \frac{d}{dt} \left[ \frac{1}{2} \left( \frac{6C_{in}}{2} \right) v_{in}^2 \right] + \frac{3}{2} \text{Re} \left\{ \mathbf{v}_3 \mathbf{i}_3 \right\} + \sum_{i=4}^6 (v_i^+ \cdot i_i^+ + v_i^- \cdot i_i^-), \quad (18)$$

where  $v_{in} = v_{in}^+ - v_{in}^-$  represents the internal bus pole-to-pole voltage. By means of the same procedure used to obtain (17), the control law for the DC bus voltage is obtained from (18), resulting in:

$$\begin{aligned} P_g^* &= v_{in} \left[ \frac{6}{2} C_{in} \frac{d}{dt} v_{in}^* + g_{1\ in} (v_{in}^* - v_{in}) + g_{2\ in} \int (v_{in}^* - v_{in}) dt \right] + \\ &+ \text{Re} \{ \mathbf{S}_3^* \} + \sum_{i=4}^6 (P_i^{+*} + P_i^{-*}), \end{aligned} \quad (19)$$

where  $g_{1\ in} = (6/2)C_{in}/K_1$ ,  $g_{2\ in} = (6/2)C_{in}/(K_1K_2)$ . Note that, similar to the control of external port voltages realized by (17), (19) provides the reference power to control of the internal bus voltage with dynamics assigned by coefficients  $g_{1\ in}, g_{2\ in}$ , and is formally equivalent to a PI regulator with feed-forward/compensation terms.

Power  $P_g^*$  must be split into ports 1 and 2 by means of a suitable logic, such as:

$$\begin{cases} P_1^* = \beta_1 P_g^* \\ P_2^* = \beta_2 P_g^* \end{cases}, \quad \beta_1 + \beta_2 = 1, \quad (20)$$

where the terms  $\beta_i$  can be constants, functions, or references obtained from an upper-level supervisory control.

Lastly, for the considered three-wire configuration, it is necessary to introduce the equilibrator control to maintain voltage balance. Define voltage unbalance as:

$$v_{bal} = v_{in}^+ + v_{in}^-, \quad (21)$$

and recognizing that, in the present topology, only DC ports can introduce voltage unbalances, the unbalance power is consequently defined as:

$$P_{un} = \sum_{i=4}^6 (P_i^{+*} - P_i^{-*}), \quad (22)$$

such that it is possible to introduce a power balance equation similar to (18) for the internal bus. Observing that the internal bus depicted in Figure 3 includes six couples of capacitors, parallel-connected with respect to voltage balancing, the desired power balance equation results in:

$$P_{bal} = \frac{d}{dt} \left[ \frac{1}{2} (12C_{in}) v_{bal}^2 \right] - P_{un}. \quad (23)$$

Considering (23) and recognizing that  $v_{bal}^* = 0$ , the reference balancing power is obtained as

$$P_{bal}^* = v_{in} \left[ g_{b1} v_{bal} + g_{b2} \int v_{bal} dt \right] - P_{un}, \quad (24)$$

where gains are defined as  $g_{b1} = (12C_{in})/(K_1)$ ,  $g_{b2} = (12C_{in})/(K_1K_2)$ . If more than one equilibrator is present, balancing power can be treated, similarly to (20), by means of a number of suitable, unity-sum coefficients.

Lastly, current references for each port are obtained from power references as:

$$\mathbf{i}_i^* = -\frac{2}{3} \frac{P_i^*}{\mathbf{v}_i} \quad i = 1, \quad (25)$$

$$i_i^* = -\frac{P_i^*}{v_i} \quad i = 2, \quad (26)$$

$$\mathbf{i}_i^* = \frac{2}{3} \frac{\mathbf{S}_i}{\mathbf{v}_i} \quad i = 3, \quad (27)$$

$$\left. \begin{aligned} i_i^{+*} &= \frac{P_i^{+*}}{v_i^+} \\ i_i^{-*} &= \frac{P_i^{-*}}{v_i^-} \end{aligned} \right\} i \in [4, 6], \quad (28)$$

$$i_{bal}^* = \frac{P_{bal}^*}{v_{in}}. \quad (29)$$

Note that (25), being aimed at controlling the internal bus voltage through (19), includes active power only. Clearly, a certain reactive power can be also exchanged if necessary, resulting in a control equation similar to (27). In more general cases, (25) and (26) are valid for, respectively, AC and DC ports connected to controllable energy sources, while (27) and (28) are valid, respectively, for AC and DC ports connected to loads or non-controllable energy sources (i.e., PV plants). Each current reference magnitude should also be limited to a predetermined value, depending on the semiconductors' maximum current, in order to avoid possible issues in cases of external faults.

#### 4. Fault Analysis

For the proposed MC, it is of interest to evaluate the effect of an external fault, of a fault on the internal DC link, and to briefly discuss the proposed MC properties in terms of fault management derived by the proposed control design. Each of these aspects is addressed in the following subsections.

##### 4.1. External Fault Analysis

For the considered MC converter, it is of interest to consider external faults on both AC and DC ports. These faults have a different effect on converter operation, depending on port functionality. If the faulted port is connected to a controllable energy source, the voltage reduction due to the fault makes it impossible to transfer the power required by higher-level control without exceeding the converter current limits. As a consequence, the power balance in the internal bus is momentarily lost, resulting in a voltage deviation, which will then be compensated by the converter control by acting on the power exchange

on the healthy ports. If the faulted port is connected to a load or non-controllable energy source, then the fault will make it impossible to maintain the correct voltage without exceeding the converter current limits. As a consequence, voltage regulation is lost.

In both cases, however, the converter current control is maintained over the whole transient, ensuring the converter operation’s safety. This is obtained by virtue of the stability properties of sliding mode controllers [59–62]. Indeed, the condition that allows the sliding condition to be reached in finite time and maintains sliding condition thereafter is expressed by (4) for each PEBB realizing an AC port, and by (10) for any module realizing a DC port. During normal operating conditions, (4) and (10) are usually satisfied for a correctly designed system under a non-restrictive hypothesis, namely, when capacitor voltages and current references are ascribable to suitable, limited, Lipschitz-continuous functions. This is taken for granted in the case of capacitor voltages, yet two significant exceptions must be considered for currents, namely, external faults and load step-changes, as the line current  $i_{load\ i}$  at the  $i$ -th port appears in power references (17). Between these two occurrences, the fault is of course the worst case, as not only can an uncontrolled transient be experienced by the system, but it may also not be possible to regulate the port voltage or exchange the required power after the transient is extinguished, depending on the value of the fault impedance. As a worst case, let us hence consider the case of a bolted fault.

For a DC port, let us consider, with no loss of generality, a bolted pole-to-midpoint fault. A pole-to-pole fault can be treated similarly due to the converter’s symmetric structure. Additionally, let us neglect, in the mathematical analysis, the diodes connected in parallel to each DC port output capacitor, which as mentioned, are used to prevent the port voltage from changing its sign, which would result in loss of controllability and possible converter damage.

In case of a bolted pole-to-midpoint fault, the  $i$ -th DC port, the fault causes an uncontrollable current in the faulted line as the converter output capacitor rapidly discharges through the line and the fault. Denote the line resistance and inductance as  $R_{line\ i}$  and  $L_{line\ i}$ , respectively, and assume, for simplicity of notation, that the fault occurs at time  $t = 0$ , the MC fault current contribution can be calculated as a simple second order RLC transient. With reference to Figure 3 for variables, the MC DC fault current contribution is generally obtained as:

$$i_{load\ i}(t) = H_{1i}e^{s_{1i}t} + H_{2i}e^{s_{2i}t} + I_{Max\ i}, \tag{30}$$

where  $H_{1i}, H_{2i}$  are constants depending on the circuit initial conditions,  $s_{1i}, s_{2i}$  are constants defined as:

$$\begin{cases} s_{1i} = -\alpha + \sqrt{\alpha^2 - \omega_0^2} \\ s_{2i} = -\alpha - \sqrt{\alpha^2 - \omega_0^2} \end{cases} \tag{31}$$

where  $\alpha = R_{line\ i}/(2L_{line\ i})$  and  $\omega_0 = 1/\sqrt{(L_{line\ i}C_i)}$  and  $I_{Max\ i}$  is the constant converter current limit set by the converter control, as mentioned at the end of Section 3.2, which is to be considered the fault steady-state value and, hence, the transient steady-state solution.

When denoting the initial condition for the converter fault current contribution as follows:

$$\begin{cases} i_{load\ i}(0) = I_0 \\ \frac{d}{dt}i_{load\ i}(0) = \frac{v_i(0) - R_{line\ i}i_{load\ i}(0)}{L_{line\ i}} \end{cases}, \tag{32}$$

the constants  $H_{1i}, H_{2i}$  are obtained as:

$$\begin{cases} H_{1i} = \frac{v_i(0) - R_{line\ i}i_{load\ i}(0) - (I_{Max\ i} - i_{load\ i}(0))L_{line\ i}s_{2i}}{L_{line\ i}(s_{1i} - s_{2i})} \\ H_{2i} = -\frac{v_i(0) - R_{line\ i}i_{load\ i}(0) - (I_{Max\ i} - i_{load\ i}(0))L_{line\ i}s_{1i}}{L_{line\ i}(s_{1i} - s_{2i})} \end{cases} \tag{33}$$

Equations (30)–(33) characterize the fault response of a DC port, but can be easily adapted to AC ports, for each phase, as follows. In this case, (30) and (31) can be used as is, which is the general solution for an RLC circuit transient. The term  $I_{Max\ i}$  appearing in (30) maintains the same meaning, but must be considered as a sinusoidal function

( $I_{Max\ i}(t) = I_{Max\ i} \sin(\omega t + \varphi)$ ), the amplitude of which is equal to the maximum current contribution set by the converter control. The initial conditions are again defined by (32), yet the solution for the constants  $H_{1i}, H_{2i}$  must now consider the sinusoidal steady-state solution, resulting in:

$$\begin{cases} H_{1i} = \frac{v_i(0) - R_{line} i_{load\ i}(0) - (I_{Max\ i}(0) - i_{load\ i}(0)) L_{line} i s_{2i} - L_{line} i \frac{d}{dt} I_{max\ i}(0)}{L_{line} i (s_{1i} - s_{2i})} \\ H_{2i} = - \frac{v_i(0) - R_{line} i_{load\ i}(0) - (I_{Max\ i}(0) - i_{load\ i}(0)) L_{line} i s_{1i} - L_{line} i \frac{d}{dt} I_{max\ i}(0)}{L_{line} i (s_{1i} - s_{2i})} \end{cases} \quad (34)$$

However, as is also the case with bolted faults, current references can be approximated with a Lipschitz-continuous function, except from a limited time. Indeed, it is straightforward to prove that the fault current (30) can exhibit, during the transient phase only, a time derivative higher than the one enforced by the converter current control, the upper bound of which, neglecting resistive terms and external voltage, can be approximated as:

$$\frac{di_{max}}{dt} = \frac{v_D}{L} \quad (35)$$

As a consequence, during the transient phase, voltage regulation and power exchange may not be performed correctly.

However, after the transient is extinguished, (4) and (10) are satisfied for any port. As a consequence, while the potential to control the port voltage/power depends on the fault impedance value, the current sliding condition is lost at the instant corresponding to the step-change, but then reached again in finite time. As a consequence, a pole-to-pole fault on one port does not violate (4) and (10) except from a very limited time, so that output currents are always kept under control and no faults on one output port can affect other ports or the internal DC bus. Additionally, under pole-to-pole fault conditions, which (4) and (10) have satisfied for voltage values smaller than the rated ones, the converter current control is maintained, so that the converter can limit the fault current to a predetermined, bearable value, such that the converter is self-protected during faults. In these regards, the most obvious choice is to keep the current constant and equal to its maximum value until the fault is resolved and voltage can be recovered. If the fault is not resolved in a predetermined time (reasonably, a few seconds) the current reference is set to zero for safety reasons. Nevertheless, if the converter control is integrated in the system protection, any fault current value can be selected.

When considering pole-to-earth faults, different problems arise depending on the state of active parts towards earth. Usually, low-voltage distribution systems are not exercised when isolated from earth, except in special applications or in regions where effective earthing is problematic, such that it is of interest to briefly consider the possible earthing solution for a system including the considered MC. With reference to Figure 3, the presence of the distributed neutral wire/DC middle point for all ports suggests that the neutral wire should be directly earthed, as is usual for AC systems. In this case, both for AC and DC systems, the proposed three-wire converter allows for correct system operation and earth fault clearance, since earth faults are equivalent to pole-to-pole faults and the considerations presented in the previous paragraph apply.

Furthermore, in hybrid distribution systems, the proposed converter topology forces the state of active parts towards earth of each section to be the same, unless isolated ports are introduced. This greatly simplifies the definition of earthing policies with respect to systems with many isolated sections and avoids unnecessary cascaded conversion stages. A significant advantage is also gained if the AC port is connected to a load or load feeder and if the AC port is connected to an AC power source. If the AC port is feeding loads, this implies that it is possible to use either a TT or TN earthing scheme, which was not possible with the two-wire MCs considered in [11], and simplifies the evaluation of electrical safety issues. If, on the contrary, the AC port is connected to an AC power source, this does not require an isolation transformer, even if a transformer is already present (i.e., MV/LV

transformer), to isolate the star centre from earth. Furthermore, problems similar to the ones discussed in [40] cannot arise due to the symmetry of the considered MC.

To complete the discussion on earth faults, a detailed analysis of this configuration in earth-isolated systems should be performed. However, this can be difficult since it is necessary to evaluate parasitic system parameters, which are difficult to assess and very case-dependent. Even though a detailed analysis of earth faults lies outside the purposes of this paper, the presented considerations clarify that, in the case of a directly earthed neutral wire, correct operation can be achieved, and fault clearance is possible both for pole-to-pole and pole-to-earth faults. Furthermore, AC and DC ports can be freely introduced with no need for specific adaptations and with no risks of common-mode voltage-related issues.

#### 4.2. Internal Fault Analysis

As previously mentioned, the condition that allows the sliding condition to be reached in finite time and maintains sliding condition thereafter is expressed by (4) for each PEBB realizing an AC port or equilibrator, and by (10) for any module realizing a DC port. These conditions are usually satisfied for a correctly designed system under a non-restrictive hypothesis, which in this case can be reduced to the capacitor voltages and current references being ascribable to suitable, limited, Lipschitz-continuous functions.

In case of a pole-to-pole and, possibly, a pole-to-earth fault on the internal DC bus, the internal voltage will be reduced, possibly down to zero, depending on the fault impedance values. As the external voltages are initially non-null, both (4) and (10) are violated, and uncontrolled currents flow through free-wheeling diodes in all PEBBs, which may result in damage. This occurrence cannot be avoided by any control algorithm, but its probability can be considered very low as the internal DC link can be easily included in a switchboard.

### 5. Simulation Results

Simulations were performed to substantiate the considered topology and related controls. Load and source parameters are presented in Table 1.

**Table 1.** Loads and sources.

Port	Connection	Details
1	Main AC Grid	400 V, 50 Hz
2	Lithium batteries	3.3 V, 60 Ah per module; 143 series connected modules
3	AC load	400 V, 50 kW, $\cos \varphi = 1$
4+	PV panels	75 kW, no-load voltage 450 V (assumed constant 50 kW in simulation)
4−	PV panels	75 kW, no-load voltage 450 V (assumed constant 50 kW in simulation)
5+	DC Load	400 V, 40 kW, variable resistive load
5−	DC Load	400 V, 40 kW, variable resistive load
6+	DC Load	400 V, 40 kW, variable resistive load
6−	DC Load	400 V, 20 kW, variable resistive load

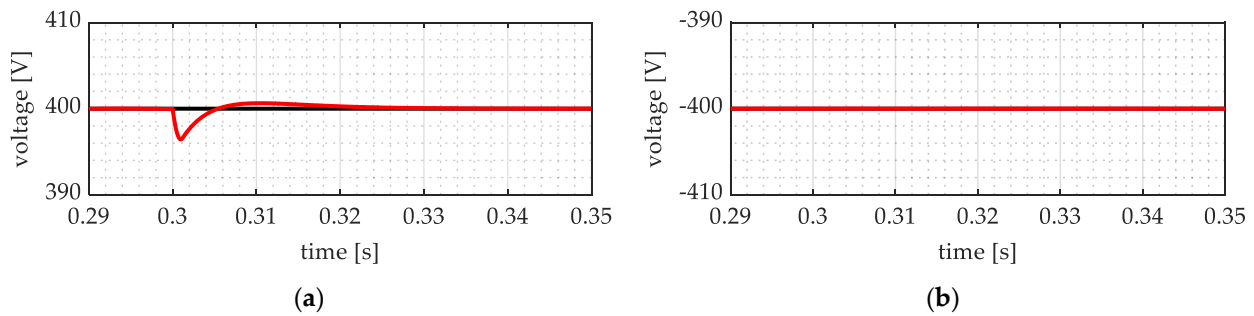
For compactness, the positive and negative halves of each port are identified with a plus and minus (e.g., 5+ represents the electric port constituted by the fifth port positive pole and middle point, while 5− represents the electric port constituted by the fifth port middle point and negative pole). Converter and control parameters are shown in Table 2. Four events were considered in order to show the control's effectiveness in managing abrupt load variations, main grid failure, and external faults. Each of these events is discussed separately in the following subsections.

**Table 2.** Three-wire, capacitive-coupled MC parameters.

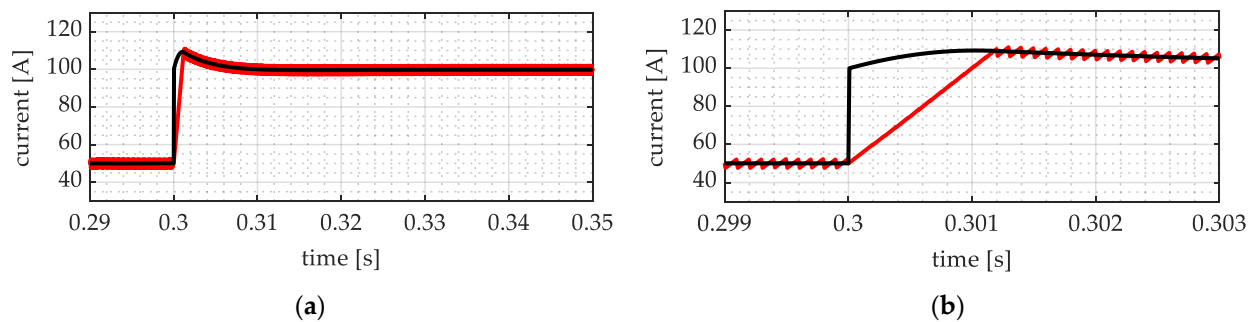
Rated Values		Components			
Internal Voltage	$\pm 450$ V	$L_i$	1 mH	$L_{eq}$	2 mH
Switching Frequency	10 kHz	$R_i$	10 m $\Omega$	$R_{eq}$	20 m $\Omega$
Maximum Port Current	250 A	$C_{1,3}$	400 $\mu$ F	$C_{4,5,6}$	6.8 mF
Control Time Constant	5 ms	$C_{in}$	1.1 mF		

### 5.1. DC Load Asymmetrical Step-Change

The first considered event is a DC load asymmetrical step-change from 20 kW to 40 kW on port 5+, occurring at time 0.3 s. The corresponding voltages  $v_{5^+}$ ,  $v_{5^-}$  are reported in Figure 4a,b. Currents  $i_{5^+}$  is reported in Figure 5a,b. One can notice that voltage and current transients exhibit the expected behaviour: initially, the load step-change causes a fast change in the current reference, which causes a violation of controllability condition (10) and, consequently, a temporary loss of sliding condition. By roughly one millisecond, condition (10) is satisfied again, reaching phase is established, and sliding condition is enforced. Once sliding condition is reached, voltage error is forced to zero following the assigned dynamic, such that nominal voltage is restored in about 25 ms ( $\cong$  five time constants). In addition, one can note that the voltage of the negative half on port five is not affected by any perturbation (Figure 4b).

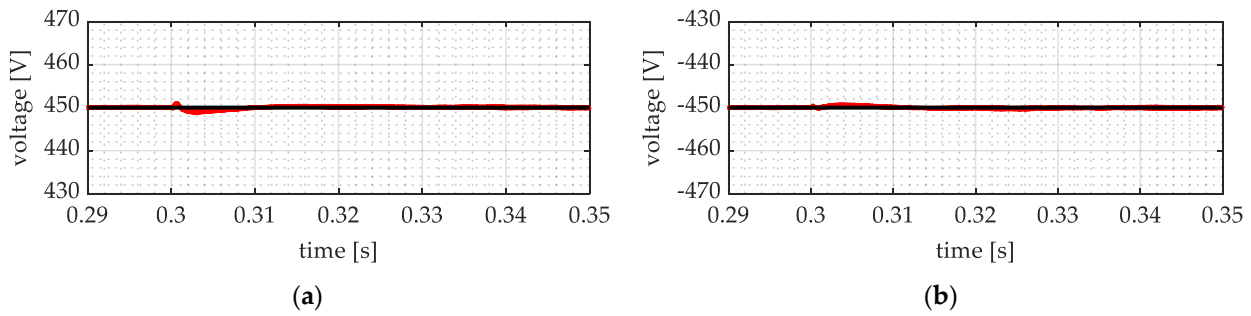


**Figure 4.** Port 5: (a) voltage  $v_{5^+}$  reference (black) and actual value (red); and (b) voltage  $v_{5^-}$  reference (black) and actual value (red) during DC load transient.



**Figure 5.** Port 5: (a) current  $i_{5^+}$  reference (black) and actual value (red) during DC load transient; and (b) reaching detail.

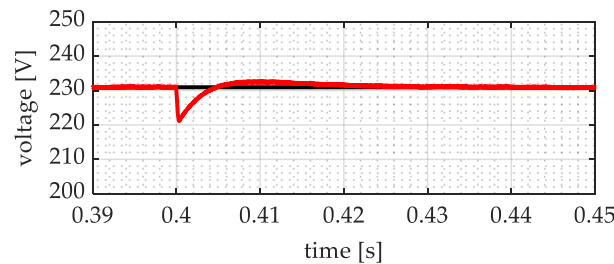
To verify the effectiveness of the equilibrator control in balancing internal voltages, the internal voltages  $v_{in^+}$  and  $v_{in^-}$  are reported in Figures 6a and 6b, respectively. One can observe that, except from a negligible transient in correspondence of the DC load step change, voltages track their respective references correctly and no voltage unbalance due to load unbalance is present.



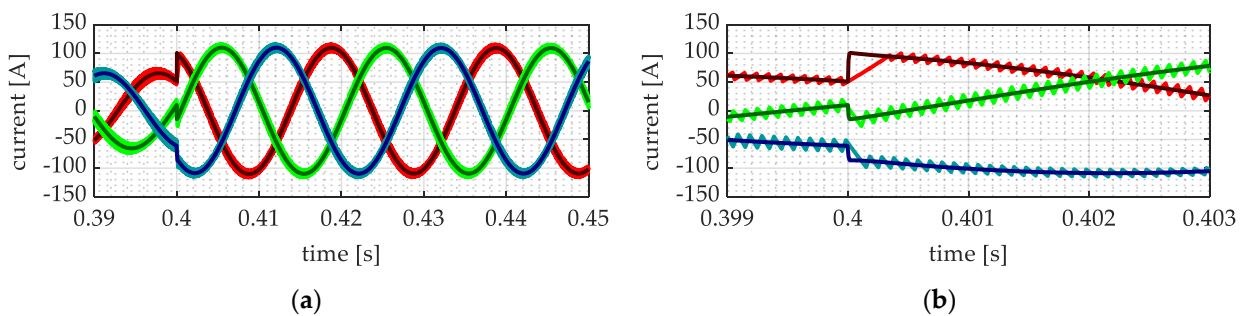
**Figure 6.** (a) Internal bus positive pole voltage reference (black) and actual value (red); and (b) internal bus negative pole voltage reference (black) and actual value (red) during DC load transient.

5.2. AC Load Step-Change

The second considered event is an AC load step-change from 25 kW to 50 kW on port 3, occurring at 0.4 s. Since a small, few-milliseconds-long transient on three phase variables can be hardly appreciated, the port 3 voltage module is shown in Figure 7. On the contrary, to appreciate the current tracking effectiveness during fast transients, phase currents are shown in Figure 8a,b. The same considerations reported for the DC load step-change apply, with particular reference to voltage tracking dynamics, momentary loss of the sliding condition, reaching phase, and re-enforcement of sliding condition. In addition, it can be noted that, since the difference between AC voltage and internal DC link voltage is larger than the difference between DC port voltages and internal DC link voltage, the maximum current derivative that can be impressed by the converter on the AC port currents is higher, resulting in a shorter reaching phase (Figure 8b).



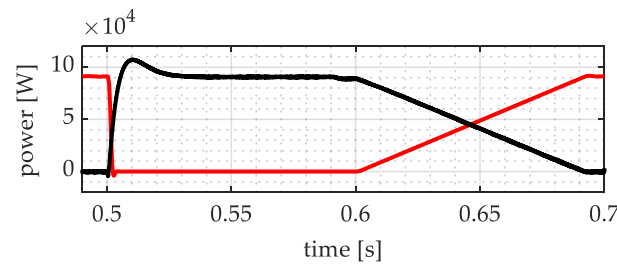
**Figure 7.** Port 3: voltage space vector reference module (black) and actual module (red) during AC load transient.



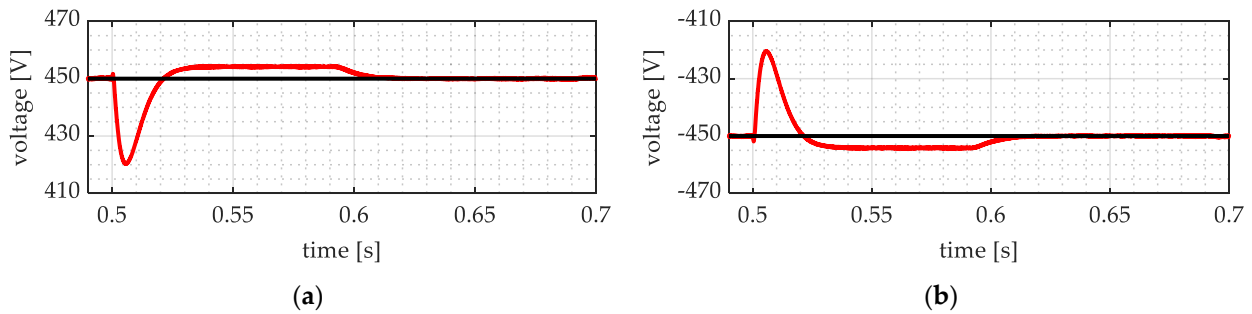
**Figure 8.** Port 3: (a) current references (dark red, green, and blue) and actual values (bright red, green and blue) during AC load transient; and (b) reaching detail.

5.3. AC Mains Fault

The third considered event is a fault affecting the main AC grid, connected to port 1, from 0.5 s to 0.6 s. The power absorbed from the available sources is shown in Figure 9, while the internal bus positive and negative pole voltages are shown in Figures 10a and 10b, respectively.

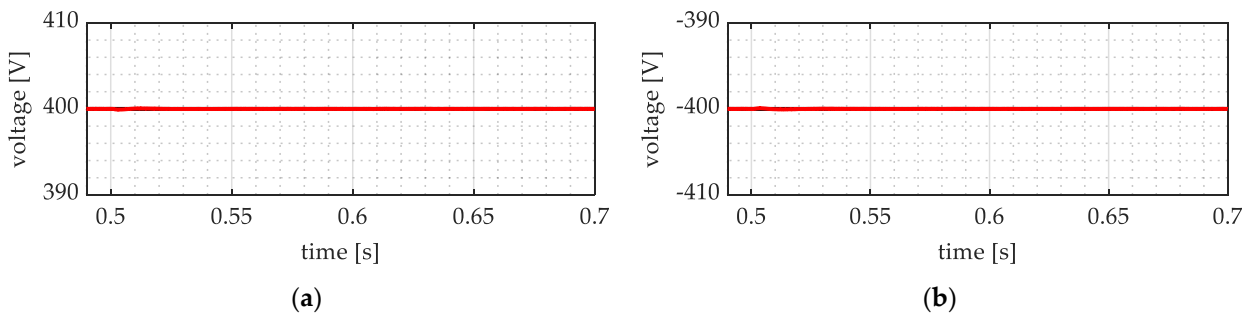


**Figure 9.** Sources powers during main grid out of service and reconnection: main grid (black), lithium batteries (red).



**Figure 10.** (a) internal bus positive pole voltage reference (black) and actual value (red); and (b) internal bus negative pole voltage reference (black) and actual value (red) during main grid out of service and reconnection.

Port five voltages  $v_5^+$ ,  $v_5^-$  are shown in Figures 11a and 11b, respectively. It can be seen that the batteries correctly operate to provide the requested power, such that the internal bus voltage experience a reasonable transient; load voltages (Figure 11a,b) are unaffected by the main grid outage. This is consistent with the considerations discussed in Section 4 in which only the module directly connected to the grid loses its sliding condition due to the fault so that the only voltage affected by any disturbance is the internal voltage, as it is controlled by that module. Consequently, the internal voltage is strictly controlled, with a perturbation during the disconnection from the grid, which does not have an impact on load voltages, and creates a negligible one during the reconnection.



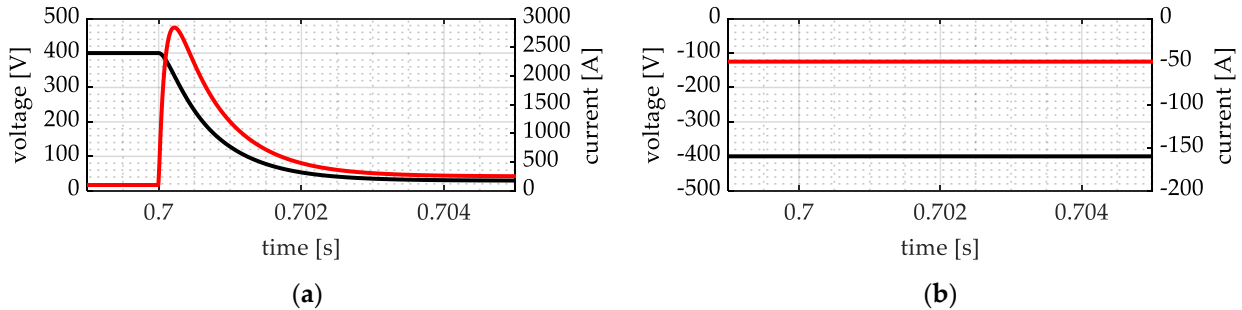
**Figure 11.** Port 5: (a) voltage  $v_5^+$  reference (black) and actual value (red), and (b) voltage  $v_5^-$  reference (black) and actual value (red) during main grid out of service and reconnection.

#### 5.4. DC Port External Fault

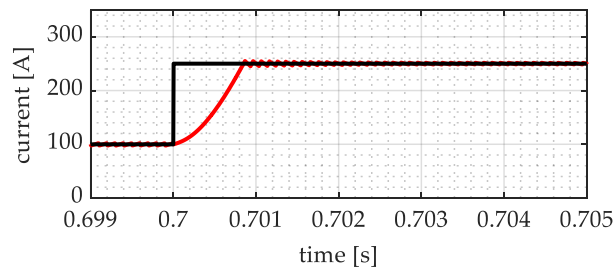
The fourth considered event is an external fault, namely, a bolted pole-to-midpoint fault on port 6+, occurring at time 0.7 s. The corresponding voltage  $v_6^+$  and current  $i_{load 6}^+$  are shown in Figure 12a, while port 6 voltage  $v_6^-$  and current  $i_{load 6}^-$  are shown in Figure 12b. Current  $i_6^+$  is shown in Figure 13; and port 5 voltages  $v_5^+$ ,  $v_5^-$  are shown in Figure 14a and 14b, respectively. It can be seen that, even though an uncontrolled fault current is experienced from the line/load, the current supplied by the converter remains



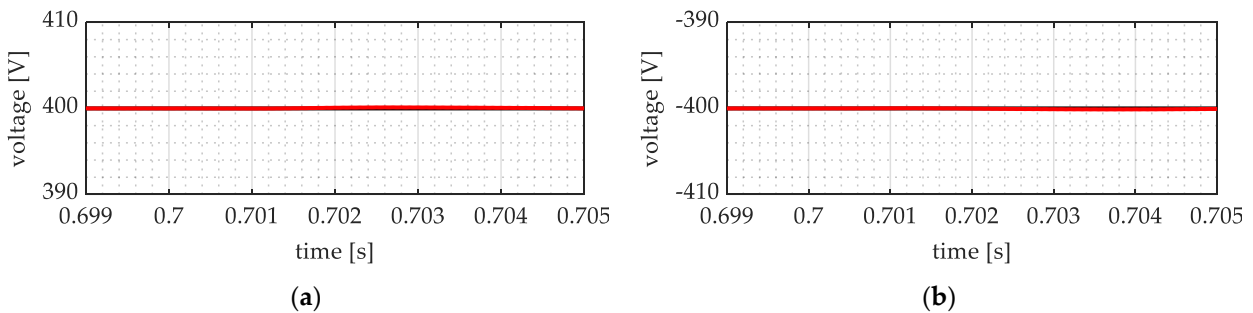
controlled during the whole fault and is correctly limited to a predetermined value. Furthermore, the healthy half of the faulted port and the other healthy port voltages are unaffected by the fault: this is again consistent with Section 4, in that there is no reason for those ports to lose the sliding condition.



**Figure 12.** Port 6: (a) voltage  $v_6^+$  (black) and current  $i_{load\ 6}^+$  (red); and (b) voltage  $v_6^-$  (black) and current  $i_{load\ 6}^-$  (red) during the short circuit on port 6.



**Figure 13.** Port 6: current reference (black) and actual value (red) during the short circuit on port 6.



**Figure 14.** Port 5: (a) voltage  $v_5^+$  reference (black) and actual value (red); and (b) voltage  $v_5^-$  reference (black) and actual value (red) during the short circuit on port 6.

As per the presented results, the considered MC exhibits robustness properties with respect to external faults, including power supply failure/perturbations, in that (4) and (10) ensure that current controllability is maintained. The presented results reinforce the consideration that the considered MC topology is particularly suited for centralized architectures, where the possibility to have a protected internal DC bus reduces the probability of internal faults. In this case, it is possible to take advantage of the external fault insensitivity of the proposed converter, which can ensure fault clearance in cases of both pole-to-pole and pole-to-earth faults.

## 6. Conclusions

While MCs have been widely studied for a wide range of applications, their application to LVDC distribution systems is worthy of further discussion due to three main issues. First, a modular topology seems to be of the utmost importance for distribution systems application, but this issue is often overlooked. Second, electronic power converters

introduce a discontinuity in the neutral wire and earthing management of hybrid AC/DC systems, which is usually addressed by introducing galvanically isolated converters, resulting in unnecessary cascaded conversion stages and complex earthing management. Third, the possibility of exploiting converter control capabilities to mitigate fault effects is scarcely explored.

In order to overcome the issues of limited modularity, interference with the state of active parts towards earth, and controllability in fault conditions, a new MC for hybrid distribution systems is introduced in this paper. This introduces two main contributions for MC applications: first, a new MC topology is introduced, and an innovative control structure based on two control layers is proposed, including a pseudo-sliding mode controller directly acting on semiconductor switching, and an inverse dynamic control approach applied to voltage controller design. Second, to overcome the lack of effective DC circuit breakers, which represents a traditional issue in DC systems, the proposed control approach is developed with particular attention to current controllability during faults, and the proposed MC properties are investigated with respect to this issue.

The presented results highlight that the proposed MC converter and its control algorithms can effectively manage different loads, providing a high-quality power supply not affected by abrupt load variations or faults on other ports. Additionally, the proposed MC was shown to behave as a fault-tolerant power hub, and can be integrated in hybrid distribution systems protection algorithms without the traditional limitations of power converters that may suffer damage from grid faults.

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