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Controlling the threshold voltage of a semiconductor field-effect transistor by gating its graphene gate

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The threshold voltage of a field-effect transistor (FET) determines its switching and limits the scaling of the supply voltage in the logic gates. Here we demonstrate a GaAs FET with a monolayer graphene gate in which the threshold voltage was externally controlled by an additional control gate. The graphene gate forms a Schottky junction with the transistor channel, modulating the channel conductivity. The control gate sets the work function of the graphene gate, controlling the Schottky barrier height and therefore the threshold voltage, and reduces the subthreshold swing down to ~60 mV dec^{-1}. The change of the threshold voltage was large enough to turn the initially depletion mode FETs into the enhancement mode FETs. This allowed to realize logic gates with a positive switching threshold in which the threshold voltage of each transistor was independently set. The presented FETs can also be operated as dual-gate FETs, which was demonstrated by realizing frequency mixers.

INTRODUCTION

The continuous scaling and requirements for low-power operation of field-effect transistors (FETs) limit the range of threshold voltage (V_{th}), which is the gate-source voltage (V_{GS}) at which a FET turns on. In modern FETs, the gates are made of metal and consequently, the threshold voltage cannot easily be adjusted because it is fixed by the work function of the metal. This problem is even more exacerbated in metal-semiconductor FETs (MESFETs) and high-electron-mobility transistors (HEMTs), which are used in high-speed communication systems[1]. In such FETs, there is an additional constraint on the threshold voltage as prohibitively large gate leakage current (I_G) is obtained if V_{th} was not properly adjusted. This is because the channel carrier density in these FETs is usually controlled by a Schottky barrier between the metal gate and semiconductor[2]. The gate current is therefore the current of the Schottky junction which must stay in the off state to keep the gate leakage negligible. The inability to tune the work function of the gate metal, on which the Schottky barrier height (SBH) and consequently the turn-on voltage of the Schottky junction critically depend, limits possible applications of MESFETs and HEMTs.

A better control of the threshold voltage of FETs could be obtained if the gate metal was replaced by a material of adjustable work function. Prior to the 45 nm technology node, poly-Si gates were used to set the threshold voltage in metal-oxide-semiconductor FETs during their fabrication[3,4]. However, poly-Si cannot be used in MESFETs and HEMTs and its work function cannot be adjusted after fabrication, i.e., during device operation. Such adjustment is possible in graphene because its Fermi level (and therefore the work function) can be controlled by an external electric field. The field effect in graphene has mainly been exploited in the applications in electronics in which graphene was used as a transistor channel of graphene field-effect transistors (GFETs). However, graphene also forms a Schottky junction with most of the semiconductors[5,6], which has previously been used to realize photodetectors[7–10], solar cells[11–13],

sensors[14,15], optical modulators[16], mixers[17], and MESFETs with a graphene gate[18–22]. The ability of graphene to form a Schottky junction with semiconductors and consequently act as a gate in a MESFET, opens up a perspective of the control of the threshold voltage of FETs. The electrostatic control of the SBH of graphene-semiconductor Schottky junctions has been used in the past to realize barristors[23], vertical heterostructures[24], and strain sensors[25].

Here we demonstrate a semiconductor MESFET with a graphene gate, i.e., a graphene-semiconductor FET (GESFET), in which the carrier density in the GaAs transistor channel was set by a monolayer graphene gate. An additional Al/AlO$_x$ control gate was fabricated on top of the graphene gate to externally control the threshold voltage of the transistor. The control gate sets the Fermi level of the graphene gate which adjusts the SBH at the graphene/GaAs interface and therefore the threshold voltage. By changing the voltage between the control and graphene gate, it was possible to change the threshold voltage of the GESFET by up to ~1.4 V. This allowed to change the sign of V_{th} (e.g., to shift V_{th} from −0.8 to 0.6 V) in GESFETs with a thin (~250 nm) GaAs channel, i.e., to turn their operation from depletion to enhancement mode after fabrication, which cannot be obtained in conventional MESFETs and HEMTs. The ability to externally control the FET mode was exploited to realize the logic gates with a positive switching threshold, i.e., the logic gates which could be cascaded. The demonstrated GESFETs can also be independently operated by each of the gates as dual-gate transistors. The dual-gate operation allowed the realization of novel functionalities, e.g., frequency up or down-conversion mixers without input resistors and therefore input power dissipation.

RESULTS

GESFET with a single gate

Figure 1a shows the schematic of a GESFET in which the transistor channel between the source (S) and drain (D) was
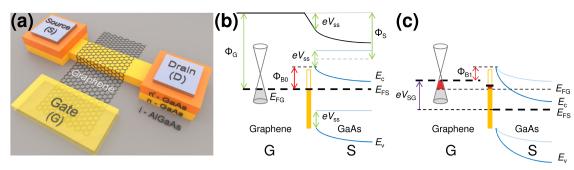
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Fig. 1 Standard (single-gate) GESFET. a A schematic of a standard GESFET fabricated on an intrinsic GaAs/AlGaAs substrate (orange/yellow/gray) epitaxially grown by molecular-beam epitaxy (MBE). The graphene gate (gray with hexagonal pattern) was transferred on top of the n-GaAs transistor channel (yellow) and was externally accessed through the Au gate pad (transparent yellow). The source and drain contacts (lavender) were evaporated on an n^+-GaAs layer (orange) to create an ohmic contact with the n-GaAs channel. **b** The equilibrium band diagram of a GESFET in the vertical direction, i.e., from the graphene gate (G) to surface states (orange bar) and n-GaAs channel (S). The Fermi level in graphene (E_{FG}) is equal to the Fermi level in the channel (E_{FS}) at $V_{GS} = 0$ V. The work function of the graphene gate and channel are Φ_G and Φ_S, respectively. The bottom of the conduction band and the top of the valence band in GaAs are denoted by E_c and E_v, respectively. V_{ss} is the voltage drop on the surface states and Φ_{B0} is the SBH. **c** The same band diagram at $V_{GS} < 0$ V, i.e., when the gate-source voltage is used to deplete the n-GaAs channel. The electrons from the depletion region fill the surface and graphene states (red). The thick dashed line shows the position of the Fermi level in each of the materials. The SBH is reduced to $\Phi_{B1} < \Phi_{B0}$.
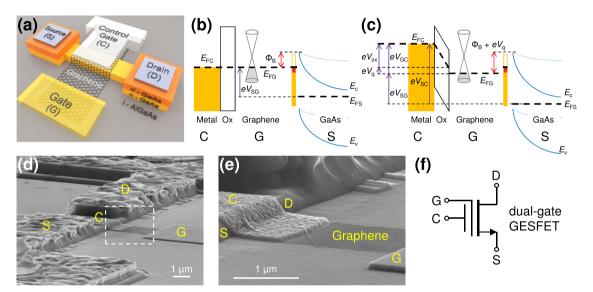

Fig. 2 Dual-gate GESFET. a A schematic of a dual-gate GESFET which differs from the standard (single-gate) GESFET in having a control gate (C; white) fabricated on top of the graphene gate. **b** The equilibrium band diagram of a dual-gate GESFET in the vertical direction, i.e., from the control-gate stack, comprising gate metal (C) on top of gate oxide (Ox), to the graphene gate (G), surface states (orange bar) and n-GaAs channel (S). The diagram is drawn for $V_{GC} = 0$ V (i.e., when the control gate is connected to the graphene gate) and $V_{GS} < 0$ V (i.e., when the channel is depleted). The SBH is Φ_B. **c** The same band diagram for $V_{GC} > 0$ V, i.e., when the voltage between the graphene and control gate is used to increase the SBH to $\Phi_B + eV_q$, where V_q is the voltage drop between graphene and its metal contact. V_{ox} is the voltage drop on the gate oxide, i.e., $V_{GC} = V_{ox} + V_q$. **d** A SEM image of a dual-gate GESFET. The top surface of the source and drain contacts is n^+-GaAs layer which became rough after annealing. **e** The enlarged part of the previous image within the enclosed white dashed rectangle. **f** The proposed circuit symbol of a dual-gate GESFET.

made of n-type GaAs. The gate (G) was made of monolayer graphene grown by chemical vapor deposition (CVD), which was transferred on top of the GaAs channel. The graphene gate was externally accessed through an Au electrode which forms an Ohmic contact with graphene. The depletion layer of the Schottky junction, formed between the graphene gate and GaAs channel, extends into the channel and reduces the thickness of the conductive (i.e., not depleted) part of the channel. This thickness was controlled by the Schottky junction voltage (V_{GS}), which modulates the depletion layer width and therefore the drain current (I_D) between the source and drain. For instance, the decrease of V_{GS} increases the depletion layer width and therefore decreases the drain current. The largest modulation of the drain current was obtained when the Schottky junction was reversely biased ($V_{GS} < 0$ V) due to the weak modulation of the depletion

layer width in forward bias ($V_{GS} > 0$ V)[2]. The use of the forward bias was also limited by the forward current of the Schottky junction which represents the gate leakage current in this FET. The electrical characteristics of the graphene/GaAs Schottky junction are shown in Supplementary Fig. 1.

At $V_{GS} = 0$ V, the conductivity of the GESFET channel depends on its thickness. We found that thin channels (<50 nm) were completely depleted at $V_{GS} = 0$ V. Such GESFETs could only be turned on at positive V_{GS} (provided that the channel is not too thin), i.e., they had $V_{th} > 0$ V and operated in the enhancement mode. However, such FETs exhibited poor performance due to the weak modulation of the depletion layer width and large gate leakage current of the Schottky junction under forward bias. The thicker channels were conductive at $V_{GS} = 0$ V, requiring negative
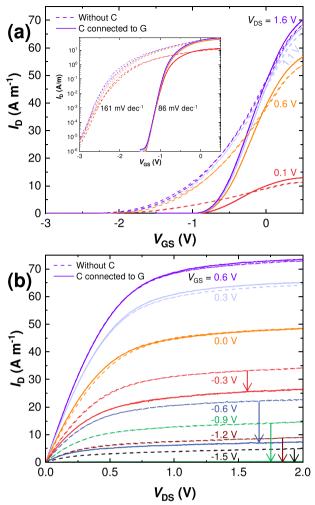
Fig. 3 The electrical characteristics of a dual-gate GESFET without the control gate (dashed lines) and with the control gate connected to the graphene gate (solid lines). The channel length $L = 1.5$ μm and width $W = 4.8$ μm. **a** The transfer curves of the GESFET where the drain current I_D (normalized by the channel width W) is measured as a function of V_{GS} at V_{DS} ranging from 0.1 to 1.6 V with a step of 0.5 V. The inset shows the same transfer curves in the semi-log scale and the corresponding subthreshold swings. **b** The output curves of the same dual-gate GESFET with I_D measured as a function of V_{DS} at V_{GS} ranging from −1.5 to 0.6 V with a step of 0.3 V.

V_{GS} to turn off, i.e., they had $V_{th} < 0$ V and operated in the depletion mode.

Figure 1 b shows the band structure of the unbiased ($V_{DS} = 0$ V) GESFET in the vertical direction at $V_{GS} = 0$ V. The Fermi level at the interface between graphene and GaAs is to a large extent pinned by the surface states of GaAs due to their large density of states (DOS). The Fermi-level pinning reduces the SBH by eV_{ss} to Φ_{B0}, where e is the elementary charge and V_{ss} is the voltage drop at the interface (the formation of the Schottky junction is illustrated in Supplementary Fig. 2). The Schottky barrier depletes the electrons in the n-type GaAs close to the interface.

The electron density in the GaAs channel is controlled by applying $V_{GS} < 0$ V which reversely biases the Schottky junction and further depletes the channel, as shown in Fig. 1c. Most of the electrons, originating from the depletion region of GaAs, fill the surface states which slightly raises the Fermi level at the surface due to the large DOS of the surface states. The remaining smaller number of electrons transfer to graphene, significantly raising the Fermi level in graphene[6,26] (equivalent to the reduction of the

work function of graphene) due to its low DOS. This decreases the SBH from the initial value Φ_{B0} to Φ_{B1}, reducing the carrier depletion in the channel. The reduction of the SBH is therefore a consequence of the limited DOS of graphene and negatively affects transistor operation.

Dual-gate GESFET

To control the SBH (i.e., the work function of graphene), a second control Al/AlO$_x$ gate stack is fabricated on top of graphene, resulting in a dual-gate GESFET shown in Fig. 2a. The graphene gate and control Al gate (C) form a capacitor in which the induced charge depends on the capacitor voltage V_{GC} rather than V_{GS}. This prevents the influence of V_{GS} on the carrier density in graphene, i.e., it prevents the filling of the electronic states in graphene by the electrons from the GaAs channel when the Schottky junction is reversely biased ($V_{GS} < 0$ V). As a consequence, the electrons originating from the depletion region in GaAs fill only the surface states, as illustrated in Fig. 2b for $V_{GC} = 0$ V. As the surface states have a very large DOS, the SBH is only slightly reduced from Φ_{B0} to $\Phi_B \approx \Phi_{B0}$, i.e., the control gate prevents the lowering of the work function of graphene and deterioration of the transistor properties. In this case, the dual-gate GESFET operates as efficiently as the MESFET with a standard metal gate, in which the SBH also does not depend on V_{GS}. The mean SBH was estimated to $\Phi_B \approx 0.75$ eV, as shown in Supplementary Figs. 3–5. Scanning electron microscopy (SEM) images of one of the fabricated dual-gate GESFETs are shown in Fig. 2d, e and its proposed electrical symbol in Fig. 2f.

Figure 3a shows the transfer characteristics of a dual-gate GESFET at different drain voltages V_{DS} when the control gate is absent (dashed lines) or connected to the graphene gate (solid lines). At positive gate voltages ($V_{GS} > 0$ V), the n-GaAs channel is fully undepleted and there is no difference in the drain current between the GESFET without and with the control gate. In the absence of the control gate, the reduction of the SBH, as the gate voltage is decreased, impedes the channel depletion. This results in a large subthreshold swing ($S_{th} = 161$ mV dec^{-1}) and very negative threshold voltage ($V_{th} = -2.1$ V). However, when the control gate is connected to the graphene gate, SBH is mainly unaffected by the decrease of V_{GS}. This depletes the channel faster compared to the GESFET without the control gate, leading to the smaller subthreshold swing ($S_{th} = 86$ mV dec^{-1}) and less negative threshold voltage ($V_{th} = -0.92$ V). In both cases (with or without the control gate), the transfer curves are quadratic at large drain voltages ($V_{DS} > V_{GS} - V_{th}$) and mainly independent of V_{DS} because the GESFET is in the saturation region. At low drain voltages (e.g., $V_{DS} = 0.1$ V), the GESFET is in the ohmic region and the drain current is much smaller. The maximum drain current $I_D = 72$ A m^{-1} was obtained at $V_{GS} = 0.6$ V which is smaller than that of commercial GaAs MESFETs with the same channel length[27]. Similarly, the extrinsic carrier mobility was only $\mu_{ext} = 162$ cm^2 V^{-1} s^{-1}. This is a consequence of the non-optimized metal contacts with the GaAs channel resulting in a large contact resistance $R_c = 6.7$ kΩ μm corresponding to the contact resistivity $\rho_c \sim 3 \times 10^{-3}$ Ω cm^2, which is much larger than that of commercial devices[28]. The transconductance, gate leakage currents, and contact resistance in the fabricated GESFETs are discussed in Supplementary Figs. 6 and 7.

Figure 3b shows the output characteristics of the same GESFET at different gate voltages V_{GS}. Similar to the transfer curves, the control gate does not make much difference if the channel is not depleted, i.e., for $V_{GS} > 0$ V. This is because the Fermi level of the graphene gate is inside the valence band in equilibrium, as shown in Fig. 1b. At positive gate voltages, the Fermi level in graphene can only shift deeper into the valence band where the DOS of graphene is large enough to suppress such shift and the increase of the SBH in the absence of the control gate. However, at negative gate voltages, the Fermi level shifts toward the Dirac
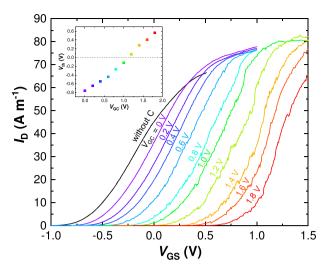
Fig. 4 The transfer curves of a dual-gate GESFET at different V_{GC} and $V_{DS} = 1$ V. The leftmost curve (black) corresponds to a GESFET in which the control gate is disconnected. Starting from the next curve (purple) and going to the right, V_{GC} increases from 0 to 1.8 V in the steps of 0.2 V. The inset shows the threshold voltage V_{th} of the GESFET (obtained from the transfer curves), which increases as V_{GC} increases and becomes positive for $V_{GC} \geq 1.2$ V. Approximately, $V_{th} = 0.76 V_{GC} - 0.83$ V.

point at which there is the minimum (zero) of the DOS of graphene. Therefore, as the gate voltage becomes more negative, the Fermi level noticeably shifts toward smaller DOS which decreases the SBH in the absence of the control gate. For this reason, as V_{GS} decreases, the drain current decreases faster in the presence of the control gate, as indicated by the arrows in Fig. 3b. Once the Fermi level crosses the Dirac point (which happens at $V_{GS} \sim -0.6$ V in Fig. 3b) and enters the conduction band, the further decrease of V_{GS} shifts the Fermi level toward larger DOS, which suppresses the Fermi level shift and the reduction of the SBH in the absence of the control gate. This suppresses further split between the drain currents in the absence and presence of the control gate. However, this effect cannot be seen in Fig. 3b because the channel was depleted by reducing V_{GS} below -0.6 V in the presence of the control gate.

The requirement to connect the control gate to the graphene gate in order to operate a GESFET as efficiently as a conventional MESFET is necessary only in the GESFETs in which the Fermi level is close to the Dirac point (e.g., as in the GESFET in Fig. 3). However, if the Fermi level is deep into the valence band, the DOS of graphene is large enough to suppress the changes of the SBH with V_{GS}. Supplementary Figures 8 and 9 show the electrical characteristics of such a GESFET. It exhibits almost the same subthreshold swing as the conventional MESFET with a Ti/Au gate and turns off before the decrease of V_{GS} shifts the Fermi level close to the Dirac point of graphene. Such GESFETs typically exhibit the smallest subthreshold swing ($S_{th} = 65$ mV dec^{-1} was obtained in this case).

In contrast to a standard MESFET, the work function of a graphene gate in a GESFET can be controlled by the control gate, which is illustrated in Fig. 2c and experimentally confirmed in Supplementary Fig. 4b. When a voltage between the control gate and graphene gate is applied, e.g., $V_{GC} > 0$ V as in Fig. 2c, the most of this voltage drops on the oxide of the control gate. However, due to the limited DOS of graphene, there is also a voltage drop V_q between the metal contact of the graphene gate and graphene (usually modeled by the quantum capacitance). This lowers the Fermi level in graphene by eV_q and consequently increases the SBH by the same amount to $\Phi_B + eV_q$. Therefore, the increase of V_{GC} (i.e., the decrease of the control gate potential V_C below the

potential of the graphene gate V_G), increases the threshold voltage V_{th} because it increases the depletion of carriers in the channel and decreases the drain current.

The influence of the control gate on the threshold voltage is illustrated in Fig. 4 which shows that the increase of V_{GC} shifts the transfer curve, i.e., the threshold voltage V_{th}, to larger gate voltages. By increasing V_{GC} from 0 to 1.8 V, the threshold voltage was increased from -0.76 to 0.56 V, as shown in the inset of Fig. 4 (the corresponding leakage currents are shown in Supplementary Fig. 10). This means that the control gate of the GESFET can be used to change the transistor operation from the depletion to the enhancement mode, representing an advantage with respect to the conventional MESFETs. The latter can only operate in one mode after the fabrication, typically the depletion mode. In this case, V_{GS} of the opposite sign of V_{DS} is required to fully deplete the channel (e.g., in an n-type MESFET, $V_{GS} < 0$ V is required at $V_{DS} > 0$ V). That limits the application of such MESFETs in digital electronics because the opposite signs of V_{GS} and V_{DS} prevent the direct cascading of transistors which is required in logic gates.

Logic gates with dual-gate GESFETs

The presented depletion mode GESFETs can overcome the inability of conventional depletion mode MESFETs and HEMTs to be cascaded in logic gates. This is illustrated in Fig. 5 which shows the static voltage transfer characteristics of a depletion-load inverter in which the threshold voltage of the driver GESFET was controlled by the voltage of its control gate. Both GESFETs have a negative threshold voltage when the control gate is connected to the gate ($V_{GC} = 0$ V). A negative threshold voltage is required for the load transistor to keep it in the on state when its gate is connected to its source. However, a negative threshold voltage of the driver transistor results in a negative switching threshold ($V_M = -0.62$ V) of the inverter at a positive voltage supply $V_{DD} = 2.5$ V, as shown in Fig. 5. In this case, the logic zero corresponds to a negative voltage at the input ($V_{IN} < V_M$) even though the output voltage is always positive (0 V $< V_{OUT} < V_{DD}$). In order to shift the switching threshold to positive voltages, $V_{GC} > 0$ V is required, as discussed in Fig. 4. The increase of the switching threshold V_M with the increase of V_{GC} is demonstrated in Fig. 5b. For example, the switching threshold was shifted to $V_M = 0.3$ V at $V_{GC} = 2$ V.

In realistic applications, setting $V_{GC} > 0$ V requires a voltage source to be connected between the gate and the control gate of the driver transistor (see Supplementary Fig. 11), which is impractical because this would require each driver GESFET to be connected to a separate voltage source in an integrated circuit (IC). This problem could be overcome simply by connecting the control gates of all driver GESFETs in the IC to a negative power supply voltage $-V_{CC} < 0$ V, as shown in Fig. 5a, thereby ensuring $V_{GC} = V_{IN} + V_{CC} > 0$ V for a large V_{CC}. This is demonstrated in Fig. 5b in which the switching threshold V_M was increased with the increase of V_{CC}. At low V_{CC}, the switching threshold was more negative compared to $V_{GC} = 0$ V (e.g., $V_M = -1$ V at $V_{CC} = 0.5$ V) because a negative input voltage makes $V_{GC} < 0$ V when V_{CC} is small. However, as V_{CC} was increased, V_M increased too and it reached $V_M = 0.7$ V at $V_{CC} = 2$ V.

The use of a negative supply $-V_{CC}$ allows to shift the switching threshold of the investigated logic gates to positive voltages which is required in practical applications. However, larger shifts are obtained at larger V_{CC}, which leads to the larger voltage drop $V_{GC} = V_{IN} + V_{CC}$ on the oxide of the control gate. This could result in the oxide breakdown when $V_{IN} = V_{DD}$ (logic 1 at the input). For example, if the present inverters were to be cascaded, $V_M = V_{DD}/2 = 1.25$ V, i.e., $V_{CC} > 2$ V at $V_{DD} = 2.5$ V would be required. This problem could be mitigated by simply reducing V_{DD}. However, this was not possible here due to the limited transconductance g_m of the GESFETs (typically, $g_m/W < 100$ S m^{-1}) because of the large contact resistance of the used non-optimized contacts. As an alternative, a gate oxide
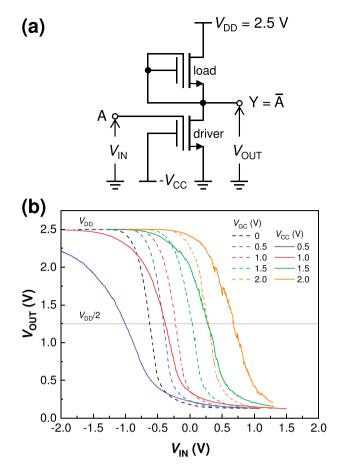
Fig. 5 **A depletion-load inverter with an externally controlled switching threshold. a** A schematic of a depletion-load inverter realized with two dual-gate GESFETs. The top GESFET (load) is kept in the on state by having both gates connected to the source. The bottom GESFET (driver) has the control gate connected to a negative power supply voltage $-V_{CC}$ so that its gate (i.e., the input voltage V_{IN}) is always at the higher potential. This shifts the threshold voltage of the driver to positive values if V_{CC} is sufficiently large. **b** The static voltage transfer characteristics of the inverter for different V_{GC} (the inverter shown in Supplementary Fig. 11) and V_{CC} (the present inverter). The switching threshold V_M of the inverter is the input voltage at which $V_{OUT} = V_{DD}/2$. Logic 0 at the input corresponds to $V_{IN} < V_M$ and logic 1 to $V_{IN} > V_M$. The corresponding voltage gain is shown in Supplementary Fig. 12.

of a similar thickness but larger relative dielectric constant (e.g., HfO_2) could be used to increase the transconductance. Nevertheless, all investigated inverters exhibit an over-unity voltage gain, as shown in Supplementary Fig. 12.

Frequency mixers with dual-gate GESFETs

A control gate could also be used as the transistor gate in its own right. Supplementary Figure 13 shows the electrical characteristics of a dual-gate GESFET in which the control gate voltage V_{CS} is used to modulate the drain current at a fixed V_{GS}. In this case, the depletion of the GaAs channel is solely controlled by the change of the SBH. A transistor with two equally functioning gates could be used to simplify more complex electronic circuits by reducing their component count and therefore the space they take in an IC. For example, a frequency mixer typically consists of a nonlinear device (a diode or transistor) whose nonlinearity is exploited to mix the signals at the two inputs of the mixer[1]. In an ambipolar resistive mixer based on GFETs, the inputs are often connected to the gate of a GFET via resistors[29]. The resistors take a valuable space in an IC and also lead to an unwanted input power
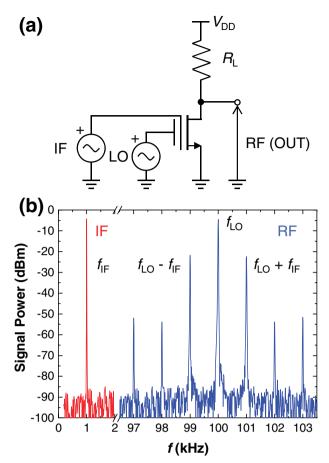

Fig. 6 **An upconverting frequency mixer based on a dual-gate GESFET. a** A schematic of the mixer. The output RF signal was obtained by mixing the input IF and LO signals. **b** The power spectrum of the input IF and output RF signals. The input IF signal is represented with a sine wave at a frequency $f_{IF} = 1$ kHz, while the LO frequency is $f_{LO} = 100$ kHz. The output RF signal comprises a signal at f_{LO}, lower sideband at $f_{RF} = f_{LO} - f_{IF} = 99$ kHz, higher sideband at $f_{RF} = f_{LO} + f_{IF} = 101$ kHz, and other harmonics of much smaller power. The conversion loss of 17.5 dB represents a power difference between the IF and RF sideband signals. The corresponding waveforms are shown in Supplementary Fig. 14.

dissipation (because the resistors create a current path between the inputs). Such frequency mixers can be simplified by a dual-gate GESFET in which the inputs are directly connected to its gates thereby completely eliminating the input resistors and the corresponding power dissipation.

Figure 6 shows a simple upconversion mixer that mixes the baseband data signal at the intermediate frequency (IF) with the high-frequency signal of the local oscillator (LO). The output radio-frequency (RF) signal consists of the IF signal shifted to the LO frequency. The load resistor R_L was chosen to fit the resistance of the GESFET at the DC operating point, so that the DC voltage at the output is $V_{DD}/2$. The conversion loss of the mixer is 17.5 dB, which is comparable to that of the best graphene mixers at such low LO power[30], even though the present mixer was measured in a DC probe station with an externally connected load resistor. The same mixer can also downconvert the RF signal if the RF and IF ports are swapped, see Supplementary Fig. 15. Further investigations of GESFET-based mixers should be performed to reach the performance of the conventional single-gate mixers.

DISCUSSION

We demonstrated single and dual-gate GaAs FETs with a monolayer graphene gate. In both types of GESFET, the conductivity of the GaAs channel was modulated by changing the width of the depletion layer of the Schottky junction formed between the graphene gate and GaAs channel. Dual-gate GESFETs had an additional control gate which was fabricated on top of the graphene gate and used to control the threshold voltage of the GESFETs. The control gate sets the Fermi level of the graphene gate and therefore the SBH, which in turn sets the threshold voltage of the GESFETs. This allowed to change the threshold voltage of the dual-gate GESFETs from ~ −0.8 V (depletion mode) to ~0.6 V (enhancement mode) by changing the control gate voltage by 1.8 V.

The control of the threshold voltage can be performed independently on each dual-gate GESFET in a circuit. This was demonstrated by a depletion-load inverter in which the driver GESFET was operated in the enhancement mode, resulting in a positive switching threshold of the inverter. The control gate can also be connected to the graphene gate to reduce the subthreshold swing, or operated independently to provide an additional functionality. The latter was demonstrated by realizing simple frequency mixers in which two different signals were applied to each of the gates.

The presented technology can be applied to any other semiconductor material (e.g., Si, InGaAs, and InP) which makes a Schottky junction with graphene[31]. The figures of merit of the GESFETs are expected to be mainly affected by the choice of the channel material and their dual-gate configuration. For example, the operating voltage and power dissipation are directly related to the bandgap of the channel material. However, slightly larger power dissipation is expected in GESFETs (with respect to MESFETs) because they have the additional control gate resulting in an additional leakage current at large operating voltages. Similarly, the device speed (or bandwidth) is directly related to the carrier mobility in the channel, but we expect that the ultimate speed will be limited by the resistance of the graphene gate at very short gate lengths ($L < 100$ nm).

The demonstrated dual-gate GESFETs with a graphene gate pave the way for the development of FETs in which the threshold voltage can be varied almost arbitrarily after fabrication (i.e., during device operation) thus satisfying the demand of different range of applications.

METHODS

Fabrication of the transistor channel

A stack of semi insulating AlGaAs, lightly n-doped GaAs (~10^{17} cm^{-3}), and n$^+$-doped GaAs (>10^{18} cm^{-3}) was grown by MBE on an intrinsic (100) GaAs wafer. Electron-beam (e-beam) lithography (Raith eLINE at 10 kV) was used to define the mesa structure. A solution of H_3PO_4 was used to remove n$^+$-GaAs above the transistor channel. Source and drain contacts were patterned by e-beam lithography. The contacts comprising a stack of Au/Ge/Ni/Au (20/75/17/100 nm) were deposited by e-beam evaporation (at a base pressure of 10^{-6} mbar) followed by annealing in an Ar/H$_2$ atmosphere (for 20 s at 325 °C).

Fabrication of the graphene gate

Graphene grown by CVD[32,33] was directly transferred on the chip and then patterned by e-beam lithography to define the gate Schottky junction (with a channel length 1 μm $< L <$ 15 μm). O$_2$ plasma was used to remove the excess graphene. The gate contact was patterned by e-beam lithography on graphene outside the channel area. It consisted of pure Au (100 nm) deposited by e-beam evaporation.

Fabrication of the control gate

The dual-gate GESFETs were fabricated from standard (single-gate) GESFETs after they were electrically characterized. The control gate was patterned by e-beam lithography on graphene covering the channel. It consisted of Al (100 nm) evaporated by e-beam lithography. Al oxidized in air forming a thin (~4 nm) native layer of AlO$_x$ on all surfaces of Al, including the surface in contact with graphene. This formed a control Al/AlO$_x$ gate stack on top of graphene with a gate capacitance of $C_{ox} = 1.4$ μF cm^{-2}.[34,35] To demonstrate that the observed effects are not related to a possible direct contact between Al and the GaAs channel, we also fabricated reference devices without the graphene gate, see Supplementary Fig. 16.

Device characterization

The electrical measurements were performed in FormFactor probe stations Summit 11000 and EP6 in air ambient. Keithley 2600B series source-measure units, a function generator Tektronix AFG 3022B, and an oscilloscope Keysight DS09064A were used in electrical characterizations of the realized GESFETs, inverters, and mixers. The capacitance–voltage (CV) measurements were performed using Keithley 4200A-SCS parameter analyzer with a CV unit 4215-CVU. The SEM characterization was performed in Raith eLINE at 10 kV.

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ACKNOWLEDGEMENTS

AUTHOR CONTRIBUTIONS

R.S. designed the study, directed the project, performed data analysis, and wrote the manuscript. L.A. fabricated the devices and performed the electrical measurements and data analysis. A.T. and A.F. grew GaAs/AlGaAs heterostructures by MBE and S.S. provided experimental support. A.Z. grew graphene by CVD. All authors reviewed the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-022-00302-y.

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