Article

Origin of the Temperature Dependence of Gate-Induced Drain Leakage-Assisted Erase in Three-Dimensional NAND Flash Memories

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Abstract: Through detailed experimental and modeling activities, this paper investigates the origin of the temperature dependence of the Erase operation in 3D NAND flash arrays. First of all, experimental data collected down to the cryogenic regime on both charge-trap and floating-gate arrays are provided to demonstrate that the reduction in temperature makes cells harder to Erase irrespective of the nature of their storage layer. This evidence is then attributed to the weakening, with the decrease in temperature, of the gate-induced drain leakage (GIDL) current exploited to set the electrostatic potential of the body of the NAND strings during Erase. Modeling results for the GIDL-assisted Erase operation, finally, allow not only to support this conclusion but also to directly correlate the change with temperature of the electrostatic potential of the string body with the change with temperature of the erased threshold-voltage of the memory cells.

Keywords: NAND Flash memory; 3D array; gate-induced drain leakage; semiconductor device modeling

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1. Introduction

Three-dimensional NAND Flash technology represents the leading solution for non-volatile data storage [1–5] thanks to its very low cost per bit, which is the direct outcome of its ability to reach an extremely high storage density with a cost-effective process [6–9]. One of the most relevant innovations behind that capability is the integration of the 3D memory array over an n^+-doped polysilicon source plate on top of the CMOS peripheral circuitry [8,10–12]. In spite of the benefits of this integration scheme, the lack of any connection of the NAND strings to a p-doped bulk contact makes the exploitation of gate-induced drain leakage (GIDL) at the string edges the only viable option to provide the string body with the holes needed during an Erase operation. GIDL-assisted Erase has been the object of detailed investigations in the past, which successfully highlighted its time dynamics through both TCAD and compact models [10,13,14]. However, some aspects of this operation, such as its temperature (T) dependence, still require better explorations, especially for T values ranging from room temperature (RT) down to the deep-cryogenic regime ($T < 50$ K). Indeed, cryogenic operation of 3D NAND Flash memories has been recently reported as a promising candidate for future high-performance applications [15–19]. Nevertheless, to date, it is still not entirely clear what impact temperature has on the processes underlying the performance and reliability of memories when they are operated at cryogenic temperatures. The GIDL-assisted Erase of 3D NAND Flash memories is an operation that leverages on a large number of physical processes. As each of these features

a specific T dependence, the identification of the main process controlling the T activation of the Erase is a mandatory prerequisite to extend the reliable operation of devices out of nominal T conditions. Although it is known that the GIDL current features a positive T activation [10,20–23], such dependence has not been explored down to cryogenic temperatures. Moreover, it remains unclear if the GIDL current is the dominant T-activated phenomenon during Erase. Indeed, a recent work put forward the hypothesis that it is the emission of electrons from the charge-trap layer that determines the main thermal activation of Erase [16].

In this paper, we experimentally investigate, for the first time, GIDL-assisted Erase in 3D NAND Flash arrays over an extremely wide T interval from 300 K down to the cryogenic regime and on both charge-trap (CT)- and floating-gate (FG)-based memory cells. We provide clear experimental evidence showing that Erase becomes more demanding in terms of the voltage needed to reach a target cell threshold voltage (V_T) when T is reduced. The observation that the nature of the cell storage layer does not impact the T dependence of the Erase operation allows the identification of the main factor responsible for the observed slow-down in the weakening of the GIDL current when T decreases. Detailed modeling results allow to confirm this view and to correlate the T-induced change of the electrostatic potential of the string body during an Erase pulse with the T-induced change of the erased V_T of the memory cells.

2. Experimental Section

The samples investigated in this work are 3D NAND Flash array test elements based on charge-trap (CT) and floating-gate (FG) storage with, respectively, $N_{WL} = 10$ and $\gg$10 vertically stacked wordline (WL) layers. To offer the opportunity to monitor either a single string (SS) or many strings (MS) in parallel, the contacts of some of the bitlines (BL) are independently available for biasing, while those of some others (a few thousands) are short-circuited, as schematically shown in Figure 1a.

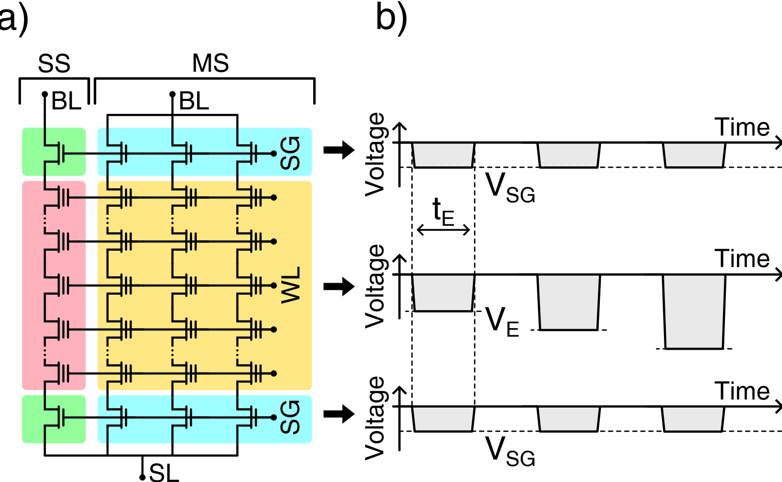


Figure 1. (**a**) Schematic description of the test elements investigated in this work (only some of the WLs are depicted in the scheme). (**b**) Voltage waveforms applied to the array WL and SG to achieve ISPE, with grounded SL and BL (t_E is the duration of the Erase pulses).

To explore the Erase operation over a wide T interval ranging from 300 K to about 15 K, the investigated samples were encapsulated in a package and mounted in a cryostat, as described in [24]. An Incremental Step Pulse Erasing (ISPE) scheme was used, consisting of negative voltage pulses of increasing amplitude V_E applied to the array WLs and negative voltage pulses of constant amplitude V_{SG} applied to the select-gate (SG) lines, with grounded BLs and sourceline (SL) (see Figure 1b). Note that the application of negative pulses to the array WL and SG is perfectly equivalent to the application of positive pulses to the BL, SL, and SG; although the latter solution represents the standard way to perform

the Erase operation in 3D NAND arrays, the former allows to simplify the experimental setup needed to carry out all operations on the investigated test elements. All cells were Erased well below their neutral state, i.e., the state in which no charge is present inside the storage node.

After each ISPE pulse, the BL current vs. WL voltage ($I_{BL} - V_{WL}$) trans-characteristic of single cells was measured, with all the other WLs under the pass condition, positively biased SG and BL, and grounded SL. When I_{BL} is read through an SS contact, the curve obtained via this measurement allows the extraction of the V_T of a single cell in the sub-block under test. When I_{BL} is read through an MS contact, instead, the curve provides an equivalent V_T of many cells in parallel. In both cases, V_T is defined as the V_{WL} value leading to a fixed I_{BL} value well below the minimum saturation level of the string current at $T = 15$ K. An example of the $I_{BL} - V_{WL}$ trans-characteristic resulting from an MS measurement at different T values is reported in the inset in Figure 2a for a CT-based sample, highlighting the I_{BL} threshold value. The rightward shift in the trans-characteristic with the reduction in T results in the typical increase in V_T observed in all MOS devices down to the cryogenic regime [25–31]. The change in V_T with respect to the 300 K value is reported as a function of T in Figure 2a along with data from 50 SS measurements. Clearly, the trend obtained from the MS measurement is very similar to the average trend obtained from the latter, confirming that MS measurements allow us to achieve results representative of single cell behavior and to avoid the statistical variability and noise typical of SS results.

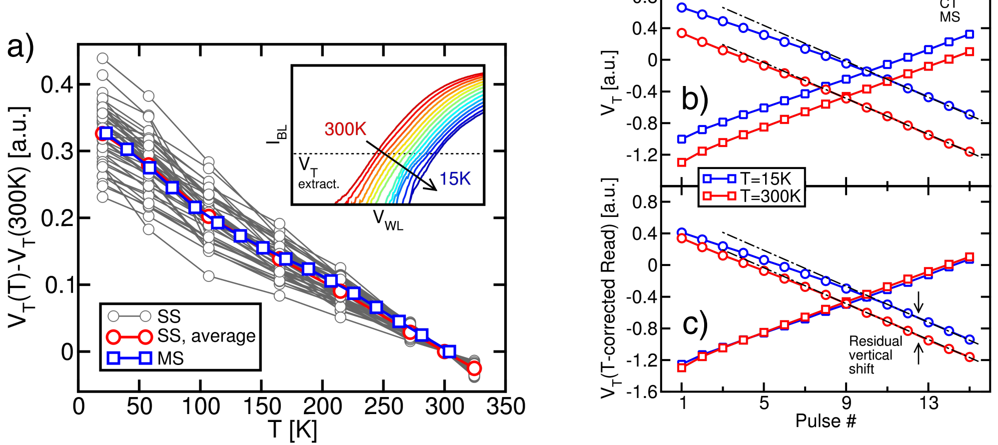
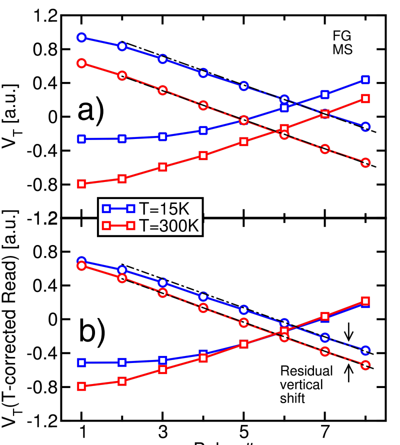


Figure 2. (**a**) T-induced change of cell V_T, with respect to 300 K. Data are reported for 50 SS and 1 MS measurements on CT-based cells. The average of the SS measurements is also highlighted. The inset shows a representative example for the $I_{BL} - V_{WL}$ trans-characteristic of the MS structure, at different T values (a log scale is used for I_{BL}). (**b**) V_T evolution with the ISPE pulse number at $T = 300$ K and 15 K, as obtained from MS measurements on CT-based samples (circles). ISPP results are also shown (squares). (**c**) Same as in (**b**) but with the T dependence of the Read operation subtracted from the V_T values at $T = 15$ K. Dashed black lines are guides to the eye. All the voltages reported in this work were normalized to the same arbitrary constant.

Figure 2b (circles) shows the V_T evolution with the ISPE pulse number, as obtained from an MS measurement on a CT-based sample at $T = 300$ K and 15 K (both Read and Erase operations were carried out at the same T). Although V_T features a linearly decreasing trend with a T-independent slope, the curve at 15 K is significantly above the one at 300 K. This can be only partially attributed to the T dependence of the V_T value resulting from a Read operation (see Figure 2a). Figure 2c shows, in fact, that the 15 K curve remains clearly above the 300 K one even when the T dependence of the Read operation is subtracted from its V_T values (this correction was performed by vertically shifting the transients measured at $T = 15$ K by a quantity equal to the T-induced shift in the neutral V_T). This demonstrates that cells become harder to Erase with the reduction in T, in agreement with what was

reported in [16,17] where data were gathered down to 77 K. Cell programming, instead, is not made significantly harder by the reduction of T: Figure 2b (squares) shows, in fact, that when an Incremental Step Pulse Programming (ISPP) scheme is adopted [32,33], the V_T transient at $T = 15$ K is still above that at 300 K but overlaps with it when the T dependence of V_T is accounted for. This indicates that the transfer of negative charge from the channel to the storage layer of the memory cells during Program remains almost the same irrespective of T, meaning that the T dependence of Fowler–Nordheim tunneling is very weak [16,17].

Figure 3a,b proves that the same evidence gathered on CT-based samples also appears for FG-based devices. Note that the discrepancy present in the ISPP curves in Figure 3b for the first three pulses comes from the different initial placements of the cells at T = 300 K and 15 K. However, when constant-current operation is reached, such discrepancy is removed as the result of the convergent nature of the ISPP scheme [33]. The fact that the worsening of the Erase performance appears on FG-based samples is particularly important because it shows that the T dependence of the Erase operation in 3D NAND Flash arrays does not trace back to something specifically related to the storage layer. For instance, it cannot be ascribed to the limited number of microscopic defects storing charge in the CT layer and neither to the T dependence of their time constant for carrier capture/emission [34–37]. Nor it is to be traced back to the fact that in the case of CT samples, cell Erase is the result of both electron emission from the storage layer and hole injection in the opposite direction [16,17,38]. In this regard, moreover, it is worth noting that the quantum–mechanical tunneling of holes from the channel to the storage layer of the memory cells is surely involved in the Erase operation of CT-based samples, being the only physical mechanism able to move V_T below its neutral value. However, the T dependence of this mechanism is expected to be very weak, in analogy to the case of electron tunneling from the channel to the storage layer during Program. Therefore, neither the structure of the storage layer nor the physical processes involved in the charge transfer can be considered as the origin of the T dependence of the Erase operation. Also, because such T dependence is similarly observed for the largely different string lengths of the investigated CT and FG samples, that origin can neither be related to nonuniformities in the electrostatic potential along the string body during the Erase pulses, which may arise from electron/hole capture and emission at the polysilicon grain boundaries [39–41].



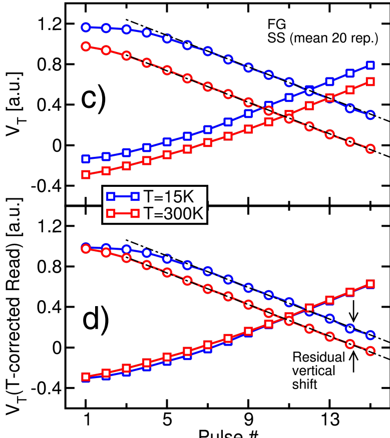


Figure 3. (**a**,**b**) Same as in Figure 2b,c, but for FG-based cells. (**c**,**d**) Same as in Figure 2b,c but for an average of 20 SS measurements on FG-based cells.

Finally, Figure 3c,d shows that the same trends obtained through the MS measurements were obtained through the average of SS measurements as well, confirming that the parallel Read of many memory cells does not introduce any artifact into the observed phenomenology.

3. Modeling

3.1. Physical Picture

A common origin for the T dependence of the Erase operation in CT- and FG-based arrays can be traced back to the change with T of the GIDL current setting the string electrostatic potential during the Erase pulses. In particular, a weakening of the GIDL current at the string edges with the reduction of T may easily explain the lower effectiveness of the Erase operation at $T = 15$ K with respect to 300 K appearing from all the results presented in Section 2. That weakening, in fact, makes the electrostatic potential in the string body (V_B) during the Erase pulses more negative at the former than at the latter T. For the same negative V_E applied at the cell WL, this results in a voltage drop over the cell gate stack that is lower at 15 K than at 300 K, making the Erase operation less effective.

To better visualize the impact of V_B on the Erase operation, Figure 4 schematically shows the band diagram along the gate stack of a memory cell during an Erase pulse at $T = 15$ K and 300 K for the same applied V_E. Direct reference is made to the ISPE scheme adopted in Section 2 and, in particular, to the part of this scheme during which V_T displays a linear decrease with the Erase pulse number. When this condition is reached, each ISPE pulse gives rise to the same change in charge in the cell storage layer. This means that the average current flowing through the cell tunnel dielectric and the average voltage drop over this dielectric (V_{tun}) remain constant from one Erase pulse to the next. Moreover, under the assumption that the current vs. voltage characteristic of the tunnel dielectric during Erase does not change with T (in the case of dominant tunneling processes, the T dependence of such characteristic should be very weak, as discussed in the previous Section), the average value of V_{tun} must be the same at $T = 15$ K and 300 K. The change in V_B (δV_B) between the two T arising from a different GIDL current at the string edges, then, has to turn into an equal change in the electrostatic potential in the cell storage layer ($\delta V_{sl} = \delta V_B$). This results in less positive charge in the cell storage layer at $T = 15$ K, meaning that the Erase operation is less effective at low temperatures.

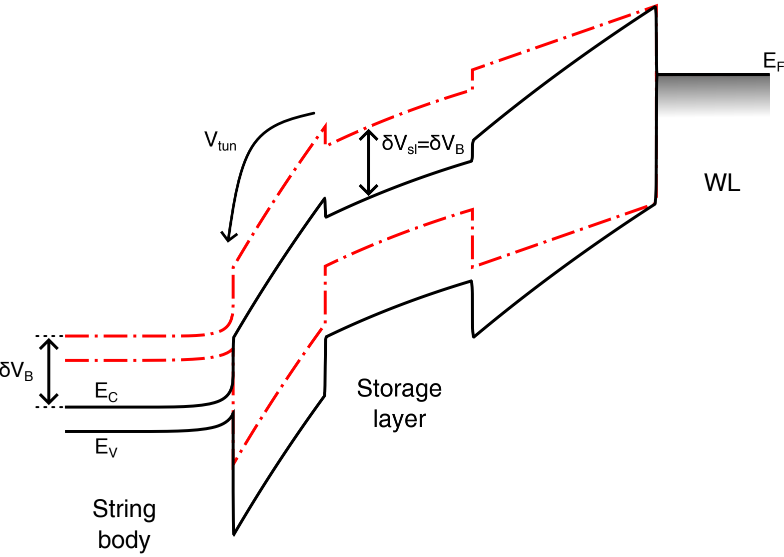


Figure 4. Schematic band diagram along the gate stack of a CT-based memory cell during an ISPE pulse at $T = 300$ K (solid black curves) and 15 K (dashed red curves). E_C and E_V are, respectively, the conduction band and valence band edge of the materials. E_F is the Fermi level in the metal WL. For the sake of simplicity, the tunnel–dielectric stack is considered as a single-layer dielectric.

To determine the change in the erased cell V_T arising from the T-induced δV_B, the following approximated expression for V_{tun} during an Erase pulse can be used (the expression generalizes what was reported in [42]):

$$V_{tun} = -\alpha_G(V_E - V_B - \Delta V_T + \beta), \quad (1)$$

where ΔV_T is the cell V_T shift from the neutral value, α_G is the capacitive coupling ratio between the WL and the storage layer, and β is a constant accounting for the built-in voltage drop in the device. From (1), it is evident that a T-induced δV_B must be compensated by an equal and opposite change in ΔV_T to maintain the same V_{tun} during the ISPE operation. A negative δV_B during the Erase pulses between $T = 15$ and 300 K gives rise, then, to a higher erased V_T at the former T. This not only explains the experimental evidence in Figures 2c and 3b,d but also allows us to state that the magnitude of the vertical shift in the Erase transients, once corrected by the T dependence of the Read operation, quantitatively corresponds to the T-induced $|\delta V_B|$ during the ISPE pulses at $T = 15$ K and 300 K.

3.2. Simulation Results

To check the validity of the physical picture presented in Section 3.1 and confirm the conclusions drawn from (1) on the equality of the T-induced change in ΔV_T and V_B during an ISPE operation, we relied on the compact model for GIDL-assisted Erase in CT-based 3D NAND Flash strings presented in [13,14]. The model was originally developed to carefully reproduce the time dynamics of V_B, I_{BL}, and V_T during a single Erase pulse and was here extended to reproduce the entire ISPE scheme. Figure 5 shows the lumped-parameter circuit at the heart of the model, which includes a module reproducing the V_B dynamics in the presence of the GIDL current (light blue region) and a module reproducing the dynamics of charge transfer and storage in the gate stack of the cells (yellow region). In the circuit, I_{GIDL} is the GIDL current providing the string with the holes needed to fix V_B during the Erase pulse. I_h represents the total hole current flowing from the channel to the WL of a memory cell. A fraction of this current results in holes trapped in the cell storage layer ($I_{h,t}$), and another fraction results in holes recombining with stored electrons ($I_{h,r}$) (all the remaining current corresponds to holes reaching the WL and not contributing to cell Erase [43]). I_e is the total current arising from the release of electrons from the storage layer to the channel of the memory cell. Details about the functional form of the previously mentioned currents are reported in [14], along with the physical meaning of all the capacitive terms in the model. As a final remark, note that a negative WL voltage V_E with grounded BL was assumed for Figure 5 to keep the same voltage convention as used in Sections 2 and 3.1 (differently from [13,14], where a positive voltage was applied to the BL with grounded WL).

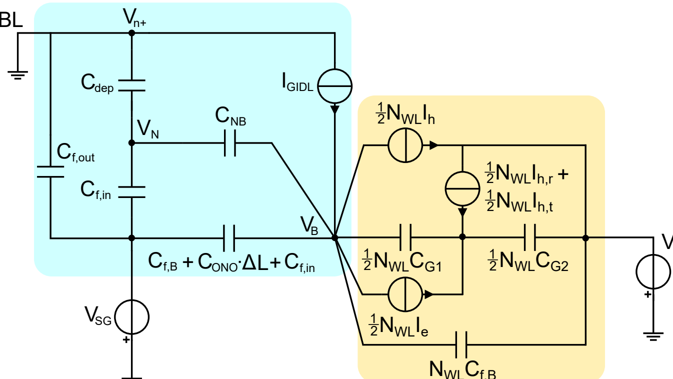


Figure 5. Compact model for GIDL-assisted Erase in CT-based 3D NAND Flash strings, adapted from [13,14]. The light-blue region corresponds to the part of the model reproducing the V_B dynamics in the presence of the GIDL current, while the yellow region corresponds to the part of the model reproducing the dynamics of charge transfer and storage in the gate stack of the cells. Note that only half of the string is considered in the model thanks to its symmetry.

Table 1 shows the parameters of the template NAND string considered in this compact model, matching that used in [13,14]. Trapezoidal pulses were assumed in the simulations, with rise/fall time and plateau duration equal to 10 µs and 1 ms, respectively. V_E was set to -10 V in the first pulse and then increased by $V_s = -0.5$ V per pulse. To address the

dependence of the V_T transient on T, the I_{GIDL} characteristics were scaled by a factor γ moving from 300 K to a lower T value (no other parameter was changed in the simulations when changing T). This factor was obtained from results in the literature collected on planar bulk MOSFETs [44,45], reported in the inset in Figure 6. In this regard, it is worth noting that non-negligible differences exist between the GIDL phenomenology in planar bulk MOSFETs and thin-channel cylindrical NAND strings: In the former devices, in fact, the GIDL current arises from vertical band-to-band tunneling within the drain junction of the transistor [46–49]. In the latter, instead, the band-to-band tunneling process occurs along the longitudinal direction at the n^+ edges of the string due to the weak band bending achievable in the radial direction [13,50,51]. Although some differences may in principle also exist in the T dependence of the GIDL current of the two types of devices, we relied on the available data on MOSFETs owing to the lack of available results on NAND strings. A direct exploration of the GIDL current vs. voltage characteristics in NAND strings, in fact, is precluded by the floating body and bipolar effects coming into play due to the n^+ contacts at both the string edges [50,52–55]. With this caveat, Figure 6 reports the I_{GIDL} vs. V_B characteristics assumed in our compact model simulations. Note that a quantitative match between the experimental data and model was outside of the scope of this work, which instead highlights the impact that the T-induced change in the GIDL current has on the resulting Erase transient. For this reason, we chose not to introduce any other T dependence in the compact model. Moreover, the simulation results remained valid regardless the specific T dependence of the GIDL current, which only determines the quantitative value of δV_B.

Table 1. String parameters assumed in our compact model simulations. N_D^B and $N_D^{BL} = N_D^{SL}$ are, respectively, the donor doping concentrations of the string channel and of the upper and lower n^+ regions. L_{WL}, L_{SG}, and L_S are the WL, SG, and WL spacing lengths. ϕ_m is the WL work function; r_f, t_{Si}, and t_{WL} are the filler oxide, channel, and WL thicknesses in the radial direction. $t_{O1}/t_N/t_{O2}$ are the thicknesses of the oxide/nitride/oxide stack used as gate dielectric.

N_{WL}	10	$L_{WL} = L_{SG}$	50 nm
L_S	50 nm	r_f	17.5 nm
t_{Si}	10 nm	$t_{O1}/t_N/t_{O2}$	4/4/4.5 nm
t_{WL}	40 nm	$N_D^{BL} = N_D^{SL}$	$5 \cdot 10^{19}$ cm^{-3}
N_D^B	10^{15} cm^{-3}	ϕ_m	4.8 eV

Figure 7a shows the simulated time evolution of V_B during some of the pulses of the ISPE scheme at $T = 300$ K and 15 K. The results reveal, first of all, that during each Erase pulse V_B displays a rapid drop, followed by a relevant rise during the first front of the pulse and then a slow growth during the pulse plateau (see [13,14] for further details on this trend). The V_B transient, additionally, displays just a very weak dependence on the pulse number. In agreement with the physical picture discussed in Section 3.1, moreover, V_B is more negative at $T = 15$ K than at 300 K. This is a direct consequence of the weakening of I_{GIDL} at the former T, which introduces the only T dependence in the simulations. In this regard, Figure 7b shows that the simulated I_{BL}, which corresponds to I_{GIDL} soon after the pulse plateau, spans the same values at both temperatures. This is, in the end, expected from the negative feedback setting V_B as a result of V_E and I_{GIDL} [13,14] and shows that δV_B during the Erase pulse nearly matches the horizontal shift in the curves in Figure 6 at the current levels involved in Figure 7b. As a final remark, note that Figure 7b also shows that the hole flow from the channel to the storage layer of the memory cells represents the dominant Erase mechanism in our simulations, making I_h much higher than I_e.

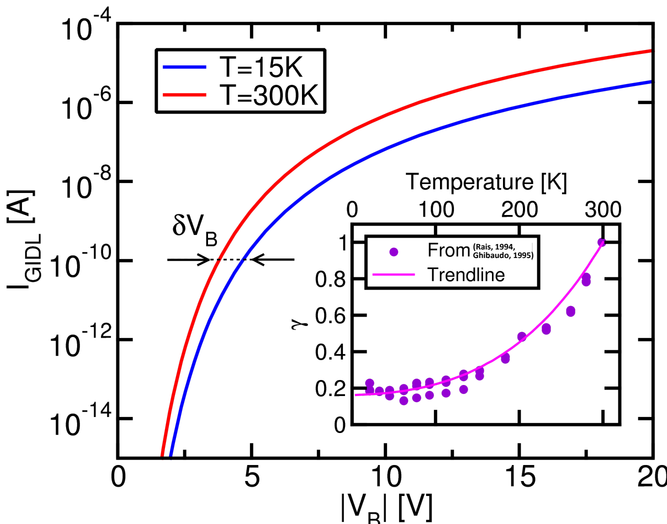


Figure 6. I_{GIDL} vs. V_B characteristics assumed in the compact model simulations at $T = 300$ K and 15 K. The inset shows the factor γ determining the decrease in I_{GIDL} with the reduction of T from 300 K, as obtained from experimental data collected on planar bulk MOSFETs [44,45].

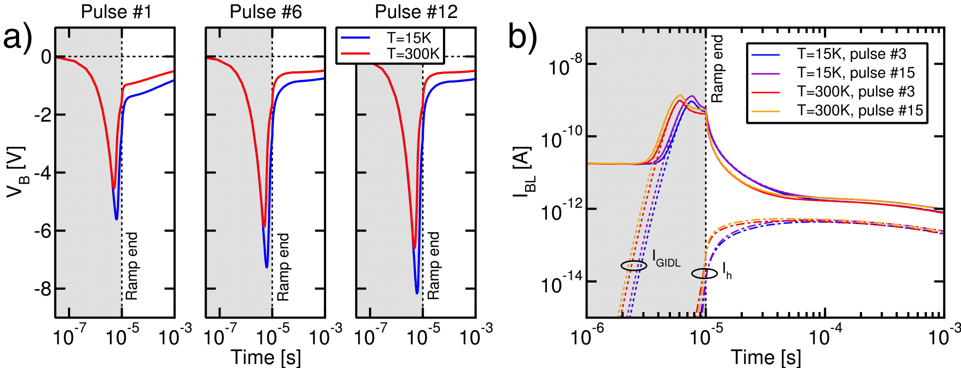


Figure 7. (**a**) Simulated V_B transient during ISPE pulses at $T = 300$ K and 15 K. The grey and white regions correspond, respectively, to the pulse front and plateau. (**b**) Simulated I_{BL}, I_{GIDL}, and I_h during two Erase pulses of the ISPE scheme. The grey and white regions correspond, respectively, to the pulse front and plateau.

The ΔV_T transients resulting from the compact model simulations are reported in Figure 8a. A linear trend with the pulse number clearly appears, in agreement with the fundamentals of the ISPE scheme. Additionally, in agreement with the experimental observations reported in Figures 2c and 3b,d, the Erase operation is less effective at $T = 15$ K than at 300 K. Once again, it is worth remarking that this result was obtained with our compact model through a weakening of the GIDL current only, with no thermal activation of the charge flows through the cell tunnel dielectric during the Erase pulses. Figure 8b demonstrates that the vertical shift in the ΔV_T transients at different T values well matches the corresponding values of δV_B for all the simulations in the range of 15 K to 300 K (δV_B was calculated by considering the V_B value at the end of the plateau of the Erase pulses). This confirms the physical picture discussed in Section 3.1 with a rigorous modeling approach.

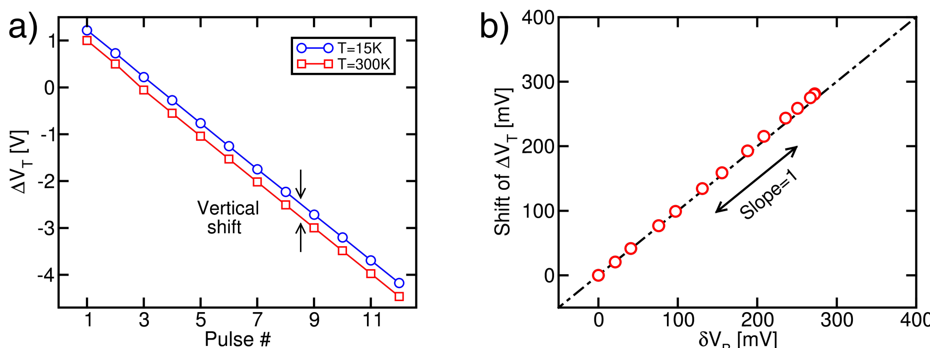


Figure 8. (**a**) Simulated ΔV_T transients during ISPE at $T = 15$ K and 300 K. (**b**) Scatter plot of the vertical shift in ΔV_T transient with T and its corresponding δV_B for different T values between 15 K and 300 K. The black dashed line is a guide to the eye, highlighting a one-to-one correlation.

4. Conclusions

In this work, we investigated the origin of the T dependence of the Erase operation in 3D NAND Flash arrays through experimental and modeling activities. We showed that such origin can be traced back to the T dependence of the GIDL current setting V_B during the Erase pulses. In particular, a weakening of the GIDL current with the reduction in T allows to easily explain the lower effectiveness of the Erase operation observed when T decreases down to the cryogenic regime. Finally, the T-induced change in V_B was directly correlated to the T-induced change in V_T obtained from an ISPE scheme.

Author Contributions: Methodology, G.M.; Validation, G.M.; Investigation, D.G.R.; Resources, L.C.; Writing—original draft, D.G.R.; Writing—review & editing, A.S.S. and C.M.C.; Supervision, A.S.S. and C.M.C. All authors have read and agreed to the published version of the manuscript.

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References

1. Monzio Compagnoni, C.; Goda, A.; Spinelli, A.S.; Feeley, P.; Lacaita, A.L.; Visconti, A. Reviewing the evolution of the NAND Flash technology. *Proc. IEEE* **2017**, *105*, 1609–1633. [CrossRef]
2. Kim, H.; Ahn, S.-J.; Shin, Y.G.; Lee, K.; Jung, E. Evolution of NAND Flash Memory: From 2D to 3D as a Storage Market Leader. In Proceedings of the 2017 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 14–17 May 2017; pp. 1–4. [CrossRef]
3. Goda, A. 3-D NAND technology achievements and future scaling perspectives. *IEEE Trans. Electron Devices* **2020**, *67*, 1373–1381. [CrossRef]
4. Goda, A. Recent progress on 3D NAND Flash technologies. *Electronics* **2021**, *10*, 3156. [CrossRef]
5. Shim, S.I.; Jang, J.; Song, J. Trends and Future Challenges of 3D NAND Flash Memory. In Proceedings of the 2023 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 21–24 May 2023; pp. 1–4. [CrossRef]
6. Tanaka, H.; Kido, M.; Yahashi, K.; Oomura, M.; Katsumata, R.; Kito, M.; Fukuzumi, Y.; Sato, M.; Nagata, Y.; Matsuoka, Y.; et al. Bit cost scalable technology with punch and plug process for ultra high density Flash memory. In Proceedings of the 2007 IEEE Symposium on VLSI Technology, Kyoto, Japan, 12–14 June 2007; pp. 14–15. [CrossRef]
7. Jang, J.; Kim, H.-S.; Cho, W.; Cho, H.; Kim, J.; Shim, S.I.; Jang, Y.; Jeong, J.-H.; Son, B.-K.; Kim, D.W.; et al. Vertical cell array using TCAT (Terabit Cell Array Transistor) technology for ultra high density NAND Flash memory. In Proceedings of the 2009 Symposium on VLSI Technology, Kyoto, Japan, 15–17 June 2009; pp. 192–193.

8. Parat, K.; Dennison, C. A floating gate based 3-D NAND technology with CMOS under array. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 48–51. [CrossRef]
9. Monzio Compagnoni, C.; Spinelli, A.S. Reliability of NAND Flash arrays: A review of what the 2-D–to–3-D transition meant. *IEEE Trans. Electron Devices* **2019**, *66*, 4504–4516. [CrossRef]
10. Caillat, C.; Beaman, K.; Bicksler, A.; Camozzi, E.; Ghilardi, T.; Huang, G.; Liu, H.; Liu, Y.; Mao, D.; Mujumdar, S.; et al. 3D NAND GIDL-assisted body biasing for erase enabling CMOS under array (CUA) architecture. In Proceedings of the 2017 IEEE International Memory Workshop (IMW), Monterey, CA, USA, 14–17 May 2017; pp. 1–4. [CrossRef]
11. Parat, K.; Goda, A. Scalig trends in NAND Flash. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 27–30. [CrossRef]
12. Kalavade, P. 4 bits/cell 96 Layer Floating Gate 3D NAND with CMOS under Array Technology and SSDs. In Proceedings of the 2020 IEEE International Memory Workshop (IMW), Dresden, Germany, 17–20 May 2020; pp. 1–4. [CrossRef]
13. Malavena, G.; Lacaita, A.L.; Spinelli, A.S.; Monzio Compagnoni, C. Investigation and compact modeling of the time dynamics of the GIDL-assisted increase of the string potential in 3-D NAND Flash arrays. *IEEE Trans. Electron Devices* **2018**, *65*, 2804–2811. [CrossRef]
14. Malavena, G.; Mannara, A.; Lacaita, A.L.; Spinelli, A.S.; Monzio Compagnoni, C. Compact modeling of GIDL-assisted erase in 3-D NAND Flash strings. *J. Comput. Electron.* **2019**, *18*, 561–568. [CrossRef]
15. Aiba, Y.; Tanaka, H.; Maeda, T.; Sawa, K.; Kikushima, F.; Miura, M.; Fujisawa, T.; Matsuo, M.; Horii, H.; Mukaida, H.; et al. Bringing in Cryogenics to Storage: Characteristics and Performance Improvement of 3D Flash Memory. In Proceedings of the 2021 IEEE International Memory Workshop (IMW), Dresden, Germany, 16–19 May 2021; pp. 1–4. [CrossRef]
16. Aiba, Y.; Tanaka, H.; Maeda, T.; Sawa, K.; Kikushima, F.; Miura, M.; Fujisawa, T.; Matsuo, M.; Sanuki, T. Cryogenic operation of 3D Flash memory for new applications and bit cost scaling with 6-bit per cell (HLC) and beyond. In Proceedings of the 2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Chengdu, China, 8–11 April 2021; pp. 1–3. [CrossRef]
17. Sanuki, T.; Aiba, Y.; Tanaka, H.; Maeda, T.; Sawa, K.; Kikushima, F.; Miura, M. Cryogenic operation of 3-D Flash memory for storage performance improvement and bit cost scaling. *IEEE J. Explor. Solid-State Comput. Devices Circuits* **2021**, *7*, 159–167. [CrossRef]
18. Tanaka, H.; Aiba, Y.; Maeda, T.; Ota, K.; Higashi, Y.; Sawa, K.; Kikushima, F.; Miura, M.; Sanuki, T. Toward 7 Bits per Cell: Synergistic Improvement of 3D Flash Memory by Combination of Single-crystal Channel and Cryogenic Operation. In Proceedings of the 2022 IEEE International Memory Workshop (IMW), Dresden, Germany, 15–18 May 2022; pp. 1–4. [CrossRef]
19. Aiba, Y.; Higashi, Y.; Tanaka, H.; Kikushima, F.; Fujisawa, T.; Mukaida, H.; Miura, M.; Sanuki, T. Demonstration of Recovery Annealing on 7-Bits per Cell 3D Flash Memory at Cryogenic Operation for Bit Cost Scalability and Sustainability. In Proceedings of the 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 11–16 June 2023; pp. 1–2. [CrossRef]
20. Rosar, M.; Leroy, B.; Schweeger, G. A new model for the description of gate voltage and temperature dependence of gate induced drain leakage (GIDL) in the low electric field region [DRAMs]. *IEEE Trans. Electron Devices* **2000**, *47*, 154–159. [CrossRef]
21. Lopez, L.; Masson, P.; Née, D.; Bouchakour, R. Temperature and drain voltage dependence of gate-induced drain leakage. *Microelectron. Eng.* **2004**, *72*, 101–105. [CrossRef]
22. Alnuaimi, A.; Nayfeh, A.; Koldyaev, V. Electric-field and temperature dependence of the activation energy associated with gate induced drain leakage. *J. Appl. Phys.* **2013**, *113*, 044513. [CrossRef]
23. Dabhi, C.K.; Roy, A.S.; Chauhan, Y.S. Compact Modeling of Temperature-Dependent Gate-Induced Drain Leakage Including Low-Field Effects. *IEEE Trans. Electron Devices* **2019**, *66*, 2892–2897. [CrossRef]
24. Refaldi, D.G.; Malavena, G.; Giulianini, M.; Chiavarone, L.; Spinelli, A.S.; Monzio Compagnoni, C. First evidence of SET-like behavior of 3-D NAND Flash cells in the deep-cryogenic regime. *IEEE Trans. Electron Devices* **2024**, *71*, 1066–1071. [CrossRef]
25. Beckers, A.; Jazaeri, F.; Ruffino, A.; Bruschini, C.; Baschirotto, A.; Enz, C. Cryogenic characterization of 28 nm bulk CMOS technology for quantum computing. In Proceedings of the 2017 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 11–14 September 2017; pp. 62–65. [CrossRef]
26. Beckers, A.; Jazaeri, F.; Enz, C. 28 nm Bulk and FDSOI Cryogenic MOSFET: (Invited Paper). In Proceedings of the 2018 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Beijing, China, 21–23 November 2018; pp. 45–46. [CrossRef]
27. Luo, C.; Li, Z.; Lu, T.T.; Xu, J.; Guo, G.P. MOSFET characterization and modeling at cryogenic temperatures. *Cryogenics* **2018**, *98*, 12–17. [CrossRef]
28. Beckers, A.; Jazaeri, F.; Enz, C. Cryogenic MOSFET Threshold Voltage Model. In Proceedings of the ESSDERC 2019—49th European Solid-State Device Research Conference (ESSDERC), Cracow, Poland, 23–26 September 2019; pp. 94–97. [CrossRef]
29. Beckers, A.; Jazaeri, F.; Grill, A.; Narasimhamoorthy, S.; Parvais, B.; Enz, C. Physical Model of Low-Temperature to Cryogenic Threshold Voltage in MOSFETs. *IEEE J. Electron Devices Soc.* **2020**, *8*, 780–788. [CrossRef]
30. Singh, S.K.; Gupta, S.; Vega, R.A.; Dixit, A. Accurate modeling of cryogenic temperature effects in 10-nm bulk CMOS FinFETs using the BSIM-CMG model. *IEEE Electron Device Lett.* **2022**, *43*, 689–692. [CrossRef]

31. Grill, A.; Michl, J.; Diaz-Fortuny, J.; Beckers, A.; Bury, E.; Chasin, A.; Grasser, T.; Waltl, M.; Kaczer, B.; De Greve, K. A Comprehensive Cryogenic CMOS Variability and Reliability Assessment using Transistor Arrays. In Proceedings of the 2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Seoul, Republic of Korea, 7–10 March 2023; pp. 1–3. [CrossRef]
32. Hemink, G.J.; Tanaka, T.; Endoh, T.; Aritome, S.; Shirota, R. Fast and accurate programming method for multi-level NAND EEPROMs. In Proceedings of the 1995 Symposium on VLSI Technology. Digest of Technical Papers, Kyoto, Japan, 6–8 June 1995; pp. 129–130.
33. Monzio Compagnoni, C.; Gusmeroli, R.; Spinelli, A.S.; Visconti, A. Analytical model for the electron-injection statistics during programming of nanoscale NAND Flash memories. *IEEE Trans. Electron Devices* **2008**, *55*, 3192–3199. [CrossRef]
34. Refaldi, D.G.; Malavena, G.; Chiavarone, L.; Spinelli, A.S.; Monzio Compagnoni, C. Evidence of widely distributed time constants in the vertical charge loss of 3-D charge-trap NAND Flash memories. *IEEE Electron Device Lett.* **2024**, *10*, 1811–1814. [CrossRef]
35. Schanovsky, F.; Verreck, D.; Stanojevic, Z.; Schallert, S.; Arreghini, A.; van den Bosch, G.; Rosmeulen, M.; Karner, M. Modeling the Operation of Charge Trap Flash Memory–Part I: The Importance of Carrier Energy Relaxation. *IEEE Trans. Electron Devices* **2024**, *71*, 547–553. [CrossRef]
36. Verreck, D.; Schanovsky, F.; Arreghini, A.; van de Bosch, G.; Stanojevic, Z.; Karner, M.; Rosmeulen, M. Modeling the Operation of Charge Trap Flash Memory–Part II: Understanding the ISPP Curve with a Semianalytical Model. *IEEE Trans. Electron Devices* **2024**, *71*, 554–559. [CrossRef]
37. Solanki, R.; Manwani, A.; Mahajan, A.; Patrikar, R.M. Modeling of program/erase transient in heterogeneous SiNx charge trap Flash memories. *Superlattices Microstruct.* **2020**, *144*, 106577. [CrossRef]
38. Amoroso, S.M.; Monzio Compagnoni, C.; Mauri, A.; Maconi, A.; Spinelli, A.S.; Lacaita, A.L. Semi-analytical model for the transient operation of gate-all-around charge-trap memories. *IEEE Trans. Electron Devices* **2011**, *58*, 3116–3123. [CrossRef]
39. Giulianini, M.; Malavena, G.; Monzio Compagnoni, C.; Spinelli, A.S. Time dynamics of the down-coupling phenomenon in 3-D NAND strings. *IEEE Trans. Electron Devices* **2022**, *69*, 6757–6762. [CrossRef]
40. Tsai, W.-J.; Lin, W.L.; Cheng, C.C.; Ku, S.H.; Chou, Y.L.; Liu, L.; Hwang, S.W.; Lu, T.C.; Chen, K.C.; Wang, T.; et al. Polycrystalline-silicon channel trap induced transient read instability in a 3D NAND Flash cell string. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 11.3.1–11.3.4. [CrossRef]
41. Lee, S.-H.; Kwon, D.W.; Kim, S.; Baek, M.-H.; Lee, S.; Kang, J.; Jang, W.; Park, B.-G. Investigation of transient current characteristics with scaling-down poly-Si body thickness and grain size of 3D NAND Flash memory. *Soid-State Eectron.* **2019**, *152*, 41–45. [CrossRef]
42. Miccoli, C.; Monzio Compagnoni, C.; Amoroso, S.M.; Spessot, A.; Fantini, P.; Visconti, A.; Spinelli, A.S. Impact of neutral threshold-voltage spread and electron-emission statistics on data retention of nanoscale NAND Flash. *IEEE Electron Device Lett.* **2010**, *31*, 1202–1204. [CrossRef]
43. Monzio mpagnoni, C.; Mauri, A.; Amoroso, S.M.; Maconi, A.; Spinelli, A.S. Physical modeling for programming of TANOS memories in the Fowler-Nordheim regime. *IEEE Trans. Electron Devices* **2009**, *56*, 2008–2015. [CrossRef]
44. Rais, K.; Balestra, F.; Ghibaudo, G. Temperature dependence of gate induced drain leakage current in silicon CMOS devices. *Electron. Lett.* **1994**, *30*, 32–34.:19940011. [CrossRef]
45. Ghibaudo, G.; Balestra, F. Low temperature characterization of silicon CMOS devices. In Proceedings of the International Conference on Microelectronics, Nis, Serbia, 12–14 September 1995; pp. 613–622. [CrossRef]
46. Chan, T.Y.; Chen, J.; Ko, P.K.; Hu, C. The impact of gate-induced drain leakage current on MOSFET scaling. In Proceedings of the 1987 International Electron Devices Meeting, Washington, DC, USA, 6–9 December 1987; pp. 718–721. [CrossRef]
47. Parke, S.A.; Moon, J.E.; Wann, H.C.; Ko, P.K.; Hu, C. Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model. *IEEE Trans. Electron Devices* **1992**, *39*, 1694–1703. [CrossRef]
48. Chang, C.; Lien, J. Corner-field induced drain leakage in thin oxide MOSFETs. In Proceedings of the 1987 International Electron Devices Meeting, Washington, DC, USA, 6–9 December 1987; pp. 714–717. [CrossRef]
49. Chen, J.; Chan, T.Y.; Chen, I.C.; Ko, P.K.; Hu, C. Subbreakdown drain leakage current in MOSFET. *IEEE Electron Device Lett.* **1987**, *8*, 515–517. [CrossRef]
50. Gundapaneni, S.; Bajaj, M.; Pandey, R.K.; Murali, K.V.R.M.; Ganguly, S.; Kottantharayil, A. Effect of band-to-band tunneling of junctionless transistors. *IEEE Trans. Electron Devices* **2012**, *59*, 1023–1029. [CrossRef]
51. Fan, J.; Li, M.; Xu, X.; Yang, Y.; Xuan, H.; Huang, R. Insight into gate-induced drain leakage in silicon nanowire transistors. *IEEE Trans. Electron Devices* **2015**, *62*, 213–219. [CrossRef]
52. Jomaah, J.; Ghibaudo, G.; Balestra, F. Temperature dependence of gate-induced-drain-leakage (GIDL) current in thin-film SOI MOSFETs. In Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductivity, Reno, NV, USA, 22–27 May 1995; pp. 260–270.
53. Chen, J.; Assaderaghi, F.; Ko, P.-K.; Hu, C. The enhancement of gate-induced-drain-leakage (GIDL) current in short-channel SOI MOSFET and its application in measuring lateral bipolar current gain beta. *IEEE Electron Device Lett.* **1992**, *13*, 572–574. [CrossRef]

54. Dunga, M.; Kumar, A.; Ramgopal Rao, V. Analysis of floating body effects in thin film SOI MOSFETs using the GIDL current technique. In Proceedings of the 2001 8th International Symposium on the Physical and Failure Analysis of Integrated Circuits, Singapore, 13 July 2001; pp. 254–257. [CrossRef]
55. Park, H.; Colinge, J.; Cristoloveanu, S.; Bawedin, M. Persistent Floating-Body Effects in Fully Depleted Silicon-on-Insulator Transistors. *Phys. Status Solidi A* **2020**, *217*, 254–257. [CrossRef]

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