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Event-driven SPAD camera with 60 ps IRF and up to $1.6 \cdot 10^8$ photon time-tagging measurements per second

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ABSTRACT

We present a compact camera module based on an array of 16 × 16 single-photon avalanche diodes (SPADs) with fast-gating capabilities and hosting 16 shared time-to-digital converters (TDCs) with a least significant bit (LSB) of 6 ps. SPADs are gated with a rising-edge of less than 500 ps and show an average instrument response function (IRF) of 60 ps FWHM, including the TDCs, with less than 4 ps time-dispersion across a 30 ns gate window. Differential non-linearity (DNL) and integral non-linearity (INL) are as good as 0.04 LSB and 3.6 LSB, respectively. An event-driven readout protocol optimizes data transfer from the SPAD chip to the FPGA, handling the time-of-flight (TOF) pre-processing in order to minimize the dead-time of the TDCs, thus sustaining up to $1.6 \cdot 10^8$ conversions per second. TOF data can be transferred towards a PC via USB-C with a maximum throughput of about 6 Gbit/s.

Our camera meets the requirements of an optimized multi-pixel solution for non-line-of-sight (NLOS) imaging, as it combines fast-gating with narrow IRF: the sub-nanosecond activation of the SPADs is exploited to reject spurious light pulses, like the first bounce one from the relay wall, and properly acquire multiply-scattered photons arriving from the hidden target, while its narrow IRF allows for centimeter-accurate NLOS reconstructions. Furthermore, while the high throughput paves the way towards real-time NLOS acquisitions at video-rates, the compact form-factor of our camera can optimize size, weight, power and cost of current state-of-art NLOS imaging systems.

Keywords: SPAD camera, SPAD array, NLOS imaging, fast-gating, time-of-flight, TDC

1. INTRODUCTION

Non-line-of-sight (NLOS) imaging is among those imaging techniques that exploit the time of flight (ToF) of single photons to capture 3D depth-resolved images [1]. NLOS imaging systems make use of a pulsed laser source to illuminate a visible surface (i.e., the relay wall), and are designed to only collect photons that diffuse multiple times before reaching the sensor, discarding the ones that are directly reflected from the relay wall thanks to the time-filtering of incoming light implemented by the gated-mode operation of the detector. Time-gated SPAD sensors proved excellent performance in this field [2], [3], especially those offering an Instrument Response Function (IRF) as narrow as few tens of picoseconds, which enables NLOS reconstruction with centimeter-accurate resolution.

NLOS imaging also benefits from a large sensor, able to acquire return echo pulses over a wide area, where the event rate per pixel is quite low. Since acquisition times are proportional to the number of employed pixels, the 16 × 16 SPAD camera herein presented is developed to provide a scalable multi-pixel architecture, aiming to enable high-resolution NLOS reconstructions at video rates by coupling the camera with an external scanning system, such as a X-Y galvanometer mirror system.

2. SPAD CAMERA

The SPAD camera we present is built around the 16 × 16 SPAD imager shown in Figure 1 (left) and it is based on the printed circuit boards (PCBs) stack shown in Figure 1 (right). At the bottom of the stack, a digital interface board is equipped with a Xilinx Artix-7 (XC7A200T) field programmable gate array (FPGA) and USB-C link, whereas the two upper boards host and supply the custom 16 × 16 SPAD imager. This system is embedded in a compact $10 \times 7 \times 5$ cm^3 housing, provided with a standard C-Mount thread for lenses, and accessed through SMA connectors in order to grant seamless compatibility with NLOS acquisition systems for easy installation in the end application. Other external components required to perform NLOS measurements are: i) a pulsed laser as a source of active illumination; ii) a 2-axis

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scanning system to extend image resolution; iii) a PC to process the data received by the SPAD camera and run the NLOS reconstruction algorithms. No additional time-correlated single-photon counting (TCSPC) unit is required nor to compute photon ToFs, nor to synchronize the scanning system, since the employed sensor ensures Time-Tagged Time-Resolved (TTTR) capabilities.

3. 16 × 16 SPAD ARRAY

The sensor is a 16 × 16 SPAD array fabricated in a 160 nm Bipolar-CMOS-DMOS (BCD) technology, where SPADs with excellent performance were developed [4]: with the SPADs exceeding their breakdown voltage by 5 V, photon detection efficiency (PDE) peaks at about 70% at 490 nm wavelength, and timing response approaches 30 ps FWHM. Dark count rate (DCR) has a median value below 1 kcps and afterpulsing probability is typically negligible and well below 1%.

Avalanche sensing and pre-processing electronics have been integrated on the same die of photodetectors. Within the active area, each microcell (i.e., a 2 × 2 SPAD sub-array) includes a fast-gated frontend. Gated mode operation is implemented by actively modulating the voltage of each SPAD from below to above its breakdown level, rather than simply masking output avalanche pulses triggered during gate-OFF windows. Indeed, this latter solution does not prevent the SPADs to be blinded by strong direct reflections prior to the vary faint NLOS signal, hence does not suite NLOS imaging technique. To ensure the narrowest temporal response, a low-threshold is set by fast comparators in order to minimize the dispersion in the avalanche build-up rise-time.

Given the low NLOS event rate, a bank of 16 shared time-to-digital converters (TDCs) is embedded outside the imaging area, on one side of the array, allowing to convert up to 16 events per gate window. TDCs feature a dual START-STOP interpolation architecture in order to exploit the sliding-scale technique [5], so to improve conversion linearity. Within each interpolator, a coarse-fine architecture is nested [6], leading to a worst-case conversion time of ~ 50 ns and final resolution of ~ 6 ps, which helps reducing the TDC's contribution to the overall timing jitter of the sensor. The full-scale range (FSR) of the converter is extended to ~ 2.45 µs by means an additional 10-bit counter. An asynchronous fixed priority arbiter (FPA) tree is designed to convey the first photon detection of a macrocell (i.e., a cluster of 4 × 4 SPADs) to its own TDC, providing the converter with the 4-bit address of the first fired SPAD, or, in case of concurrent events, following a fixed priority list. A validation circuit evaluates possible collisions, eventually resetting the TDC and rearming the FPA tree for propagating further events.

16 output serializers are implemented to transfer the 30-bit time-conversion of each TDC, which the 4-bit SPAD address is attached to, to an external FPGA through an event driven protocol. Each serializer is timed by an external 200 MHz clock and drives two parallel output lines, sustaining a maximum throughput of about 10^7 conversions per second, thus leading to an overall IC data rate of $1.6 \cdot 10^8$ conversions per second. A pipelined architecture allows each TDC to start new conversions during data transfers.

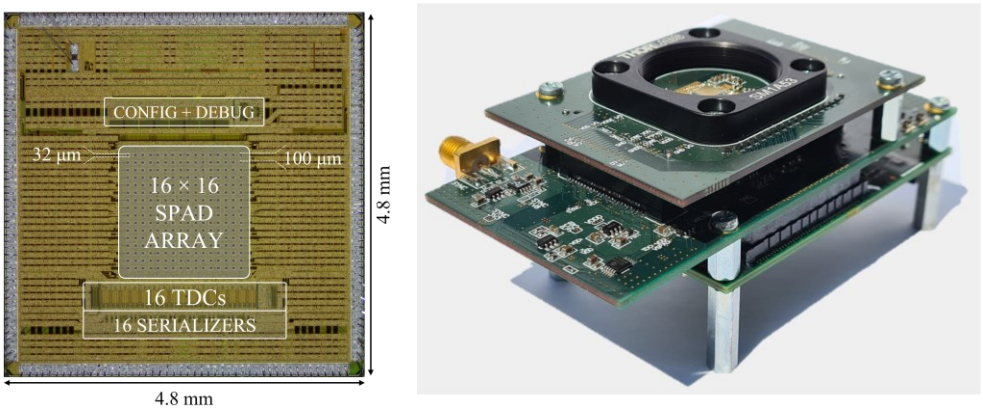

Figure 1. Left: micrograph of the 16 × 16 SPAD array, whose size is 4.8 mm × 4.8 mm. Left: photograph of the boards of SPAD camera. External dimensions are 10 × 7 × 5 cm^3.

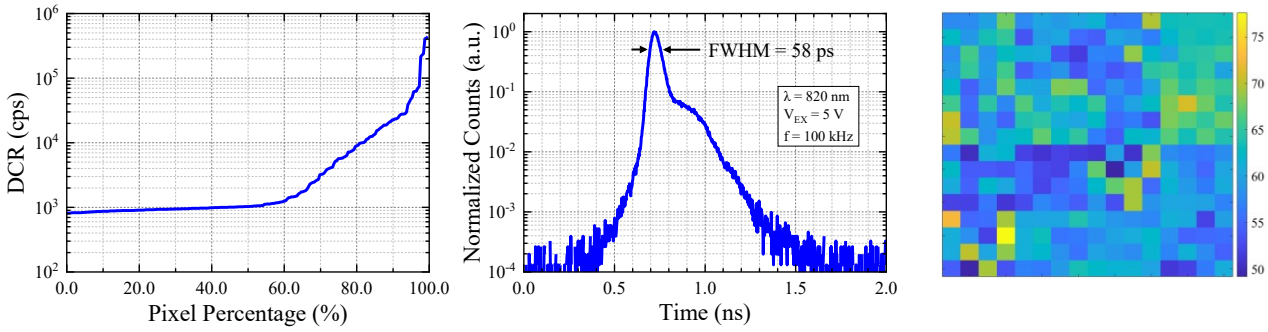

Figure 2. Left: Percentage distribution of dark count rates. Values are measured at ~ 320 K operating temperature and with an excess bias voltage of 5 V. Middle: Single-pixel IRF obtained with a narrow-pulsed laser (15 ps FWHM) at 820 nm wavelength, operated at 100 kHz repetition rate. The excess bias voltage is 5 V. Measured FWHM is 58 ps, while the additional bump appearing after the main peak is due to the actual shape of the laser pulse. Right: map of the IRF (FWHM) of the 16 x 16 pixels. Values are in picoseconds.

32 µm square SPADs with rounded corners have been laid out at 100 µm pitch. Detector size was selected as a trade-off between a high fill-factor and a narrow IRF, with a sufficient pixel-to-pixel distance to accommodate the microcell circuitry and signal routing towards the peripheral TDCs. The resulting fill-factor is about 9.6%. This value could be improved up to a theoretical 80% by mounting a microlens array (MLA), which the sensor is set up to mate.

Overall chip size is 4.8 mm × 4.8 mm, with the active area measuring 1.6 mm × 1.6 mm (see Figure 1 - left).

4. EXPERIMENTAL RESULTS

In order to prove NLOS imaging capabilities, the characterization of the SPAD camera is presented in terms of DCR, IRF and both differential and integral conversion linearities (i.e., DNL and INL, respectively). All reported measurements were acquired with the array operated in fast-gated mode and the SPAD excess bias voltage set to 5 V, to better represent real-world operating scenarios. Moreover, the count rate of each TDC was controlled to not exceed 5% of the gate repetition rate, aiming to avoid pile-up distortion [7].

4.1 DCR

The percentage distribution of DCR of single-SPADs is reported in Figure 2 (left). DCR median value is ~ 1 kcps, with a slope changing at about 60% mark and 6 hot pixels exceeding 100 times the average DCR value. By comparing to these results to the one expected for this technology, operating temperature is estimated to be ~ 320 K. DCR does not significantly change with gate frequency.

4.2 IRF

Figure 2 (middle) shows the IRF to a narrow-pulsed laser (15 ps FWHM) of one representative SPAD, whose FWHM is 58 ps. A complete map of the 16 × 16 pixels is reported in Figure 2 (right) and shows uniform temporal responses ranging from 50 ps to 75 ps FWHM across the whole array, with an average value of about 60 ps and a dispersion of ~ 5 ps. By scanning the laser across a 30 ns gate window, temporal responses experience a minor 3.4 ps standard deviation, which does not significantly affect practical measurements and, therefore, makes this camera perfectly compatible with NLOS imaging requirements on resolution.

4.3 DNL and INL

DNL and INL, which are reported in Figure 3, were evaluated along a 30 ns gate window when applying a gate signal with a repetition rate of 25 MHz. Root-mean-square values of DNL and INL are as low as 250 fs (~ 0.04 LSB) and 21.56 ps (~ 3.6 LSB), respectively, and appear to be limited by the fast-gated operation of the sensor, rather than the TDCs themselves. Indeed, a damped oscillation pattern is visible from both DNL and INL graphs and is due to the power supply ringing induced by the fast discharge currents of the SPADs' anodes at the rising edge of the gate, which also affects counts distribution.

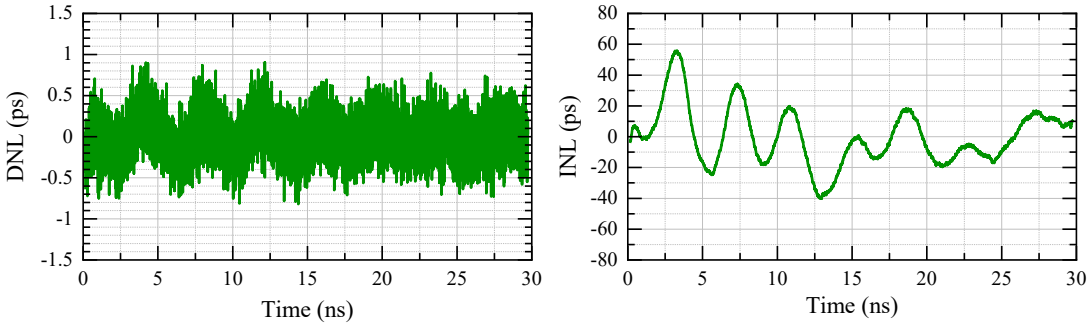

Figure 3. DNL (left) and INL (right) of one representative pixel along a gate-window of 30 ns.

5. CONCLUSIONS

We developed a time-gated SPAD camera based on a custom 16 × 16 SPAD imager featuring TCSPC functionalities. The goal of this system is to provide seamless integration with existing time-resolved NLOS imaging setups and pave the way towards video rate NLOS reconstruction, without compromising image quality and resolution of current solutions. By proving an average IRF of 60 ps FWHM combined with fast-gated operation (< 500 ps activation times), this imager matches the performance of other state-of-the-art NLOS sensors, but it offers a larger number of pixels together with TCSPC functionalities to speed up acquisitions. By exploiting an event-driven readout approach, rather than a typical frame-based one, the module is able to achieve a maximum throughput of $1.6 \cdot 10^8$ conversions per second. Moreover, such an event-driven protocol enables TTTR capabilities, thus allowing to synchronize external scanning systems with no need of dedicated TCSPC units.

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