Circuit Modeling of Fast Ethernet Signal for EMC and SI Analysis

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***Abstract*—The 100BASE-TX Fast Ethernet is the most widely adopted standard in residential sector today. This standard requires the signal generated by the physical layer to be encoded with a Multi-Level Transmit (MLT)-3 modulation, which shifts the spectrum energy to low frequencies. Improper design of the Fast Ethernet system causes Electromagnetic Compatibility (EMC) and Signal Integrity (SI) related issues that occur in real-world applications, yet an efficient circuit model for MLT-3 signal generation, which is crucial for system EMC and SI performance evaluation, is not available in the literature. This paper fills this gap by presenting a circuit model that simulates the behavior of the physical layer for Fast Ethernet applications. By tuning the sampling frequency parameter of the circuit and adding an RC filter, the circuit model mimics the time-domain and frequency-domain characteristics of a measured MLT-3 signal, allowing to effectively address the testing and optimization of EMC and SI issues in Fast Ethernet systems.**

Keywords— Circuit model, Electromagnetic Compatibility (EMC), Fast Ethernet, MLT-3, Signal Integrity (SI).

I. INTRODUCTION

Over the last forty years, Ethernet technology has emerged as the most widespread communication technology in a wide variety of fields. Developed originally to be deployed in Local Area Networks (LANs), its characteristics such as cost effectiveness, ease of installation, reliability, and expandability have led to its application expanding to other sectors such as automotive, space, Internet of Things (IoT), Machine to Machine (M2M), etc.

Different Ethernet standards exist and are defined based on the applications and the data transmission speeds. To date, the most deployed technology, particularly in the residential area, is 100BASE-TX also referred to as Fast Ethernet. 100BASE-TX requires copper unshielded twisted pair cable and supports data transfer speeds of 100Mbps. It uses the CSMA/CD protocol for collision detection and uses a maximum cable length of 100 meters. The "100" in the name refers to the data transfer rate of 100Mbps, "BASE" refers to the use of baseband signaling, and "TX" refers to the use of twisted pair cable [1]. The information is transmitted via the so-called transmission twisted pair, and the transmitted signal is encoded using the Multi-Level Transit (MLT)-3 technique.

The MLT-3 is a type of encoding technique used in Ethernet networks that encodes data using three signal levels, rather than the two levels used in traditional binary signaling (i.e. 0 and 1). This allows for more efficient use of the available bandwidth and improved signal quality. In fact, reducing the number of signal transitions decreases the amount of electromagnetic interference (EMI) introduced by the source itself by shifting the harmonic content of the signal to a lower frequency range.

Even though the signal is intended to be as disturbance-free as possible, the EMC theory suggests that electromagnetic emissions and disturbances affecting signal integrity are caused not only by the source, but also by the interconnection of the different blocks of the system [2], [3] and by the load terminations [4], [5]. It is therefore important to have a reference signal that takes these effects into account and allows them to be evaluated correctly.

Since solving EMC and SI problems at the design stage is cost- and time-effective, it is deemed necessary to design a signal that can simulate the signal required by the test procedures as closely as possible. Several codes are already available in MATLAB® that effectively perform this task; application of these codes in studying the performance of Ethernet systems leads to reliable results, as reported in [6-8]. However, transferring the signals thus defined into a different simulation environment, i.e., electromagnetic simulation software that is specifically used in analyzing and solving EMC problems, requires an additional step that could easily be overcome by implementing a solution directly on the software itself. Furthermore, to the best of the authors' knowledge, there is not an efficient circuit model in the literature for simulation of fast Ethernet signal.

To fill this gap, in this paper, an EMC-oriented circuit model of fast Ethernet is proposed. The paper is structured as follows. Section II presents an overview of the encoding technique implemented in 100BASE-TX standard, describing the rationale behind the selected encoding.

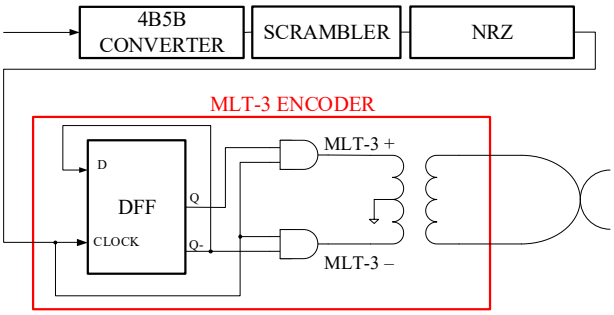


Fig. 1. 100BASE-TX, physical layer encoding system.

Section III describes the basic circuit model implemented to simulate the impact of the encoded signal on the system's electromagnetic emissions and signal fidelity, followed by the analysis of the simulations carried out in both the time and frequency domains. In particular, these simulations are implemented in ANSYS® Electronics (circuit simulator) and MATLAB® Simulink. These analyses show that in the case of direct implementation of the circuit described in the standards, it is necessary to select the sampling frequency appropriately in order to consider the transitional effects of the actual signal. Section IV describes the proposed final model, which includes the introduction of an RC filter for preserving signal rise and fall times when the source is connected to a load. To verify the effectiveness of the filter, the section also presents simulations performed in the time and frequency domains as developed in the previous section. From the simulations, it is confirmed that the proposed model allows a correct evaluation of EMC and SI aspects from the design stage. An example of application of the coding thus generated to a load consisting of a microstrip line of variable length is given in Section V. The conclusions are given in Section VI.

II. MLT-3 Encoding Technique Overview

IEEE 802.3u 100BASE-TX physical layer standards for 100 Mbps over Cat. 5 Unshielded Twisted-wire Pair (UTP) cable defines as encoding technique the combination of 4B5B, and MLT-3. In addition, 100Base-TX requires a scrambling stage, which is meant to randomize the digital signal to further reduce radiated emissions [9], [10]. The encoding stage schematic diagram is reported in Fig. 1.

The signal is transmitted and received via two of the four twisted pairs of a cable of Cat. 5 or higher; each twisted pair is used for transmission in only one direction and each segment of the network has a maximum cable length of 100 m. The digital source signal is a Non Return to Zero (NRZ) encoded signal, i.e. a simple binary encoded signal, where each low level is translated as a zero and each high level as a one. Such an encoded signal causes clock synchronization problems when the beat stream consists of long strings of 0's and 1's in sequence and therefore no voltage level transitions are present. With such a signal, the receiver struggles to retrieve the correct clock and may fail to deduce the correct number of bits.

In order not to lose information on the synchronization signal, the 4B5B encoding method is used, which allows 4-bit words to be mapped into 5-bit words, thus guaranteeing at least one voltage transition every five bits. Each 4-bit word is preliminarily assigned a corresponding 5-bit word. Although it guarantees correct synchronization, this method has the disadvantage to increase the output bit rate from the nominal

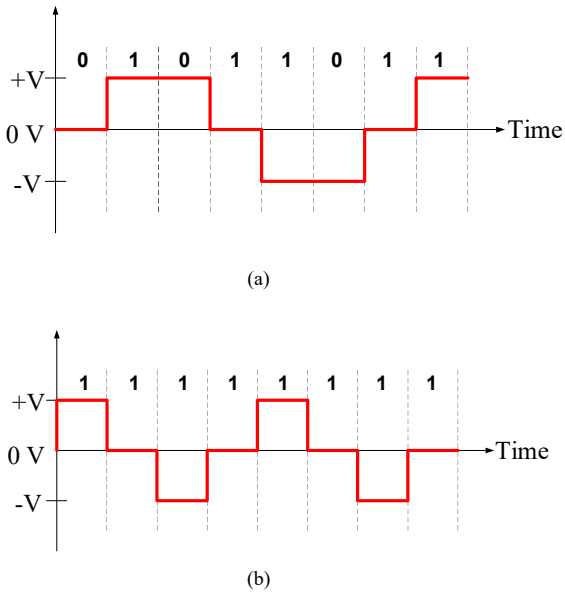


Fig. 2. MLT-3 signal: (a) typical case and (b) worst case.

100 Mbps at which the NRZ-encoded signal is transmitted to 125 Mbps. The new bit rate exceeds the rated UTP cable natural frequency, which is 100 MHz (in this application the baud rate coincides with the bit rate).

In order to reduce the signal transmission frequency thus ensuring the possibility of using UTP cables (which are far cheaper than their higher category equivalents) without attenuation or crosstalk problems, the MLT-3 encoding technique is used. The MLT-3 encoding allows transmitting the bit stream at a lower frequency, i.e., 31.25 MHz. The MLT-3 technique foresees the physical output signal varying between three analogue levels: + V, 0, and – V, as shown in Fig. 2(a). Each "1" bit in the input bit stream corresponds to a logic level transition. No direct transition between +1 and -1 logic levels are allowed, which results in a shift of the signal harmonics content towards lower frequencies. A 125 Mbps digital signal is therefore delivered as a 31.25 MHz signal that corresponds to just one quarter of the output bit rate of the 4B5B stage. In fact, the maximum transmission frequency occurs in case of four "1" bits stream, as shown in Fig. 2(b). This type of encoding offers a twofold advantage: the signal encodes 100 Mbps, and varies slowly enough to be transmitted over a Cat.5 UTP cable.

III. Basic Circuit Model of Physical-Layer

The environment in which the model has been developed is ANSYS® Electronics (circuit simulator) [11], to ensure interoperability between the various tools allowing detailed analysis of EMC and SI issues.

The aim is to generate a waveform that could replicate the signal behavior for pre-compliance implementation. The figures of merit of the output signal must then be defined. To establish the characteristics of the waveform output to the system, reference is made to the compliance tests for 100BASE-TX physical layer defined in ANSI X3.263 and IEEE 802.3 standards reported in [9], and to the patent US005280500 submitted by M. Mazzola et al. [12].

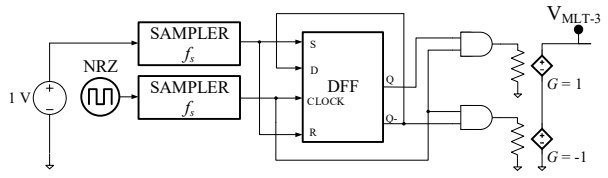


Fig. 3. Basic circuit model derived from the 100BASE-TX standard.

A. Basic Model

Fig. 3 illustrates the basic model circuit diagram. The input of the system is represented by two signals: A DC signal whose only function is to keep the state of the Delay Flip-Flop (DFF) in delay mode, and a modulated NRZ signal switching at a maximum frequency of 125 MHz. The latter represents the expected input to the MLT-3 coding module, considering all the pre-modulations described in the previous paragraph. The two signals are sampled at a certain sampling frequency f_s. The sequences thus obtained represent the inputs of the DFF.

For the MLT-3 encoding of the signal we refer to the structure proposed in [12]: the DFF receives the modulated NRZ sequence as input clock. The inverted output of the DFF itself is in turn feedback connected to input D. Thus, each positive transition of the input clock corresponds to a change of state of the outputs.

The outputs of the DFF are hence connected to two dual-input "AND" gates respectively. The second input of both gates is connected to the same clock represented by the NRZ signal. The two "AND" gates generate two output signals, which subtract from each other via the two voltage controlled sources connected as shown in Fig. 3. Eventually, the MLT-3 modulated signal is observed at the output of the controlled sources.

B. Time Domain Simulation

Once the topology of the circuit to be simulated has been defined, the selection of the sampling frequency is made to obtain the waveform that best approximates the real behavior of the MLT-3 modulated signal. A signal with a transmission speed of 125 Mbps is expected at the input. The expected output waveform is depicted in [13]. The rise and fall times are expected to vary between 3 ns and 5 ns, with a typical value of 4 ns. The minimum signal period is 32 ns, and each bit is transmitted in a time interval of 8 ns.

Three sampling frequencies are then selected to analyze the signal trend over time: 125 MHz, 250 MHz, 1250 MHz. These frequencies are imposed in the two sampler blocks and allow the continuous signals to be converted into sequences. The sampling theorem for non-periodic signals requires that the sampling frequency has to be properly selected so as not to incur errors in the interpretation of the information itself.

A correct application therefore requires the selection of a sampling frequency that is equal to or greater than twice the maximum frequency at which the signal is transmitted. A comparison of the graphs obtained by simulation in the time domain, however, shows that as the sampling frequency increases, the assumption of signal rise and fall times equal to 4 ns decays: Indeed, the higher the frequency, the more rise and fall times decrease. A comparison of Fig. 4(a) with Fig. 4(b) and Fig. 4(c) demonstrates that the rise and fall times tend to zero as the sampling frequency increases. These times are closely related to the harmonic content of the signal and the

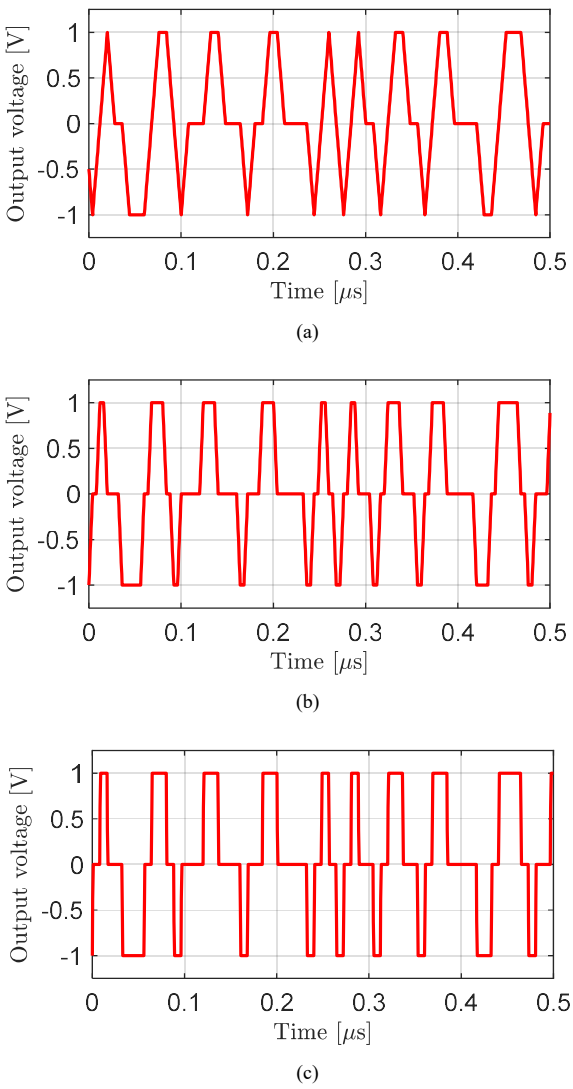


Fig. 4. Time domain analysis of MLT-3 signal considering f_s equal to (a) 125 MHz, (b) 250 MHz, and (c) 1250 MHz.

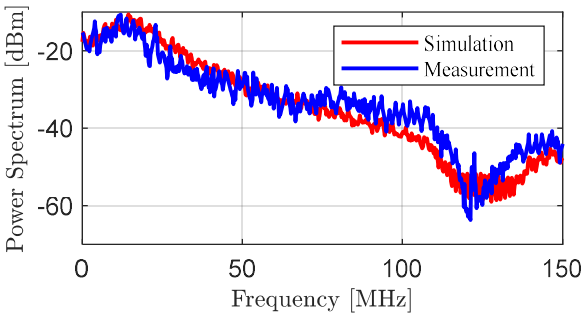
TABLE I. SA SETTINGS [15]

Spectrum Analyzer settings		
Span frequency	***Center frequency***	***RBW***
150 MHz	75 MHz	300 kHz

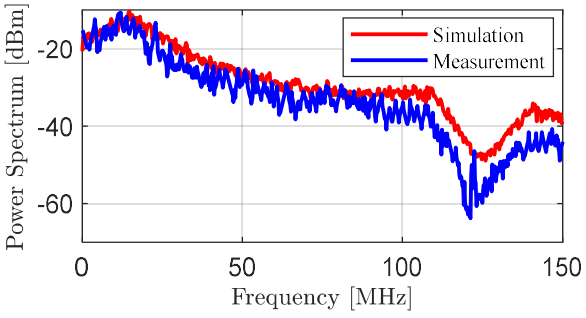
presence of electromagnetic interference. Usually, longer rise and fall times are selected to decrease electromagnetic interference due to the signal itself. Consequently, for the purpose of EMC and SI simulations, the solution best suited to approximate real-world case is to select 125 MHz as sampling frequency.

C. Frequency Domain Analysis

To investigate the effect of the sampling frequency on the signal spectrum the time domain sequences obtained in the previous step are exported in the MATLAB® Simulink environment for better post-processing. Here, the spectrum of the sampled signal is obtained via a Spectrum Analyzer (SA) block [14]. The rationale for the choice not to apply an FFT algorithm arises from the intention to conduct a direct comparison with the spectrum of an MLT-3 signal measured



(a)



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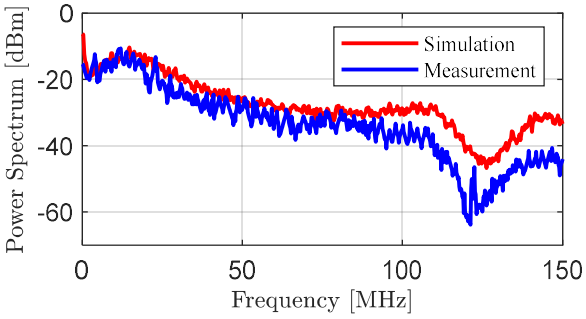


(c)

Fig. 5. Comparison of the spectrum of an MLT-3 signal measured by SA with the simulated spectra of the MLT-3 signals sampled at frequency (a) 125 MHz, (b) 250 MHz, and (c) 1250 MHz.

using a SA [15], [16]. The simulation is conducted in the frequency range from 0 Hz up to 150 MHz (i.e., just above the rated maximum frequency of Cat. 5 cables). The frequency spectra of the signals obtained considering the different sampling frequencies are compared with the frequency spectrum of the MLT-3 signal presented in [15] considering the SA settings shown in Table I.

From this analysis, it is evident that the spectrum of the signal sampled at 125 MHz is more similar to the measured spectrum than the spectrum of signals sampled at twice and ten times the maximum signal frequency. In particular, when observing the high-frequency behavior (see Fig. 5), it is evident that spectra obtained by sampling at higher frequencies do not closely follow the measured spectrum, meaning that the energy associated with each harmonic is greater than the measured one. On the other hand, by selecting 125 MHz as the sampling frequency, the deviation between the simulated and measured spectrum is significantly smaller. In practical application, this results in more reliable EMC and

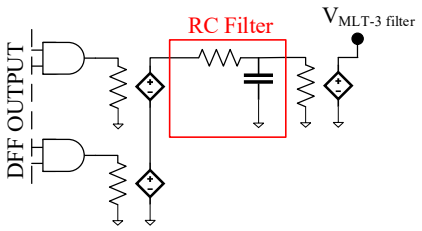


Fig. 6. Improved circuit model involving the addition of an output RC filter to the MLT-3 coding stage.

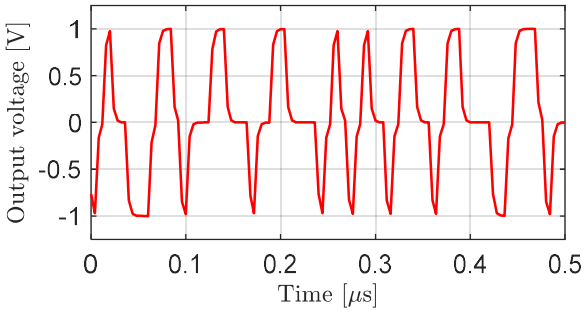


Fig. 7. MLT-3 signal generated by the proposed model.

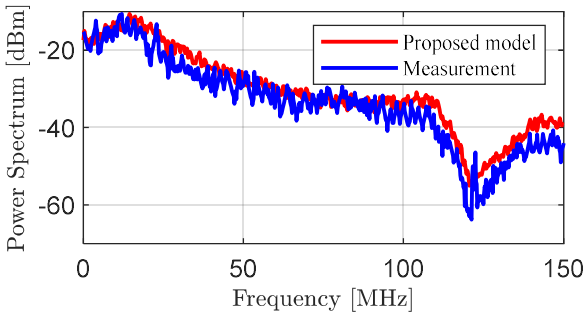


Fig. 8. Comparison of the spectrum of an MLT-3 signal measured by SA with the simulated spectrum of an MLT-3 signal obtained by the proposed model.

SI analyses at design level. As a matter of fact, selecting the signal whose frequency spectrum is closest to the measured one allows to employ in simulation the signal that best approximates the harmonic content of the signal required by the standard.

IV. Improved Circuit Model

A. Model Implementation

The basic model derived from the application of the circuit described in [12] by selecting a sampling frequency of 125 MHz adequately simulates the standardized signal. In practical applications, however, a load (e.g. an Ethernet cable) is connected to the encoder output, hence the waveform is further filtered and consequently loses the rising and falling characteristics whose importance has been described in the previous paragraphs.

To prevent this loss of information, an RC filter is placed at the output of the encoder stage as shown in Fig. 6. The RC filter forces a transient in the shift from one voltage level to the other, reintroducing rise and fall times of duration congruent with the specifications. The suggested resistance and capacitance values are $R = 50\ \Omega$ and $C = 40$ pF.

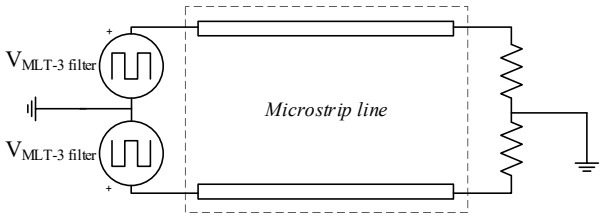
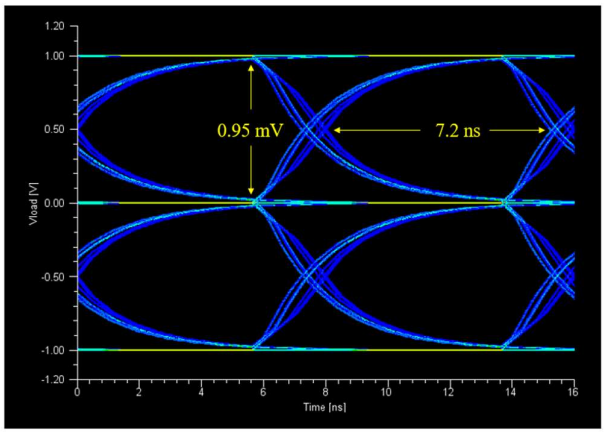
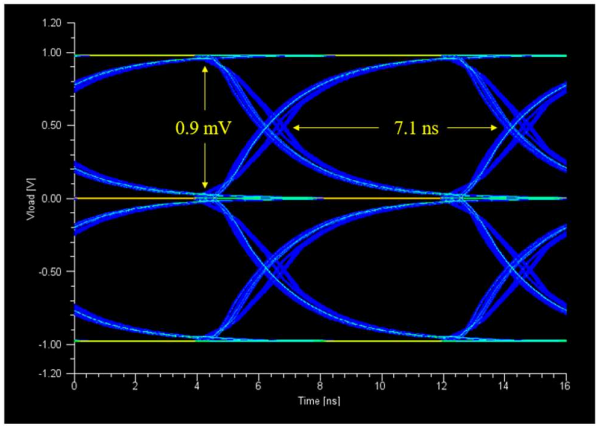


Fig. 9. Configuration for MLT-3 application considering a differential microstrip line of variable length as transmission path.



(a)



(b)

Fig. 10. Eye diagrams resulting from a standard differential load in cascade with (a) a 1 cm microstrip line, and (b) a 10 cm microstrip line.

B. Time-Domain and Frequency-Domain Analysis

As carried out in the previous sections, time and frequency analyses are developed to estimate the compliance of the simulated signal with the signal required by regulations.

The time domain analysis reported in Fig. 7 shows that the signal generated considering the RC filter is an improved version that matches considerably better the MLT-3 signal reported in [13]. The comparison shown in Fig. 8 additionally confirms that this signal satisfactorily mimics the frequency spectrum of the measured signal [15].

The improved circuit model, by selecting a sampling frequency of 125 MHz and introducing an RC filter at the output of the encoding stage, is therefore deemed to carry out simulation at design stage, thus allowing a preliminary study to assess how the system responds to an input MLT-3 signal that introduces disturbances relevant to EMC and SI analysis.

V. Application

To test the performance of the signal generation circuit in a real application, the MLT-3 signal provided by the improved model was applied to a transmission path consisting of a differential microstrip line, as described in Fig.9. Two different configurations were simulated, varying the length of the line from 1 cm to 10 cm. The results are presented in Fig. 10(a) and (b) in the form of eye-diagrams. It is observed by comparing the two graphs that by increasing the length of the trace, the eye height is reduced, as is expected from the SI theory.

The result confirms the validity of the proposed model to conduct an efficient SI analysis at design level. The proposed lengths were selected by considering real-world applications where microstrip lines longer than 10 cm are unlikely to be used; however, since the model behavior is consistent with theory, fair outcomes are also expected considering different transmission paths, e.g., an Ethernet twisted-wire pair cable.

VI. Conclusion

In this work, a circuit model simulating the performance of MLT-3 coding for EMC and SI simulations has been proposed. The principle scheme was derived directly from considering the standards governing the design of the physical layer of the 100 Mbps Ethernet transmission network. The selection of the sampling frequency is made in order not to return a theoretically correct sampling, but to ensure that the output signal exhibits a pattern that highlights possible electromagnetic interference issues. The aim is to obtain a frequency spectrum that counts the harmonic content of a real MLT-3 encoded signal.

An improved model is developed by adding an RC filter at the output of the encoding stage. The model behavior is then simulated in the time and frequency domain. The time domain analysis justifies the choice of a sampling frequency of 125 MHz and the implementation of the RC filter to include the effects of signal rise and fall times on the output. The frequency-domain simulation reveals an excellent agreement with the spectrum of the measured MLT-3 signal.

The proposed circuit is a simple model that can be implemented in any circuit simulation software. It makes it possible to intervene at design level in the event of EMC or SI problems, thus saving costs and time. For instance, the proposed method can be readily combined with the Ethernet cable model in [17] for system-level prediction.

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