Frequency Synchronization Techniques for DC-DC Converters with Time-Based Control

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***Abstract*—In this brief, a frequency synchronization method for time-based-controlled power converters is presented. The proposed synchronization technique makes it possible to precisely lock the internal oscillators frequency of the time-based controller (i.e., the power converter switching frequency) to any externally provided clock signal, without trading the dynamic performance. By leveraging the differential structure of the time-based controller, the proposed feedback loop operates orthogonally with respect to the main voltage regulation loop, minimizing any interaction with the latter. The presented frequency synchronization scheme has been implemented on a time-based buck converter in a 180-nm BCD process to fully verify the performance.**

***Index Terms*—Dc-dc converter, buck converter, time-based control, phase-locked-loop, frequency synchronization.**

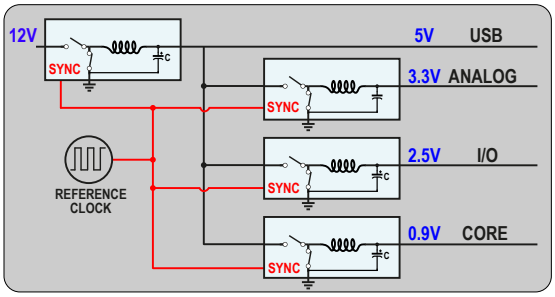

Fig. 1. Exemplary power distribution tree for a 12 V bus with external clock synchronization.

I. Introduction

Nowadays DC-DC converters and power-management-integrated-circuits (PMICs) require high flexibility, low cost, and small form factors. Time-based signal processing, first introduced in [1], was demonstrated as an effective alternative to conventional voltage-based and digital signal processing. Because it stores information in the time difference between two events, the time-based controller uses digital-level signals, taking advantage of technology scaling (low power consumption and area occupation) without introducing quantization. In recent years, this control topology has been extended to a variety of applications, proving the effectiveness of this method [2], [3], [4], [5], [6], [7], [8], [9]. Essentially, the voltage error is converted into a time difference between two events and is processed in the time-domain. The voltage-to-time conversion is achieved through a voltage-controlled oscillator (VCO) and a voltage-controlled delay line (VCDL). The converter switching frequency is internally generated by the time-based control using the VCO. Although its value is selected by design, unavoidable process variation can cause the switching frequency to slightly offset from the target value. This behavior poses a challenge when multiple DC-DC converters are utilized in PMICs or system on chip (SoC) to generate these supply rails, as shown in Fig. 1. Indeed, two key challenges are managing switching noise that can propagate through the power distribution network [10], [11] and limiting the electromagnetic emissions. Beat frequencies corresponding to the differences between the frequencies of the various DC-DC converters could be easily reduced by synchronizing all the regulators with an external clock [10]. This strategy ensures predictable operation within a controlled frequency range, enabling designers to minimize EMI, simplify filtering, and improve the power distribution in complex, multi-rail environments. Moreover, external synchronization enables a simple method for performing spread-spectrum frequency modulation (SSFM) [12], [13], [14] and dynamic frequency scaling (DFS) [15], [16], [17], [18], thereby allowing for a reduction in the system's power consumption.

When using a standard voltage-based or digital control, switching frequency synchronization is straightforward, as both controllers rely on a single oscillator that is not involved in the controller transfer function. The switching frequency can thus be easily linked to that of an external clock. In time-based compensators, the oscillator (i.e., VCO) sets the integral gain, making frequency alignment to an external clock nontrivial. In this paper, we introduce a frequency synchronization technique for power converters featuring time-based control. The proposed synchronization mechanism is based on a phase-locked loop (PLL), which operates on the common mode frequency of the VCOs without affecting the output voltage regulation loop, which operates on the differential frequency of the VCOs. This paper is organized as follows: in Sect. II the time-based control applied to a buck DC-DC converter is introduced. In Sect. III the system specifications are discussed, and the design choices related to a frequency-locked loop (FLL) and a PLL architecture are analyzed. Sect. IV provides experimental results from the prototype buck converter. Conclusions are drawn in Sect. V.

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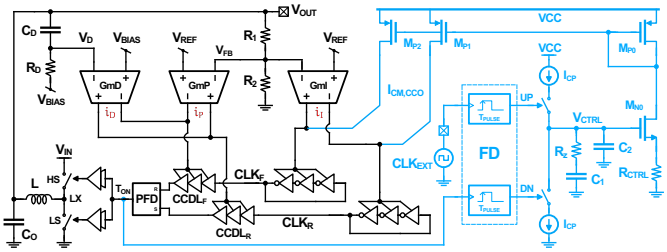


Fig. 2. Block diagram of a time-based buck converter (black) with external clock synchronization using a frequency-locked loop (light blue).

II. Time-Based Control

The simplified schematic diagram of a time-based compensator applied to a buck converter is shown in black in Fig. 2. The controller is composed of two main building blocks: a differential VCO and a VCDL. The output voltage is downscaled by a resistive divider with gain $1/N = R_2/(R_1+R_2)$, which produces a voltage, V_{FB}. This signal feeds the current-controlled oscillators (CCOs) by means of the transconductor $G_{m\text{I}}$ and the current controlled delay lines (CCDLs) utilizing the transconductor $G_{m\text{P}}$. The derivative transfer function is implemented in the voltage domain employing the high-pass filter $C_{\text{D}}R_{\text{D}}$. The high-pass filter output is fed to the transconductor $G_{m\text{D}}$ to generate the current i_{D} to the CCDLs. The time-based controller implements a PID transfer function, which can be written as [7]:

$$G_{\text{T}_{\text{PID}}}(s) = \frac{K_{\text{I}}}{s} + K_{\text{P}} + sK_{\text{D}}, \tag{1}$$

with

$$K_{\text{I}} = G_{m\text{I}} \cdot K_{\text{CCO}} \tag{2a}$$

$$K_{\text{P}} = G_{m\text{P}} \cdot K_{\text{CCDL}} \tag{2b}$$

$$K_{\text{D}} = N \cdot \frac{G_{m\text{D}}}{\omega_{\text{D}}} \cdot K_{\text{CCDL}}, \tag{2c}$$

where K_{CCO} is the CCO gain expressed in [rad/A·s], K_{CCDL} is the CCDL gain expressed in [rad/A] and $\omega_{\text{D}} = (R_{\text{D}}C_{\text{D}})^{-1}$ is the angular frequency of the high-pass filter pole. The phase-frequency detector (PFD) compares the two CCDL outputs and generates the PWM signal, with a gain $G_{PFD} = 1/2\pi$. When using this type of compensator, the converter switching frequency, f_{SW}, is generated inside the converter by properly setting the common mode bias of the CCOs.

III. External Frequency Alignment Architecture

A. FLL Implementation

A FLL can be used to force the DC-DC converter to operate at a frequency imposed by an external clock, CLK_{EXT}, having a frequency f_{ext}. A possible implementation can be obtained by sensing the PFD output and comparing its frequency, f_{SW}, with f_{ext} using a frequency detector (FD). The FD takes as inputs the external clock waveform and the PFD output. It connects them to a pulse generator, which generates the UP signal and DN signals in Fig. 2 that are used to drive a charge-pump (CP). The adoption of a pulse generator is necessary to ensure the FLL's correct operation, regardless of the duty

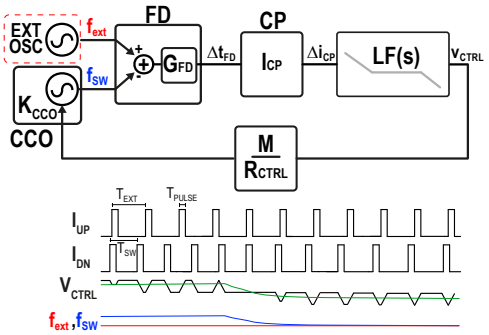


Fig. 3. Small signal model of the frequency-locked loop (top) and relevant signals during a transient where f_{SW} is higher than f_{ext} (bottom).

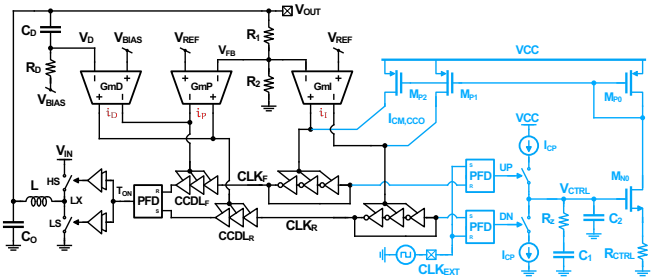


Fig. 4. Block diagram of a time-based buck converter with the proposed phase-locked loop.

cycles of the two clock signals. The average current at the charge pump output is:

$$\overline{I_{\text{CP}}} = I_{\text{CP}} \cdot T_{\text{PULSE}} \cdot (f_{\text{ext}} - f_{\text{SW}}), \tag{3}$$

where $T_{\text{PULSE}} = T_{\text{UP}} = T_{\text{DN}}$ is the duration of the pulses generated by the FD block, and I_{CP} is the CP current. This current is injected in a loop filter composed of a capacitor C_2 in parallel to the series of the capacitor C_1 and the resistance R_z such that the loop filter impedance $Z_{\text{LF}}(s)$ is:

$$Z_{\text{LF}}(s) = \frac{1 + sC_1R_z}{s(C_1+C_2)\left(1 + s\frac{C_1C_2}{C_1+C_2} \cdot R_z\right)}. \tag{4}$$

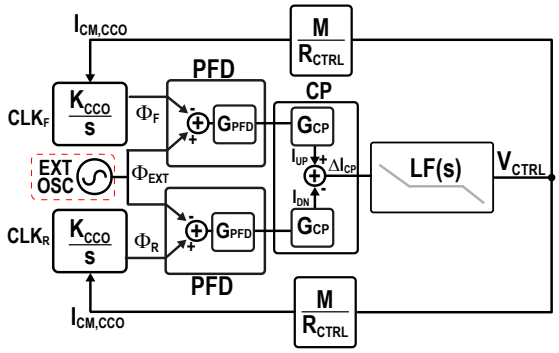
The filter output voltage V_{CTRL} is buffered to the resistance R_{CTRL}, to generate a control current. This current is mirrored with a gain factor M and is used to modulate the bias current, i.e. the common-mode of the two oscillators. The overall transfer function $T(s)$ of the FLL can be written as:

$$T(s) = G_{\text{FD}} \cdot I_{\text{CP}} \cdot Z_{\text{LF}}(s) \cdot \frac{M}{R_{\text{CTRL}}} \cdot K_{\text{CCO}}, \tag{5}$$

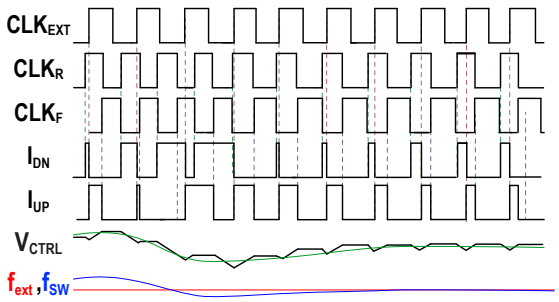
where $G_{\text{FD}} = T_{\text{PULSE}}$ is the gain of the frequency detector. Due to the integral action performed by the CP combined with the loop-filter, the FLL locks with $f_{\text{SW}} = f_{ext}$. The block diagram of the small signal model of the FLL is shown in Fig. 3, along with the relevant waveforms.

Although this solution effectively locks the power converter's switching frequency to the external clock frequency, it has two main drawbacks:

- The frequency regulation loop interacts with the voltage regulation loop;



(a)



(b)

Fig. 5. (a) Phase domain small signal model of the proposed phase locking method. (b) Timing diagram of relevant signals during a frequency variation.

- Mismatches in the FD and the CP have a direct impact on the steady-state frequency offset when the system is locked.

Regarding the first problem, it can be observed that, during transients, the time-based controller differentially alters the VCO output frequencies to establish the phase shift necessary to maintain output voltage regulation. Since the FLL uses the PFD rising-edge to generate the charge-pump pulse, there is an unavoidable interaction between the main voltage loop and the FLL. To avoid stability issues, the FLL should be designed with a bandwidth much lower than that of the voltage regulation loop, thus preventing the solution from being used when DFS is required.

Additionally, mismatches and non-idealities between the two pulse generators of the FD, as well as the offset between the up and down current sources (I_{CP}) inside the CP, are responsible for frequency offset, which can result in a beat frequency when multiple switching modules are used in a power tree. Indeed, if we assume a mismatch in the CP currents, ΔI_{CP}, and a mismatch in the pulse widths, ΔT_{PULSE}, the locking condition will be:

$$f_{\text{SW}} \simeq \frac{f_{ext}}{\left(1+\frac{\Delta I_{\text{CP}}}{I_{\text{CP}}}\right)\left(1+\frac{\Delta T_{\text{PULSE}}}{T_{\text{PULSE}}}\right)}, \tag{6}$$

leading to a first-order frequency error, f_e, given by:

$$f_e \simeq -f_{\text{ext}} \cdot \left(\frac{\Delta T_{\text{PULSE}}}{T_{\text{PULSE}}}+\frac{\Delta I_{\text{CP}}}{I_{\text{CP}}}\right) \tag{7}$$

B. PLL Implementation

To overcome these limitations, the architecture, shown in Fig. 4, is proposed.

Using two PFDs, that is, two SET/RESET flip-flops (FFs) instead of a simple FD, the controller now operates as a PLL. The upper PFD, employed to generate the up signal, is set by the CLK_{EXT} rising edge and is reset by CLK_{F}, having a frequency f_F. Similarly, the PFD used to generate the DN signal is set by CLK_{R}, with a switching frequency f_R, and it is reset by CLK_{EXT}. The phase domain small signal model and the waveforms of the proposed architecture are shown in Fig. 5.

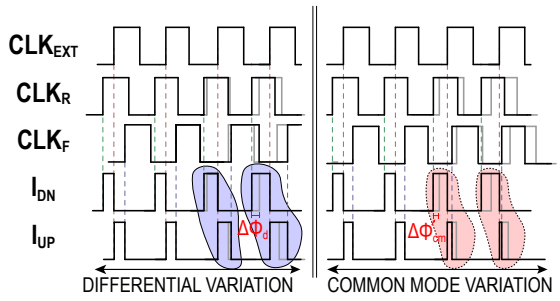


Fig. 6. Relevant waveforms during a differential-mode (left) and a common-mode (right) variation of CLK_R and CLK_F frequencies. $\Delta\Phi$ is the phase difference accumulated by a clock signal, compared to the unperturbed case (gray line).

Taking into account the integral action of voltage to phase of CCOs, the loop transfer function, T_2, can be written as:

$$T_2(s) = G_{\text{PFD}} \cdot G_{\text{CP}} \cdot Z_{\text{LF}}(s) \cdot \frac{M}{R_{\text{CTRL}}} \cdot \frac{K_{\text{CCO}}}{s}, \tag{8}$$

where $\text{G}_{\text{PFD}} = 1/2\pi$ and $\text{G}_{\text{CP}} = \text{I}_{\text{CP}}$. Due to the presence of two integrators in the loop (i.e., the CCO and the loop filter) at steady state, the following equality holds:

$$\Phi_{\text{F}} - \Phi_{\text{EXT}} = \Phi_{\text{EXT}} - \Phi_{\text{R}} \implies \frac{\Phi_{\text{R}}+\Phi_{\text{F}}}{2} = \Phi_{\text{EXT}} \tag{9}$$

Essentially, the average charge injected into the loop filter is zero if the rising edge of CLK_{R} and CLK_{F} are symmetrical with respect to the rising edge of CLK_{EXT} . In this way, the synchronization loop is insensitive to the differential frequency variations produced during line, load, as well as any other transients in the DC-DC converter. By applying a differential signal, $\Delta\Phi_d$, it is possible to write

$$\frac{\Phi_{\text{R}}+\Delta\Phi_d+\Phi_{\text{F}}-\Delta\Phi_d}{2} = \Phi_{\text{EXT}}, \tag{10}$$

meaning that the average $I_{\text{CM,CCO}}$ remains unchanged, as shown in Fig. 6 (left). On the other hand, when the external clock imposes a common mode variation, $\Delta\phi_{cm}$, the proposed loop reacts to lock the controller frequency to the external one, as shown in Fig. 6 (right). This means that, if a perfect matching between the reference and the feedback signal path exists, the cross-gain between the two control loops is zero. In reality, due to unavoidable mismatches such as the one

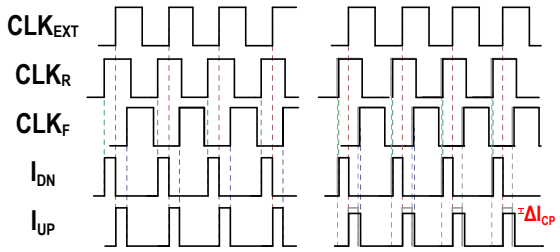


Fig. 7. Timing diagram in locked conditions without (left) and with (right) charge-pump currents mismatch.

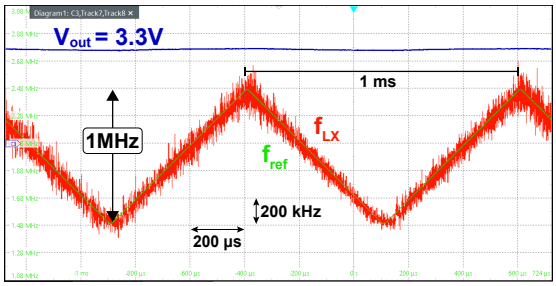


Fig. 8. Measured switching frequency of the converter when the external clock frequency is modulated with a 1ms period triangular profile having a 1MHz modulation amplitude from 1.5MHz to 2.5MHz.

between the two KCCOs, a finite interaction between the loops occurs, but its magnitude in practice is so small that it doesn't affect the stability of the two controllers. This structure also has the advantage of being insensitive to any offset in the CP. Considering a current mismatch such that the current of the upper current source is $I_{\mathrm{CP}} - \Delta I_{\mathrm{CP}}$, the system will lock to the following steady state condition:

$$(\Phi_{\mathrm{R}} - \Phi_{\mathrm{EXT}})\, I_{\mathrm{CP}} = (\Phi_{\mathrm{EXT}} - \Phi_{\mathrm{F}})\,(I_{\mathrm{CP}} - \Delta I_{\mathrm{CP}}) \rightarrow$$
$$\rightarrow \Phi_{\mathrm{EXT}} = \frac{\Phi_{\mathrm{R}} + \Phi_{\mathrm{F}}\left(1 - \frac{\Delta I_{\mathrm{CP}}}{I_{\mathrm{CP}}}\right)}{2\left(1 - \frac{\Delta I_{\mathrm{CP}}}{2I_{\mathrm{CP}}}\right)}. \quad (11)$$

Being a PLL, any asymmetries in the CP would only impact the phase difference between the $\mathrm{CLK_{EXT}}$ (as shown in Fig. 7), $\mathrm{CLK_R}$, and $\mathrm{CLK_F}$, while still having a perfectly locked frequency. In turn, in time-based converters, f_{SW} is affected by process, voltage, and temperature (PVT) variations. The proposed frequency synchronization loop overcomes this limitation, guaranteeing precise operation at a given frequency regardless of PVT variations. The PWM signal generated by the voltage control loop, however, is not aligned with the rising edge of the external clock. This means the proposed technique is not suitable for applications that require edge synchronization.

IV. Measurement Results

A prototype time-based controlled buck with enhanced frequency-synchronization loop was realized in a 180nm BCD process. The buck converter generates a regulated output voltage, V_{OUT}, of 3.3V from an input voltage, V_{IN}, ranging from 5V to 32V, providing a maximum load current of 1.4A. The internal f_{SW} generated by the CCOs is set to 2.4 MHz. The

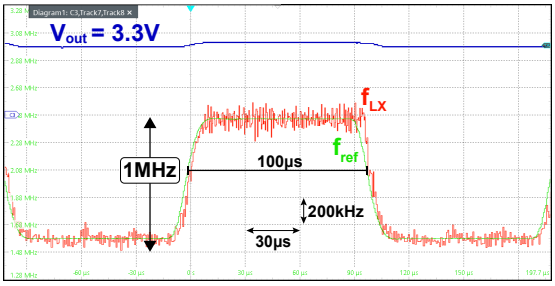


Fig. 9. Measured switching frequency of the converter when the external clock frequency is modulated with a 10μs rising time step-like frequency variation of 1 MHz, spanning from 1.5 MHz to 2.5 MHz.

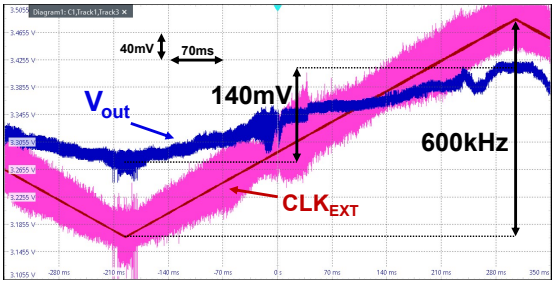


Fig. 10. Measured output voltage variation when a slow 600kHz frequency variation is applied.

PLL loop has been designed based on the linear time-invariant model in (8), which results in an accurate design since the target closed loop bandwidth of the frequency loop is $f_{SW}/20$. The proposed frequency synchronization loop consumes 12µA (locked at 2.4MHz) from the internal supply of 1.8V, which remains negligible with respect to the consumption of the whole DC-DC converter. To perform the measurements, the Agilent 33220A waveform generator is used to feed the buck with a clock signal having different modulation profiles, while the RTO2014 oscilloscope monitors such clock signal as well as the buck switch node (LX), directly displaying the real-time processed frequency information. All the measurement results included in this section are obtained for the nominal operating point of V_{IN}=12V. Figure 8 demonstrates the converter's ability to track a switching frequency modulation profile with a triangular waveform having a period of 1ms. The frequency modulation has an amplitude of 1 MHz, ranging from 1.5 to 2.5 MHz. Fig. 9 shows the tracking response when a step-like variation of 1MHz (1MHz/10μs is the limit of our instrumentation) with a period of 200μs is applied to the external clock. To assess the output voltage accuracy, the output voltage variation was measured when a 600kHz frequency ramp was used as an external clock signal, as shown in Fig. 10. The system displays an output-voltage regulation error of 0.23 mV/kHz. Figure 11 shows the superposition of the voltage spectrum when the PLL loop is off (red curve) and on (green curve). The PLL loop is able to narrow the switching frequency spur and correctly provide frequency synchronization. The measurement in Fig.12 shows the transient response to a 0.5A load step when the FLL loop is activated (purple) or deactivated (green). The two transient responses are highly similar, thus verifying that the PLL loop has negligible interaction with the main

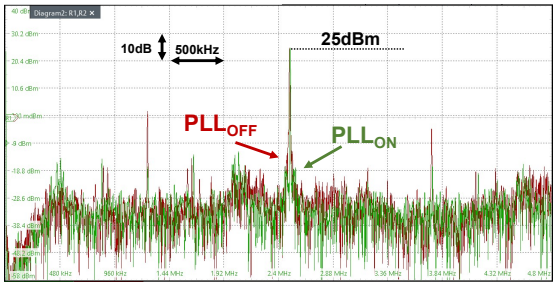


Fig. 11. Measured voltage spectrum of the inductor switching node "Lx" with (green) and without (red) the PLL active.

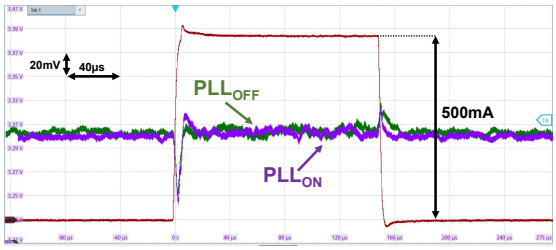


Fig. 12. Measured load step response of the converter with (purple) and without (green) the PLL enabled.

output voltage regulation loop. The die micrograph is shown in Fig. 13, highlighting the area occupation of the proposed PLL (clock synch) and of the time-based voltage control (T-PID). With reference to Fig. 4, the only components off-chip are L, C_0, and the source of the external clock CLK_{EXT}.

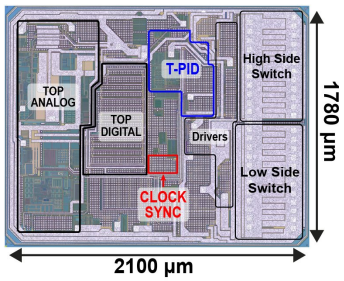


Fig. 13. Die micrograph of the fabricated PMIC. The T-PID and the clock synchronization loop are highlighted in blue and red, respectively.

V. Conclusion

In this paper, a specific method to synchronize the switching frequency of a DC-DC power converter with time-based control has been presented. Two possible implementations of the frequency synchronization loop have been described. Among them, the proposed PLL implementation, being orthogonal to the primary voltage loop, does not ideally impact either the stability or the dynamic performances of the converter. The proposed auxiliary loop design is not critical and it is insensitive to mismatch or PVT variations in the CP and the PFDs. A prototype buck converter with time-based compensator was realized. Using an external signal, we have demonstrated that the converter can track a 1ms period triangular/sinusoidal profile and a fast 1MHz/10μs step frequency variation.

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