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Low-Noise Quantum Dots in Ultra-Shallow Ge/SiGe Heterostructures for Prototyping Hybrid Semiconducting-Superconducting Devices

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Planar germanium is currently the only semiconducting platform where high-coherence spin qubits and proximity-induced superconductivity have each been demonstrated. Recent research into spin qubits in Ge/SiGe heterostructures has focused on increasing the thickness of the SiGe capping layer, reporting improvements in the electrostatic noise levels. Meanwhile, heterostructures with thinner capping layers remain rather unexplored, despite the potential advantages for proximity-induced superconductivity. Here, we study a Ge/SiGe heterostructure with a thin SiGe cap $d \approx 4\,\mathrm{nm}$ and investigate its viability to host low noise quantum dots. To keep the thermal budget compatible with superconducting layers, low-temperature oxide deposition processes were developed and implemented for the gate dielectrics. The charge noise level of fabricated devices is estimated to be $1.8 \pm 1.0\,\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$, comparable to devices fabricated on shallow heterostructures ($d \sim 20\,\mathrm{nm}$) with high-temperature deposited oxides. Low charge-noise levels, together with the straightforward integration of superconductors, make this heterostructure an attractive platform for prototyping hybrid semiconducting–superconducting devices.

Quantum devices based on hybrid semiconductor-superconductor technology have been gaining increasing attention in the past decade, strongly motivated by proposals related to topological superconductivity[1] and novel types of spin qubits[2]. So far, most of the research has focused on group III-V semiconductors, with prominent directions including studies of proximity-induced subgap states[3], Cooper Pair Splitters[4,5] and engineered Kitaev chains[6,7]. However, hybrid devices that use the spin degree of freedom, e.g., Andreev Spin Qubits[8,9], exhibit short coherence times due to the interaction with the nuclear spins of the host lattice. This motivates the search for another semiconducting platform with low hyperfine interaction and compatibility with proximity-induced superconductivity. Ge/SiGe heterostructures[10] are such a platform, as they can host spin qubits with long coherence times[11,12] and allow for induced superconducting order[13–17].

Existing Ge/SiGe heterostructures typically place the Ge quantum well $\sim 20\,\mathrm{nm}$–$100\,\mathrm{nm}$ below the surface[18]. It has been demonstrated that the charge noise levels – one of the limiting factors for hole spin qubit coherence times[19] – reduce from the level of $1.4\,\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ for a shallow heterostructure ($d \approx 22\,\mathrm{nm}$)[13] to $0.6\,\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ in a deeper $d \approx 55\,\mathrm{nm}$ heterostructure[20]. This finding suggests that thicker capping layers are preferable, provided that quantum dots (QDs) can still be electrostatically defined. For shallow or deep heterostructures, the procedure of bringing a superconductor into the proximity to the quantum well typically relies on either annealing[13,16,21] or etching[14,15] through the cap. If, however, the capping layer is sufficiently thin ($\approx 4\,\mathrm{nm}$), proximity-induced superconductivity can be achieved by directly depositing a superconducting film onto the surface of the heterostructure after native oxide removal[17]. A drawback of this approach is that it brings the quantum well much closer to the surface, potentially increasing electrostatic noise levels due to coupling to interface and oxide traps. As such, the approach raises a key question: can an ultra-shallow ($\approx 4\,\mathrm{nm}$) Ge/SiGe heterostructure host QDs with charge noise levels suitable for spin qubits with long coherence times?

Beyond the considerations of the capping layer thickness, a hybrid platform introduces another challenge related to the reduction of the thermal budget once the superconducting layer is deposited. A standard spin qubit fabrication flow involves the atomic layer deposition (ALD) of gate oxide, typically performed at $\approx 300\,^\circ\mathrm{C}$[12,22]. Such high temperatures can cause undesired interdiffusion and reactions at the superconductor–semiconductor interface[23]. To maintain control over the superconducting layer during fabrication, low-temperature ALD ($< 150\,^\circ\mathrm{C}$) is therefore required. A few studies have already demonstrated QDs with reduced

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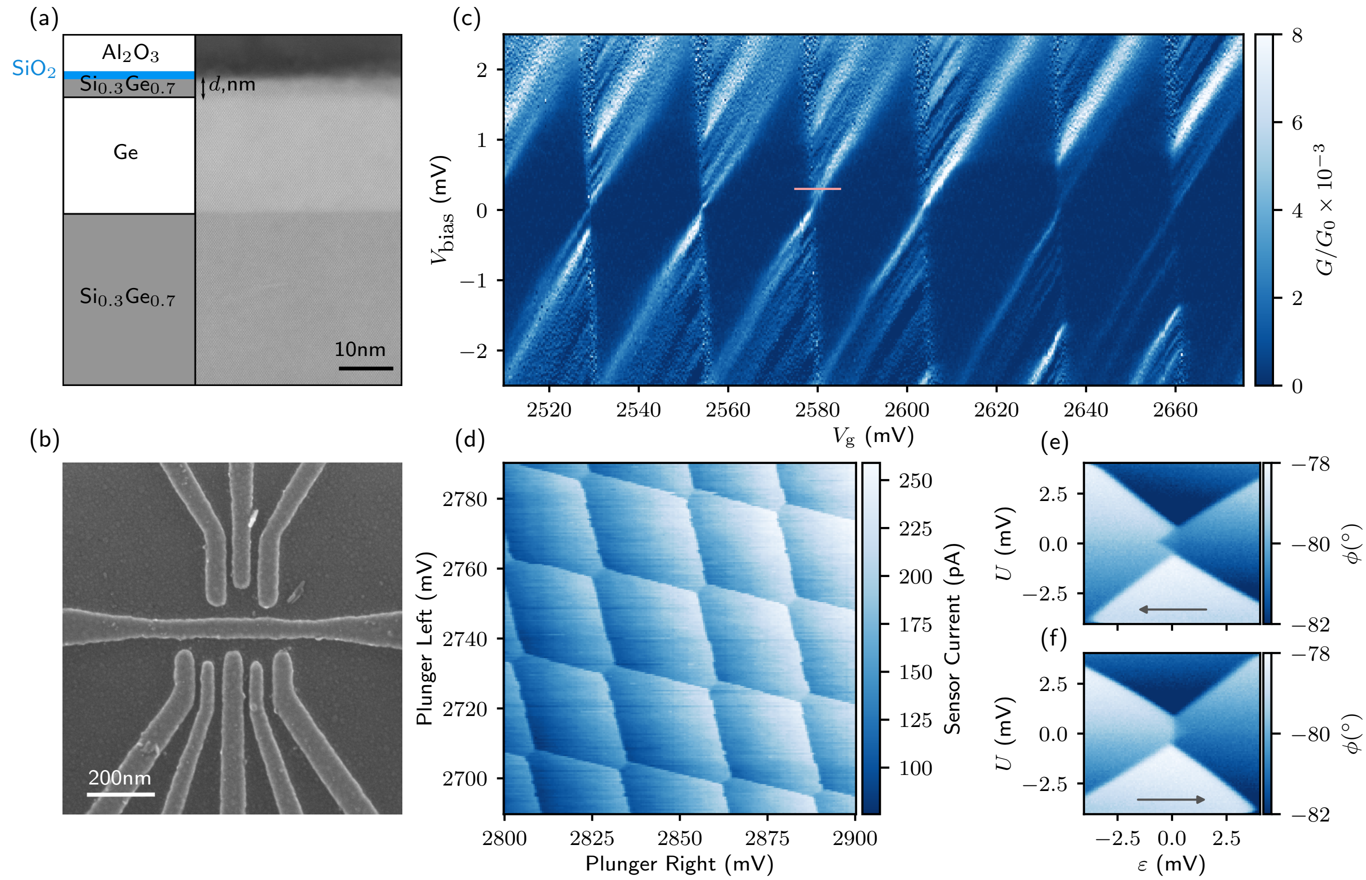

FIG. 1. QDs on an ultra-shallow Ge/SiGe heterostructure. (a) HAADF-STEM of the Ge/SiGe heterostructure with the Al_2O_3 oxide deposited on top. The estimated cap thickness is $d \approx 4\,\mathrm{nm}$. (b) SEM of a device lithographically identical to Device A. (c) Coulomb diamonds of the left QD. V_{bias} is the external voltage and G is the conductance calculated as a numerical derivative of the current I. The presented data is not corrected for the series resistance R_{in}. Pink cut indicates the gate voltage span over which the time traces in Fig. 2 were taken. (d) DQD stability diagram measured with the charge sensor. (e-f) Fast scans over the virtual detuning ε and energy U axes of the DQD. The charge occupation of the dots is measured by using a reflectometry circuit analogous to the one used in Ref[12]. The pulsing directions are indicated by the arrows. An out-of-plane magnetic field $B_\perp \approx 5\,\mathrm{mT}$ was applied.

temperature ALD oxides[21,24]. Yet, to the best of our knowledge, their charge-noise performance has not been systematically characterized.

In this work, we address both of these two challenges by characterizing QDs fabricated on an ultra-shallow Ge/SiGe heterostructure with a $d \approx 4\,\mathrm{nm}$ SiGe spacer and using low-temperature ($\sim 100\,°\mathrm{C} - 150\,°\mathrm{C}$) ALD oxides. We demonstrate that the studied platform can be used for stable QDs, and the electrostatic noise assessment reveals noise levels comparable to those on shallow cap ($\sim 20\,\mathrm{nm}$) wafers and with high-temperature ALD oxides.

We fabricated two types of devices, dubbed Device A and Device B. Both are fabricated on the same wafer, with the SiGe cap grown to be within $3\,\mathrm{nm} - 5.5\,\mathrm{nm}$. The Atomic resolution high-angle annular dark field (HAADF) - scanning transmission electron microscopy (STEM) image is shown in Fig. 1a. Details on the wafer growth and its properties can be found in Ref.17. Device A is a double quantum dot (DQD) with a charge sensor; the scanning electron microscopy (SEM) image of it is shown in Fig. 1b. Device B is a single QD, see SEM and transport data in supplementary information (SI), Sec. 2. As a comparison, we also measured transport through the charge sensor used in the spin qubit experiment of Ref.25 (dubbed Device C), where the SiGe cap is $d \approx 20\,\mathrm{nm}$.

Devices A and B have the same fabrication stack except for the ALD-grown oxide: Device A has HfO_2 grown at $150\,°\mathrm{C}$, while Device B has Al_2O_3 grown at $100\,°\mathrm{C}$. Details on the fabrication and layout of Device C are given in Ref.25. The oxide recipes for devices A and B are adapted from the high-temperature ones used in Refs.12 and 25 (Device C) to the low-temperature deposition by extending the deposition times. We observed that extending deposition times is crucially important to counteract low gas kinetics due to the reduced temperature (see SI, Sec. 1 for the fabrication details and discussion within).

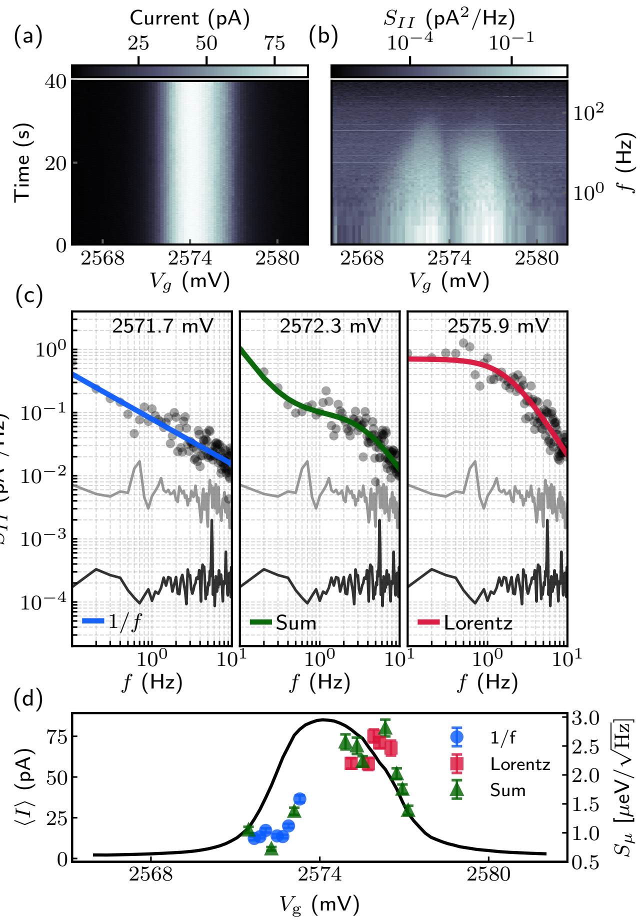

FIG. 2. Noise analysis across a Coulomb peak. (a) Time traces of current across the Coulomb peak. The remarkable stability is demonstrated within the ≈ 1 hour data recording window. The external voltage bias V_{bias} is set to $270\,\mu$V. The voltage drop V_{SD} over the QD changes by $\approx 30\%$ due to the TIA input resistance $R_{\mathrm{in}} \approx 1\,\mathrm{M}\Omega$. (b) PSD estimated via the Welch method for each of the plunger gate voltages V_{g}. The horizontal lines, independent of the plunger gate voltage V_{g}, are attributed either to mechanical vibrations or to the 50 Hz harmonics. (c) Traces demonstrating different spectral behavior (black dots) with the corresponding fit (blue, green, red curves). The corresponding voltage V_{g} at which the traces are taken are indicated at the top. For all subpanels we plot the PSD in the Coulomb blockade (black) and on top of the Coulomb peak (gray). (d) Averaged current $\langle I(V_{\mathrm{g}})\rangle$ (left axis) and electrochemical potential noise density S_μ (right axis) evaluated at 1 Hz. The colorcoding of the points is the same as in panel c. The error bars correspond to the fitting errors.

We showcase full functionality of Device A in Fig. 1c-f. In Fig. 1c the stability diagram of the left dot are presented; similar measurements for the right and sensor dots can be found in SI, Sec. 2. For all the QDs we find the charging energy to be within the range $E_{\mathrm{C}} \sim 1.5\,\mathrm{meV} - 3\,\mathrm{meV}$, similar to the QDs fabricated on thicker cap wafers[12,25]. The lowest excited states are found to have orbital energies $E_{\mathrm{orb}} \sim 0.2\,\mathrm{meV} - 0.3\,\mathrm{meV}$. In Fig. 1d we present a DQD stability diagram measured via the current response of the charge sensor dot. As shown in Fig. 1d, the transition lines for both dots are roughly equidistant and correspond to the addition energy equal to the charging energy $E_{\mathrm{add}} \approx E_C$, which implies that the effect of level quantization is not visible yet. We attribute it to the high charge density in both dots. Lithographic squeezing of the dots, surface treatment[26], control of the fixed oxide charge[27] or multi-layer gate structures[28] would be further required to reach the few-hole regime. Nevertheless, we demonstrate full charge control via fast gates in Fig. 1e-f, where, following Ref.29, we pulse through the DQD transition across the virtual detuning and energy axes. We observe charge triangles, which we attribute to charge latching rather than Pauli spin blockade, since the effect appears on both sides of the charge transition (although it is more pronounced on one side).

We now turn to assessing the electrostatic noise levels for Devices A, B, and C. It is commonly argued that the dominant source of low-frequency charge noise stems from two-level fluctuators (TLFs)[30], which leads to the spin-qubits' decoherence[31] and reduced two-qubit gate fidelities[32]. In order to characterize the noise performance of the ultra-shallow platform, we use the widely accepted metric: the electrochemical potential noise density S_μ at 1 Hz[20,33–36].

We estimate the noise levels using the so-called flank method[20,37–39]. The detailed description of data acquisition and analysis can be found in the SI, Sec. 3; here we outline the main steps of the procedure. First, we collect time traces of the current $I(t)$ through the QD across a Coulomb peak at a constant external bias voltage V_{bias}. In Fig. 2a, we plot time traces corresponding to the 3rd Coulomb resonance of the dataset presented in Fig. 1c (Device A). The voltage drop over the quantum dot $V_{\mathrm{SD}} = V_{\mathrm{bias}} - IR_{\mathrm{in}}$ is not kept constant due to the input resistance $R_{\mathrm{in}} \approx 1\,\mathrm{M}\Omega$ of our transimpedance amplifier (TIA). Some datasets were additionally measured with $R_{\mathrm{in}} \approx 100\,\mathrm{k}\Omega$ with no qualitative difference found (see SI, Sec. 6 for further details).

The PSD traces $S_{II}(f, V_{\mathrm{g}})$ for each plunger gate voltage V_{g}, estimated using the Welch method, are shown as a 2D map in Fig. 2b. A pronounced dip in low-frequency noise power is observed at the top of the Coulomb peak ($V_{\mathrm{g}} = 2574\,\mathrm{mV}$), where the transconductance $\partial I/\partial V_{\mathrm{g}}$ approaches zero. Since the contribution of the electrochemical potential fluctuations $\delta\mu(t)$ to the current fluctuations $\delta I(t)$ vanishes at zero transconductance, the noise spectrum – both at the top of the peak and deep in the Coulomb blockade – is expected to be dominated by the noise added by the TIA[20,37]. The substantial difference between the noise levels measured at the peak top and in blockade (black and gray traces in Fig. 2c) reflects the strong dependence of the TIA-added noise on the load impedance seen by the amplifier. A rigorous subtraction of the TIA noise would therefore require independent measurements of the device differential conductance, as well as the noise of the TIA for that specific load impedance. Such a procedure is beyond the scope of this work, and we therefore do not subtract the TIA-added noise explicitly. Nevertheless, for the noise levels measured in our devices, quantitative conclusions can be drawn without this detailed characterization, as we discuss below.

While the standard TIA noise model includes equivalent input current and voltage noise sources, as well as Johnson-Nyquist noise from the feedback resistor[40], in our TIA, there is an additional contribution associated with the input impedance of the amplifier $R_{\text{in}} \approx 1\,\text{M}\Omega$ (or $R_{\text{in}} \approx 100\,\text{k}\Omega$, depending on the configuration). As a result, the total input-referred current noise not only increases monotonically as the load impedance decreases, but also saturates at its largest value when the device resistance is minimal and the load impedance is dominated by R_{in} (see SI, Sec. 4). We observe that the measured noise at the top of the Coulomb peak approaches the maximal TIA-added noise and use this spectrum as an empirical reference to select spectra acquired on the flanks for further analysis. More concretely, only those spectra whose noise level exceeds the peak-top reference in the frequency range from 100 mHz to 10 Hz are retained. The frequency window is chosen for the subsequent fits such that it spans around the frequency of interest of 1 Hz, while remaining well separated from the TIA roll-off at higher frequencies (≈ 30 Hz). Nearly all spectra selected in this way also exceed the maximal saturate TIA noise at 1 Hz, indicating that the extracted noise is predominantly of the device origin.

A large fraction of the selected PSD trends S_{II} cannot be fitted purely by the $1/f^{\beta}$ function. This is expected if the contribution of a single TLF is dominant over the distribution of TLFs[32] and has already been observed in Refs.35 and 39. Following Ref.35, we define three models:

$$S_{1/f}(f) = \frac{A}{f^{\beta}}, \tag{1}$$

$$S_{\text{Lorentz}}(f) = \frac{B}{(f/f_0)^2 + 1}, \tag{2}$$

$$S_{\text{Sum}}(f) = \frac{A}{f^{\beta}} + \frac{B}{(f/f_0)^2 + 1}, \tag{3}$$

where A, B, β, f_0 are the fitting parameters. Eq. (1) describes the spectrum of the TLF distribution, Eq. (2) a single TLF, and Eq. (3) captures the contribution of both. We fit all three models and select the one that minimizes the Bayesian Information Criterion (BIC), which penalizes models with more fitting parameters. In Fig. 2c examples of the fits for three values of V_{g} are demonstrated. A clear distinction in the PSD trends is observed.

The transconductance at fixed external bias voltage $(\partial I/\partial V_{\text{g}})_{V_{\text{bias}}}$ is extracted by taking the numerical derivative of the averaged current $\langle I \rangle$, while the lever-arm α is

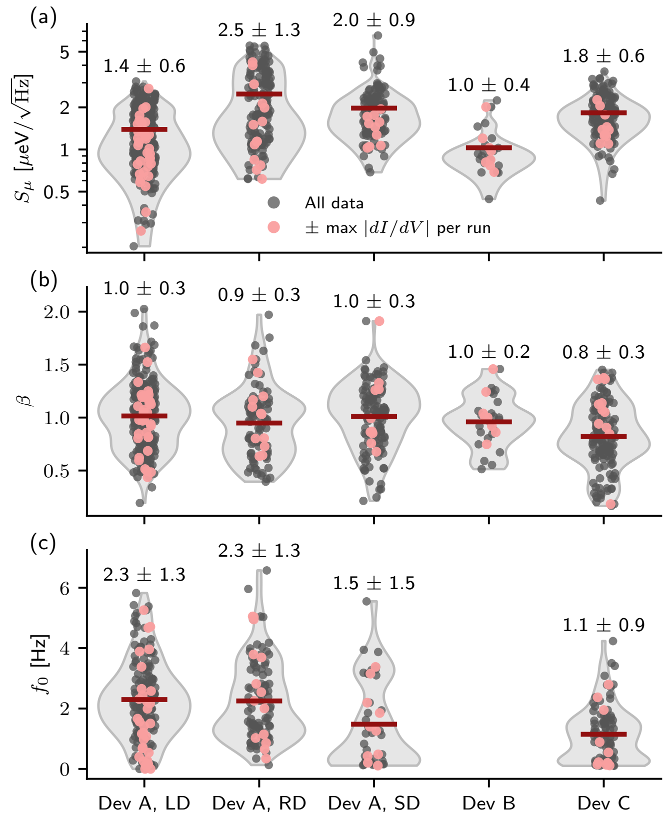

FIG. 3. Statistics of the noise metrics. The value on top of each of the violin plots corresponds to the average and standard deviation values for all data for that specific device and is marked by the bar. (a) Charge noise value evaluated at 1 Hz. (b) Extracted exponent β reported for those datapoints described by the model with the $1/f$ term. (c) Extracted frequency f_0 of the single TLF. No Lorentz contributions were observed for Device B.

obtained from the slopes of the corresponding Coulomb diamond. The lever arms vary between $0.07 - 0.11$ eV/V for Devices A and B. The PSD of the electrochemical potential fluctuations is calculated as (see SI, Sec. 4 for the derivation):

$$S_{\mu\mu}(f) = \alpha^2\, S_{VV}(f) = \alpha^2 \left(\frac{\partial I}{\partial V_{\text{g}}}\right)^{-2}_{V_{\text{bias}}} S_{II}(f). \tag{4}$$

In Fig. 2d we plot the values of noise S_μ at 1 Hz, where $S_\mu = \sqrt{S_{\mu\mu}}$, which are calculated from the fitted models throughout the Coulomb peak for selected gate voltages $[V_{\text{g}}]$. We highlight the PSD-model by color coding: $1/f$ – blue, Lorentz – red and Sum – green. Theoretically, the extracted noise amplitude $S_\mu(1\,\text{Hz})$ should be independent of V_{g} (see toy-model simulations in the SI, Sec. 5). Instead, we observe a clear non-uniform distribution across the Coulomb peak. The noise differs between the two flanks of the Coulomb peak, both in magnitude and in its spectral character: on the left it is consistent with an ensemble of TLFs, whereas on the right it is dominated by a single prominent TLF. One possible explana-

TABLE I. Selection of reported charge-noise amplitudes S_μ (in $\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$) at 1 Hz across various material platforms with different spacer thicknesses d (nm) measured via the flank method. If a reference reports different numbers upon improving the fabrication flow, we take the best result of that work.

Reference	Material	d	S_μ
Kim et al.[42]	Si/SiO_2	-	3.4
Petit et al.[43]	$^{28}Si/SiO_2$	-	2
Chanrion et al.[39]	Si/SiO_2	-	1
Elsayed et al.[35]	Si/SiO_2	-	0.61
Freeman et al.[44]	Si/SiO_2	-	0.49
Spence et al.[38]	CMOS NW	-	1.73
Jekat et al.[45]	InSb NW	-	1
Freeman et al.[44]	Si/SiGe	40	2
Connors et al.[34]	Si/SiGe	50	0.84
Holman et al.[33]	^{28}Si/SiGe	42	0.77
Struck et al.[46]	^{28}Si/SiGe	45	0.47
Mi et al.[47]	Si/SiGe	50	0.33
Paquelet et al.[48]	^{28}Si/SiGe	30	0.29
This work	Ge/SiGe	4	1.8
	Ge/SiGe	20	1.8
Hendrickx et al.[13]	Ge/SiGe	22	1.4
Lodari et al.[20]	Ge/SiGe	55	0.6
Stehouwer et al.[36]	Ge/SiGe	55	0.3

tion is that changing V_g and V_SD rearranges local screening charges and trap occupancies, thereby modifying the coupling to individual fluctuators. This non-uniformity of S_μ is not unique to our data: it was observed in Refs.38 and 39 and studied rigorously in Ref.41.

Following the protocol described above, we collected datasets for devices A, B, and C. For Device A, the noise on the Sensor QD is measured when the DQD gates are energized; on the Left (Right) QD when the Sensor QD gates are energized and those of the Right (Left) are at ground potential. All the analyzed datasets can be found in the SI, Sec. 6. We report the electrochemical potential noise density S_μ at 1 Hz (Fig. 3a), β for the PSD traces exhibiting $1/f$-trend (Fig. 3b), and f_0 for the Lorentzians (Fig. 3c). Given that most of the charge noise studies[20,35,36] use the noise evaluated at points with maximal transconductance, we highlight these operating points by pink color. The most important feature of Fig. 3a is the fact that both devices A and B exhibit noise statistics comparable to that of Device C (the sensor dot in Ref.25). The latter has demonstrated a microwave driven qubit with dephasing times up to $T_2^* = 3\,\mu\mathrm{s}$. We interpret this comparison as a promising result for the ultra-shallow heterostructures. Additionally, the exponents β are distributed around the average value of 1, which is predicted by theoretical modeling[32]. The switching frequencies f_0 are distributed in the low Hz range; we did not observe any Lorentz behavior for Device B.

To conclude, we relate the average noise level observed for Devices A and B to those reported in the literature (see Table I). We find it comparable to most of the shallow cap wafers and CMOS structures. We note, however, that it is almost six times worse than the best Ge/SiGe heterostructure with the thick 55 nm cap. Although the latter is undoubtedly preferred for quantum computing applications, ultra-shallow cap wafers offer certain advantages for prototyping hybrid devices. In principle, any material can be deposited or placed in proximity to the Ge layer upon removal of the native SiO_2 layer. This concerns not only the superconducting materials but also ferromagnetic (*e.g.* EuS) or two-dimensional materials with enhanced spin-orbit interaction such as WSe_2. Finally, a tunable proximitized QD was very recently formed on such an ultra-shallow Ge/SiGe heterostructure, demonstrating its potential for future hybrid spin-superconductor experiments[49].

SUPPLEMENTARY MATERIAL

See the supplementary material for fabrication details, additional stability diagrams, details of the noise-estimation procedure, measured levels of the transimpedance-amplifier noise and analysis of the effect of its input resistance, noise simulations, and a summary of all analyzed data sets.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author contributions

Maksim Borovkov: Conceptualization (equal); Formal analysis (lead); Investigation (equal); Methodology (lead); Resources (equal); Validation (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Yona Schell**: Investigation (equal); Writing – original draft (supporting). **Dina Sokolova**: Resources (equal). **Kevin Roux**: Investigation (supporting); Resources (supporting). **Paul Falthansl-Scheinecker**: Investigation (supporting); Resources (equal). **Giorgio Fabris**: Resources (equal). **Devashish Shah**: Investigation (supporting). **Jaime Saez-Mollejo**: Investigation (supporting). **Rodolfo Previdi**: Resources (supporting). **Inas Taha**: Investigation (supporting). **Aziz Genç**: Investigation (supporting). **Jordi Arbiol**: Investigation (supporting). **Stefano Calcaterra**: Resources (equal). **Afonso De Cerdeira Oliveira**: Resources (equal). **Daniel Chrastina**: Resources (equal). **Giovanni Isella**: Resources (equal). **Anton Bubis**: Investigation (supporting); Supervision (supporting); Resources (equal); Writing – review & editing (equal). **Georgios Katsaros**: Conceptualization (equal); Supervision (lead); Funding acquisition (lead); Validation (equal); Project administration (lead); Writing – original draft (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are openly available at the Institute of Science and Technology repository under DOI 10.15479/AT-ISTA-22242[50].

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