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Hybrid Resonant Switched-Capacitor Converter for 48V to 3.4V Direct Conversion

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***Abstract*—As the power required by modern data center processors increases, the power architecture must be adapted; for example, 48 V distribution voltage allows to reduce copper losses by a factor 16 with respect to the use of traditional 12 V power architecture. In order to generate the required processor core voltage, a two-stage approach is usually preferred, where the intermediate bus voltage is generated using an unregulated resonant DC-DC converter as, for instance, an LLC converter. Compared to LLCs, hybrid resonant switched-capacitor converters (ReSCCs) make it possible to achieve large voltage conversion ratios without the need of high turns ratio transformers. In this paper, a novel hybrid ReSCC that performs a 48V-to-3.4V direct conversion is presented. A prototype of the proposed converter has been implemented, capable of providing a continuous output power of 440 W with a maximum efficiency of 96.3% at 30 A load current.**

***Index Terms*—intermediate bus converters, hybrid switched-capacitor converter, multi-tapped autotransformer, soft switching**

I. Introduction

The 54/48 V conversion towards the regulated ASIC/CPU/GPU V_{core} voltage is usually achieved through different conversion steps that involve one or more unregulated intermediate bus converters (IBC) used to step-down the input voltage, followed by a regulated voltage regulation module (VRM) placed close to the digital load. The first stage(s) are usually characterized by high efficiency, while the VRM must finely regulate its output voltage with large bandwidth to deal with the fast load transients. For power architectures legacy, an intermediate voltage of 12 V is usually selected. However, in the long term lower intermediate bus voltage can be a promising solution to increase the VRM switching frequency in order to reduce the total power delivery network (PDN) impedance without losing efficiency. For example, a 6V intermediate voltage was selected in [1] to minimize the total losses for the conversion from 48V down to processor voltage V_{core}. As a result, there is a growing interest in fixed-ratio conversions with ratios of 8-to-1 and higher. Soft-switching resonant topologies are usually selected for IBC because of their high efficiency and power density. ReSCC such as [2], [3] and [4] have demonstrated optimal performance for 48V-to-12V conversion, while high-performance ReSCC providing greater conversion ratios have yet to be extensively investigated. This is due to the fact that the number of components (switches and capacitors) increases directly with the conversion ratio, and the growing circuit complexity might possibly undermine the theoretical performance improvement while raising cost and reliability issues as well. To overcome these issues, [5] aims to lower the circuit complexity of ReSC converters with high conversion ratios by adding more working phases in each switching cycle. A traditional LLC converter might seem a better solution, since a large conversion ratio can be achieved by increasing the turns ratio of a transformer, as reported [6]. Unfortunately, the implementation of a high turns ratio transformer is not trivial [7], and it requires a large number of layers to reduce copper losses on the secondary side. A better use of the transformer is presented in [8], where an hybrid ReSCC topology is implemented to perform a 48V-to-6V conversion. In this solution the conversion ratio is no more uniquely related to the transformer turns ratio, but it also results from a SCC structure. For this reason it is possible to mitigate the copper losses on the transformer even at relatively high conversion ratios.

In this paper we introduce a novel hybrid ReSCC topology based on ladder structure that enhance the intrinsic 4-to-1 conversion ratio of the ReSCC with the use of a 4-winding single turn transformer. A direct conversion down to 3.4 V is therefore obtained. The paper is organized as follows: in the next section a detailed description of the converter operation is given; in section III some consideration on components mismatch is discussed, while in section IV the implementation details and the experimental results are reported. Conclusions are drawn in the last section.

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II. Interleaved Hybrid Topology

The proposed converter comprises an interleaved flying capacitor structure connected to a multi-tapped autotransformer (MTA) as shown in Fig. 1. Soft-switching operation is ensured by the inductive energy stored in the magnetizing inductance of the MTA, while soft-charging of the capacitors is guaranteed by both leakage inductances of the MTA and by two additional inductive elements. Considering the converter reported in Fig. 1, and following the converter waveforms of Fig. 2a, the operation pattern in one switching cycle T_{sw} can be described by four sub-intervals as follows:

1) t_0-t_1*:* at $t = t_0$, switches Q_1, Q_4, Q_6, Q_7, and Q_{10} are turned on, and the energy stored in the magnetizing inductance

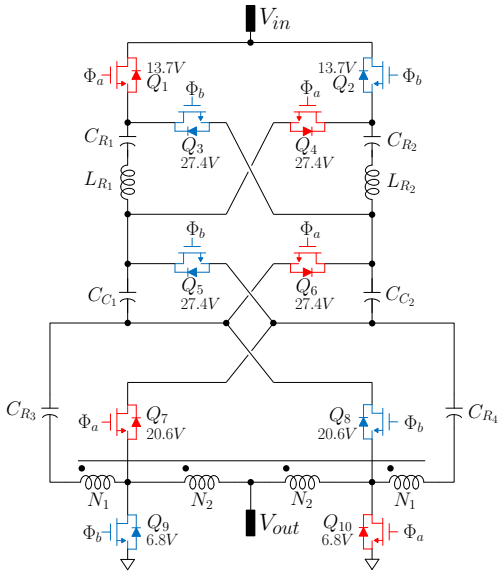

Fig. 1. Schematic of the proposed hybrid switched capacitor converter with transistors ratings reported for $V_{IN} = 48\ V$.

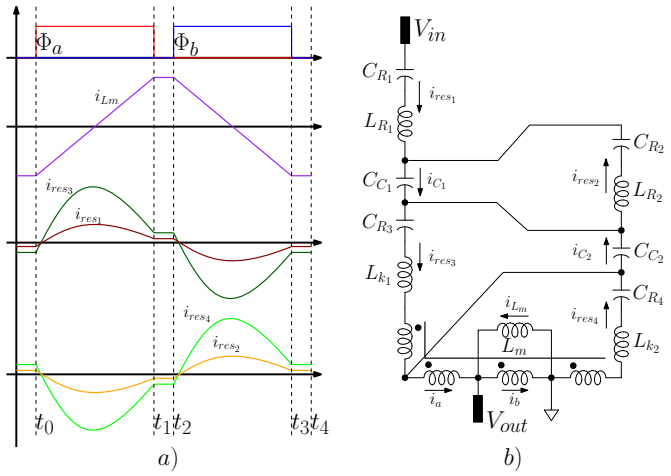

Fig. 2. a) Main current waveforms of the converter during one switching cycle and b) simplified circuit configuration during Φ_a.

of the MTA allows zero-voltage switching (ZVS) for all devices. The converter phase between t_0 and t_1 is reported in Fig. 2b, where the leakage inductances L_k responsible for the resonance, and the magnetizing inductance L_m of the MTA, are reported. Resonance is obtained with 4 tanks: C_{R_1}-L_{R_1}, C_{R_2}-L_{R_2}, C_{R_3}-L_{k_1} and C_{R_4}-L_{k_2}, which must be tuned on the same resonant frequency f_{SW}.

$$f_{SW} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

The clamp capacitances C_{C_1} and C_{C_2}, beyond participating at the voltage conversion, behaves as low impedances for the CL tanks, separating their resonant modes.

Due to resonance of the 4 tanks in the circuit, capacitances C_{R_1} and C_{R_3} are soft-charged from $i_{res_1}(t)$ and $i_{res_3}(t)$ respectively, while, considering the symmetry of the circuit and the charge balance on the capacitors, C_{R_2} and C_{R_4} are soft-discharged by opposite currents. From KCL it is possible to state that the current $i_{C_1}(t)$ corresponds to the sum of $i_{res_1}(t)$ and $i_{res_2}(t)$, which means that also C_{C_1} is soft-charged. On the other side, $i_{C_2}(t)$ can be written as $i_{res_2}(t)+i_{res_3}(t)-i_{C_1}(t)$, and so all the capacitors are charged and discharged by sinusoidal currents.

Concerning the C_{R_3}-L_{k_1} and C_{R_4}-L_{k_2} resonators, it is possible to derive the two currents as in (2), keeping in mind that, thanks to the symmetry of the circuit, the current that charges C_{R_3} is equal to the current that discharges C_{R_4}, and that resonance of the two currents is guaranteed by the leakage inductance of the MTA.

$$\begin{cases} i_{res_3}(t) = i_{res_1}(t) + i_{C_2}(t) = 3i_{res_1}(t) \\ i_{res_4}(t) = i_{res_3}(t) = 3i_{res_1}(t) \end{cases} \tag{2}$$

Given an autotransformer with N_1 turns on primary sides and N_2 turns on secondary sides, (3) is satisfied

$$N_1\left(i_{res_3}(t) + i_{res_4}(t)\right) + N_2\left(i_a(t) + i_b(t)\right) = 0 \tag{3}$$

then it is possible to derive the currents $i_a(t)$ and $i_b(t)$ as follows:

$$\begin{cases} i_a(t) = i_{res_3}(t) + i_{res_4}(t) - i_{C_2}(t) = 4i_{res_1}(t) \\ i_b(t) = -\left(6\frac{N_1}{N_2} + 4\right) i_{res_1}(t) \end{cases} \tag{4}$$

Once those currents have been derived, and noticing that the $i_{res_1}(t)$ corresponds to the input current in this phase, the output current can be written as follows:

$$i_{OUT}(t) = i_a(t) - i_b(t) = \left(6\frac{N_1}{N_2} + 8\right) i_{IN}(t) \tag{5}$$

2) $t_1 - t_2$: at $t = t_1$, switches Q_1, Q_4, Q_6, Q_7 and Q_{10} are turned off. In this time interval all the switches are off and the *dead time* can be defined as $t_{dead} = t_1 - t_2$. The output capacitances of Q_2, Q_3, Q_5, Q_8 and Q_9 are discharged by the current on the magnetizing inductance of the MTA, meanwhile, the remaining transistors output capacitors are charged up to their off state DC value. If the t_{dead} is long enough, ZVS can be ensured for all the switches. The value of the magnetizing current i_{L_m} in t_1 corresponds to its absolute peak value, which is defined as

$$i_{L_m} = \frac{V_{OUT}}{4L_m f_{sw}} \tag{6}$$

The i_{L_m} current distribution in the circuit is strictly related to the topology and output capacitors values, moreover, the different DC voltage values on the various transistors leads to a different condition for ZVS for every switch. In general, considering that a transistors Q_i output capacitance $C_{OSS,i}$ is charged/discharged by a portion k_i of the current i_{L_m}, and that its off state DC voltage value is equal to $V_{DS,i}$, then ZVS is ensured only if the following relation is satisfied:

$$t_{dead} \geq \frac{V_{DS,i}C_{oss,i}}{k_i i_{L_m}} = \frac{4L_m f_{sw} V_{DS,i} C_{oss,i}}{kV_{OUT}} \tag{7}$$

Hence, the sizing of L_m and t_{dead} are strictly related, and their values can be chosen with the aid of a simulator, however, as it will be explained in next section, this is not the only constraint in the selection of t_{dead}. As can be noted in (7) the ZVS condition is independent from the load current.

3) $t_2 - t_3$: at $t = t_2$, switches Q_2, Q_3, Q_5, Q_8 and Q_9 are turned on in ZVS. After $t = t_2$, the resonant transition takes place between C_{R_1} and L_{R_1} and between C_{R_2} and L_{R_2}, while the remaining resonant mode transition takes place between C_{R_3} and the leakage inductance L_{k_1}, and between C_{R_4} and the leakage inductance L_{k_2}. Due to the circuit symmetry, the behavior of the converter can be described the same way as for the time interval $t_0 - t_1$ referring to the Fig. 2b. In this case, the output current can be written as a function of i_{res_2} current, which absolute value corresponds to the input current.

$$i_{OUT}(t) = i_a(t) - i_b(t) = \left(6\frac{N_1}{N_2} + 8\right) i_{IN}(t) \qquad (8)$$

4) $t_3 - t_4$: at $t = t_3$, switches Q_2, Q_3, Q_5, Q_8 and Q_9 are turned off. The resonant mode of the 4 tanks are in zero-current, and so also the output current is zero. The only current flowing in the circuit is the magnetizing current i_{L_m} of the MTA. As for the period $t_1 - t_2$, the output capacitances of Q_1, Q_4, Q_6, Q_7 and Q_{10} are discharged, and, if (7) is satisfied, ZVS is guaranteed for the next phase transition. Considering (5) and (8), and observing that during the two *dead times* both the input and the output currents are zero, the conversion ratio can be derived:

$$\frac{V_{in}}{V_{out}} = 6\frac{N_1}{N_2} + 8 \qquad (9)$$

By using a 4-winding single turn transformer ($N_1 = N_2$) the 14-to-1 conversion ratio can be obtained. The same result can be obtained from the DC capacitor voltage derived from the circuit of Fig. 2 b: the DC value of $V_{C_{R_{3,4}}}$ is $3V_{out}$ and, consequently, $V_{C_{C_{1,2}}}$ and $V_{C_{R_{1,2}}}$ is $4V_{out}$. Considering these voltage levels on Fig. 2 b, V_{in} is equal to $2V_{out} + 2V_{C_{C_{1,2}}} + V_{C_{R_{1,2}}}$, hence $14V_{out}$.

III. Components Mismatch

Mismatch analysis is mandatory for multi-tank resonant converters, in fact, as long as the resonant frequency of the different tanks that made up the converter are all aligned to f_{SW}, all the currents flowing in the circuit are sinusoidal, and during switching from phase Φ_a to phase Φ_b, zero-current switching (ZCS) is obtained. However, if a mismatch between the various resonant tanks is present (for example one tank has a resonant frequency different from f_{SW}), then the multi-mode operation give rise to a mismatch in the currents flowing in the devices. In Fig. 3a the C_{R_1}-L_{R_1} tank current is reported in the case of perfect matching with switching frequency and when a mismatch (positive and negative) is present. As can be noticed, when a mismatch is present, not only the RMS current value increases, increasing conduction losses, but also ZCS is lost. Of course, additional power losses does not only limit the efficiency, but they also reduce the maximum power that the converter can deliver to the load. The optimal solution to manage this problem would be to individually control the ON times of all the switches with a zero-current detection controller, in such a way to block tank current when it crosses zero, and to regulate the switching frequency according to the slower resonator. However, since in the proposed structure the resonant tank currents sums up in different nodes of the circuit, it is not possible to individually control all the resonators.

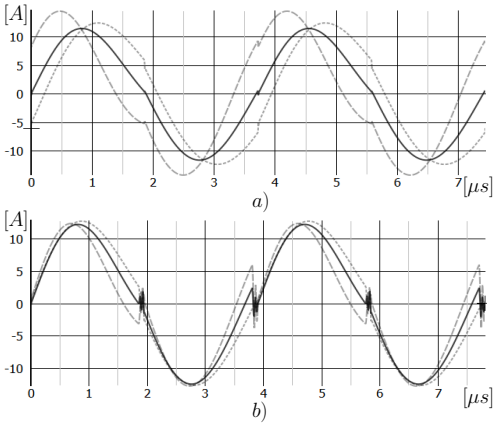

Fig. 3. Resonant tank current simulated for a) t_{dead}=10ns and b) t_{dead}=100ns, when the resonance frequency is equal to the switching frequency (solid line), higher than the switching frequency (dashed line) or lower than the switching frequency (dotted line).

Therefore, it would be better to rely on dead times to manage mismatches. During dead times all the switches are turned off. Considering components mismatches every resonant tank is characterized by a non-zero current that is forced in the circuit by the corresponding inductance. Those residual currents are able to flow in the body diodes of the power mosfets, activating discharging paths that reset the inductors currents with a rate

$$\Delta I = \frac{V^*}{L_R} t_{dead} \qquad (10)$$

where V^* is the voltage on the inductance imposed by the discharging path. As can be noticed, while V^* is dependent on V_{IN} and on the topology, L_R is the only parameter that can be adjusted during sizing, in particular, it must be low enough to guarantee a t_{dead} negligible with respect to T_{SW}. If both parameters are correctly sized, at the beginning of the next ON phase the current in every tank will be zero, reducing RMS currents and restoring ZCS during turn on transitions.

In Fig. 3b the current waveforms with the same mismatch conditions of Fig. 3a are reported, but a dead time of 100 ns has been introduced. As can be seen, now the RMS current is lower with respect to the previous case when components mismatches are introduced, and ZCS is ensured at the beginning of both operation phases. The components mismatch considerations made for the C_{R_1}-L_{R_1} tank are valid for all four resonators present in the circuit. Mismatch simulations where components tolerances have been taken into account proves the quality of the proposed compensation method, with a maximum efficiency degradation at full load of 0.6%.

IV. Prototype Implementation and Results

In order to validate the proposed converter, a prototype has been implemented for 48V-to-3.4V voltage conversion. The converter picture is shown in Fig. 4, while the main design parameters and the selected active and passive components are reported in table I. A 12 layers PCB stack with internal 3oz layers has been selected in order to be able to manage the high output current. However, as can be seen in Fig. 5, the number of layers have been enhanced to 24 under the

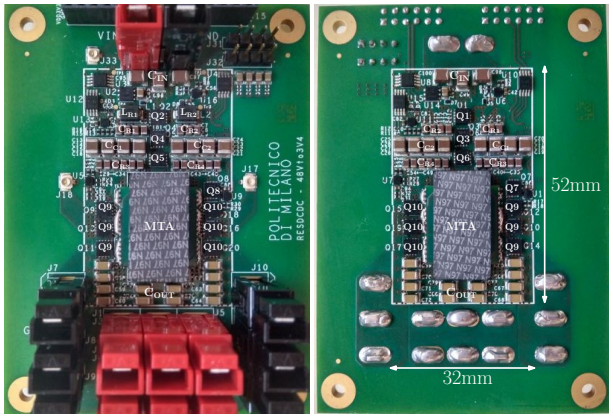

Fig. 4. Prototype top and bottom views with area dimensions.

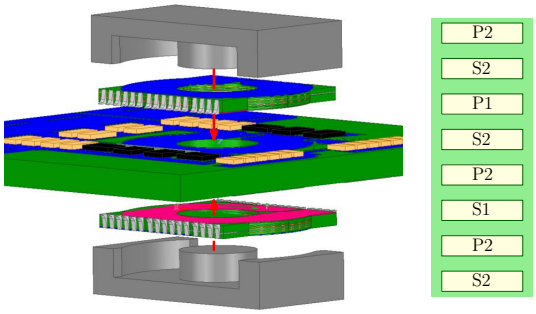

Fig. 5. Assembly view of the 4 windings PCB integrated multi-tapped autotransformer, with corresponding windings distribution used to minimize MMF (the reported stack is repeated 3 times across the total 24 layers stack). With reference to the MTA symbol used in Fig. 1, the windings, from left to right, corresponds to P1, P2, S2 and S1.

MTA ferromagnetic core by adding two PCB modules of 6 layers each, in order to further reduce the transformer losses. The windings interleaving as reported in Fig. 5 was exploited to minimize the total magnetomotive-force (MMF) while providing an optimal current distribution to the four windings, minimizing therefore the corresponding losses. This solution made it possible to use of a commercial ferromagnetic core rather than a custom matrix one, even for such a high output current design. The two ER ferromagnetic elements have been assembled with a sufficiently large gap to obtain

TABLE I
PARAMETERS AND COMPONENTS

V_{IN}	36V-60V, 48V nominal
V_{OUT}	2.5V-4.3V, 3.4V nominal
I_{OUT}	140A
$Q_1 - Q_8$	BSZ021N04LS6 (40V, 2.1mOhm, Infineon)
$Q_9 - Q_{10}$	6 x IQE006NE2LM5CG (25V, 0.6mOhm, Infineon)
Gate Drivers	LM5113
$L_{R1} - L_{R2}$	25nH (+/-15%, WE)
MTA core	2 x ER23/5/13 (N97, TDK)
$C_{R1} - C_{R2}$	32.9uF (4.7uF, 35V, X8L, 7pcs, Murata)
$C_{R3} - C_{R4}$	56.4uF (4.7uF, 35V, X8L, 12pcs, Murata)
$C_{C1} - C_{C2}$	176uF (22uF, 25V, X7S, 8pcs, Murata)
C_{IN}	60uF (10uF, 75V, X7R, 6pcs, TDK)
C_{OUT}	2.4mF (100uF, 6.3V, X6T, 24pcs, Murata)
f_{SW}/t_{DEAD}	280kHz/100ns

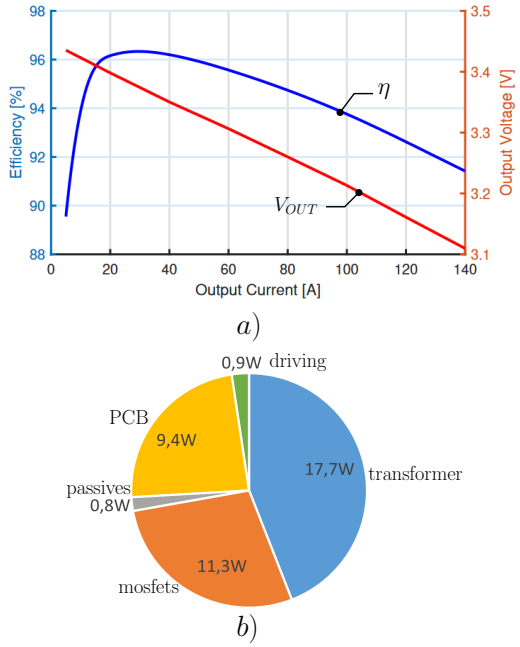

Fig. 6. a) Measured converter efficiency (blue curve) and output voltage (red curve). b) Loss distribution at 140A current load.

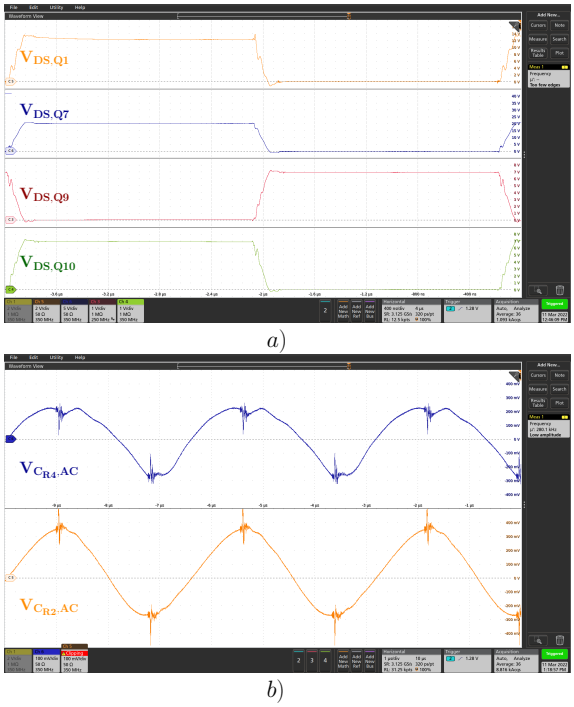

Fig. 7. a) Measured V_{DS} voltages shows ZVS through the turning on of the body diodes during both turn-on and turn-off transients, while b) resonant operation of C_{R4} and C_{R2} tanks is shown as AC coupled capacitor voltages.

a magnetizing inductance that ensure ZVS on all switches in 100 ns dead time. The total converter area is 52mm x 32mm, while the height, limited by the two ER ferromagnetic elements, is 10.4mm.

The implemented converter has been tested up to a total output power of 440 W with forced air cooling. In Fig. 6a the obtained converter efficiency and output voltage as function

of the load current are reported. A peak efficiency of 96.3% at 30 A load current has been measured, whereas at no load conditions the measured output voltage corresponds exactly to 3.428 V, validating the designed conversion ratio. Fig. 6b shows the loss breakdown analysis at 140A current load, it is possible to notice that the design of the transformer and PCB is critical, and a further optimization can lead to an efficiency improvement. In Fig. 7a, the V_{DS} voltages of main transistors are reported in order to check soft switching operation. ZVS is ensured by body diodes turn on during both turn on and turn off transients, while ZCS causes a small oscillation during those transients. In Fig. 7b, the capacitors voltages highlights the resonance operation.

V. Conclusions

In this paper, a new resonant switched-capacitor converter topology for 48V bus conversion has been introduced. An extremely high conversion ratio of 14-to-1 is obtained relying both on an interleaved switched-capacitor network, and on a 4-winding transformer, which also ensures ZVS on all the switches. The need of a single turn primary winding for the transformer made it possible to devote most of the PCB layers to the output winding that carries the high output current. Therefore, the need of a high turns ratio transformer that would come with conventional LLC topologies is overcome, allowing to improve the converter power density. The implemented prototype converter reaches a peak efficiency of 96.3% at 30 A, while it can provide up to 140 A to the load. A power density of 415 W/inch^3 is obtained using a 12 layers PCB stack.

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