Progress in Additive Manufacturing
https://doi.org/10.1007/s40964-026-01528-8

RESEARCH

Wafer-scale PBF-LB/M additive manufacturing of $SnAg_3$ as thermal interface materials for advanced high-power electronics cooling

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Received: 3 July 2025 / Accepted: 7 January 2026
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Abstract
To support the miniaturization of electronics with increasing power, advanced cooling strategies are needed. Unlike conventional cooling pathways for wafer-scale electronics that involve the use of thermal pastes, we introduce an additive manufacturing route using laser powder bed fusion (PBF-LB/M) to fabricate 50–200 µm thick $SnAg_3$ deposits that function as thermal interfaces between the Si substrate and the heat exchanger. The results reveal that by fine tuning the PBF-LB/M process parameters, it is possible to engineer the microstructure of the printed thermal interface materials onto Si wafer and to limit the Si damage. These findings demonstrate a promising solution for wafer-scale additive manufacturing of advanced cooling architectures, enabling the fabrication of high-power electronics.

Keywords Wafer-scale electronics · Additive manufacturing on silicon · Laser powder bed fusion (PBF-LB/M) · Solder-based thermal interface materials · Direct metal printing for electronics cooling.

1 Introduction

In recent years, the advancements in integrated circuits industry resulted in smaller and more powerful electronic devices. This increase in power generates more heat, while the reduction in size limits the surface area available for traditional cooling methods. According to Moore's law [1], integrated circuit components halve in size and double in power roughly every 18 months. Power density in devices like power converters is expected to rise to 500 W/cm^2, with localized hotspots on chips reaching heat fluxes over 1000 W/cm^2, which negatively impacts the performance of the microprocessors [2–6]. Standard cooling solutions, including microchannel heat sinks, vapor chambers and heat pipes are often insufficient, particularly for high-power electronic in space applications, where high heat fluxes must be dissipated with low thermal resistance [7, 8].

Conventional cooling systems use a layered design with a heat sink and thermal interface materials (TIM), as shown in Fig. 1A. The TIM is often applied to connect physically and thermally the device and the heat sink, filling microscale gaps between their surfaces. However, both the contacting interface and the TIM significantly influence heat transfer efficacy and are characterized by parameters like thermal interface resistance (TIR) and thermal conducting resistance (TCR) [9, 10]. TIR refers specifically to the resistance to heat flow at the physical boundary between the TIM and the solid surfaces it connects, which arises from imperfect contact at the microscopic level due to surface roughness or voids. TCR instead refer more broadly to the total resistance to heat transfer across the entire interface, including the intrinsic resistance of the TIM itself and the quality of its adhesion to adjacent surfaces. High TIR or TCR values can significantly limit the efficiency of heat dissipation, meaning that even a TIM with good bulk thermal conductivity

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Published online: 12 February 2026

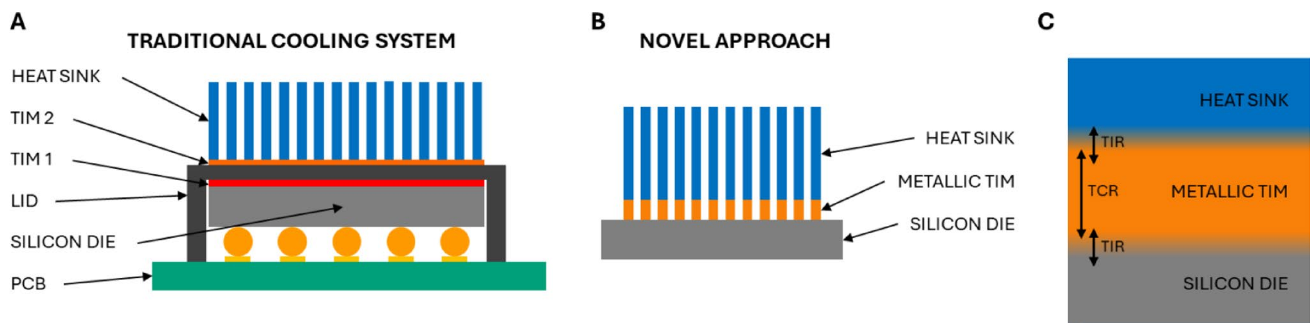

Fig. 1 **A** Schematics of conventional packaging in electronic microprocessors, modified from Azizi et al. [11], **B** novel cooling system and **C** geometry of TIM between the electronic device and the heat sink, showing the TIR and TCR resistance components, modified from Cao et al. [9]

may underperform if the interface resistance is not properly minimized.

Selecting a TIM requires careful consideration of several key factors to ensure optimal performance, reliability and ease of application. Thermal conductivity, bond line thickness and contact thermal resistance are major factors affecting the performance of TIMs [10]. A high bulk thermal conductivity of the TIM is a primary consideration, as it directly impacts heat transfer efficiency and helps maintain device temperatures within safe limits, avoiding overheating. Moreover, the TIM's TCR, which depends on both the material's properties and the quality of its contact with adjacent surfaces, should be minimized to obtain a performant connection between the die and the heat sink [10, 12].

Over the past two decades, various types of TIMs have been developed, including thermal pastes, phase change materials, ceramic reinforced polymer composites, 3D ceramic filler networking composites, flexible thin films and resilient thermal conductors [9, 10]. Ceramic reinforcements like Al_2O_3, SiC, AlN, and BN are often employed because they offer high thermal conductivity while remaining electrically insulating, which is particularly advantageous in electronic applications where electrical isolation must be maintained alongside efficient heat dissipation [13]. Thermal pastes are the most common type of TIMs, which typically comprise thermally conductive particles, such as like silver, aluminium oxide (Al_2O_3) and zinc oxides (ZnO), boron nitride (BN) and aluminium nitride (AlN), dispersed in a polymeric viscous medium [14, 15], . By filling air gaps, they ensure good contact between components and heat sinks, however, they present a limited thermal conductivity ranging from 1 to 10 W/m·K [10, 16–20].

Azizi and coworkers [11, 21] introduced a novel solution that leverages Powder Bed Fusion – Laser Beam/Metal (PBF-LB/M) to directly print a metal TIM and the heat exchanger onto the active Si die, thus eliminating the need of low-conductivity thermal pastes. PBF-LB/M is an additive manufacturing (AM) process that uses a high-powered laser to selectively melt metal powder layer by layer, enabling the production of complex-shape components. This approach is revolutionary because it eliminates the TIM2, which is typically located between the lid and the heat sink. By directly integrating the heat exchanger onto the die, it removes a major thermal bottleneck in conventional packaging architectures, significantly reducing interfacial thermal resistance and improving overall heat dissipation efficiency.

This research proposes an PBF-LB/M-deposited tin-based solder alloy (i.e., $SnAg_3$ alloy) as an interlayer for directly bonding metallic heat sinks onto silicon substrates. The $SnAg_3$ (~ 3 wt% Ag) alloy was chosen among tin-based solder alloys due to its favourable thermal conductivity. The thermal conductivity of the similar $SnAg_{3.5}$ alloy was determined to be 74 W/m·K at 30 °C by Kehoe et al. [22]. This value significantly surpasses that of the traditional SnPb37 alloy, which exhibited a thermal conductivity of 55 W/m·K at 30 °C. Moreover, Sn-based alloy's low melting point (~ 250 °C) mitigates thermal stresses during solidification and cooling.

Utilizing alloys with lower melting points reduces heat exposure to the substrate and adjacent components during processing. This is particularly advantageous for heat-sensitive components such as those used in electronic circuits. Furthermore, melting at lower temperatures helps mitigate the risk of thermal expansion mismatches between the TIM and the Si substrate [23–25]. This is particularly important as excessive thermal expansion differences can lead to mechanical stress and potential damage, such as crack formation and propagation at the joint and the surrounding materials [26, 27].

The Si-$SnAg_3$ interface was investigated in this work to evaluate the impact of PBF-LB/M processing parameters on interfacial bonding and substrate integrity. The results showed that higher volumetric energy density (VED) led to deeper laser penetration and partial melting of the silicon substrate. This promoted the diffusion of silicon into the Sn alloy and the formation of columnar, silicon-rich structures protruding into the metallic deposit. However, excessive

energy input also induced thermal stress-related cracking in the brittle silicon. Reducing the energy density mitigated substrate damage while still ensuring good metallurgical bonding and adequate melt pool penetration compatible with electronic dies.

The main contributions of this work can be summarized as follow: (i) Wafer-scale PBF-LB/M fabrication of a $SnAg_3$ TIM on silicon; (ii) Establishment of a PBF-LB/M processing window for crack-free deposition; (iii) Comprehensive microstructural characterization of the deposits and the Si–$SnAg_3$ interface; (iv) Measurement of thermal conductivity of printed $SnAg_3$ alloy; (v) Quantitative evaluation of laser-induced damage to the Si substrate caused by melt pool penetration.

2 Materials and methods

The $SnAg_3$ (2.9 wt% Ag, 0.02 wt% Pb) air-atomized powder with size < 80 µm was supplied by IMR metal powder technologies GmbH. A 3-inch diameter and 0.5 mm thickness <100> monocrystalline undoped silicon wafer was used as the substrate for the PBF-LB/M prints.

The selected powder was first analysed using a Field Emission Scanning Electron Microscope (FE-SEM) model Zeiss Sigma 500 equipped with energy dispersive X-ray spectroscopy (EDS) and secondary electrons and backscattered electrons detectors (EBSD). The morphology of the PBF-LB/M deposits was also characterized by an FE-SEM microscope (Jeol JSM-7200 F) equipped with an EDS Detector (X-Max N 80mm^2 Detector—Oxford Instruments) and an EBSD detector (Nordlys Nano EBSD Detector—Oxford Instruments). The EDS measurements were performed at 15 kV and EBSD measurements were performed at 20 kV. The measurements results were analysed using the Aztec software (Oxford Instruments). Kernel Average Misorientation (KAM) maps were computed from the EBSD datasets using a misorientation threshold of 5°, meaning that only local misorientation angles above this cutoff were included in the calculation. The Sn-based TIM melt pool penetration depth into the Si substrate was measured directly on polished cross-sections by recording the maximum penetration distance observed at the interface. Quantification of silicon incorporation within the Sn matrix was obtained through EDS area analysis, performed over the entire cross-sectional region of the metallic layer.

X-ray diffraction (XRD) measurements were performed using Bruker D8 Discover and Rigaku SmartLab diffractometers employing Cu Kα radiation. The data were collected in the diffraction angle range $20° \leq 2\theta \leq 70°$, with a step size of 0.01° and a scan rate of 1°/min.

The samples were produced by PBF-LB/M using a pulsed-laser Renishaw AM250 equipped with Reduced Build Volume (RBV) system and operating in inert (Argon) environment. The silicon substrate was fixed on an aluminium plate using a high temperature resistant tape, as shown in Fig. 2A. Substrate pre-heating was not employed during fabrication. The job layout, reported in Fig. 2, consists of 9 linear tracks (i.e., lines A – I for the first print job and lines J – R for the second print job) 0.5 mm wide and 1 cm in length, and 9 square samples (i.e., Squares A – I for the first print job and J – R for the second print job) 5 mm wide. Two print jobs were performed with the same layout but with different printing parameters combinations. Laser power of 110 and 70 W were employed in the first and the second PBF-LB/M jobs, respectively. Laser exposure time (140 µs) and layer thickness (25 µm) were kept constants for all the samples in both jobs. Hatch and point distances, instead, were varied to investigate how different Volumetric Energy Density (VED) values could affect the material microstructure and the Sn alloy deposits bonding to the substrate. Different VED values for each sample are reported in Table 1. VED is calculated according to the following equation:

$$VED = \frac{Laser\ power * Time\ of\ exposure}{Hatch\ distance * Point\ distance * Layer\ thickness} \quad (1)$$

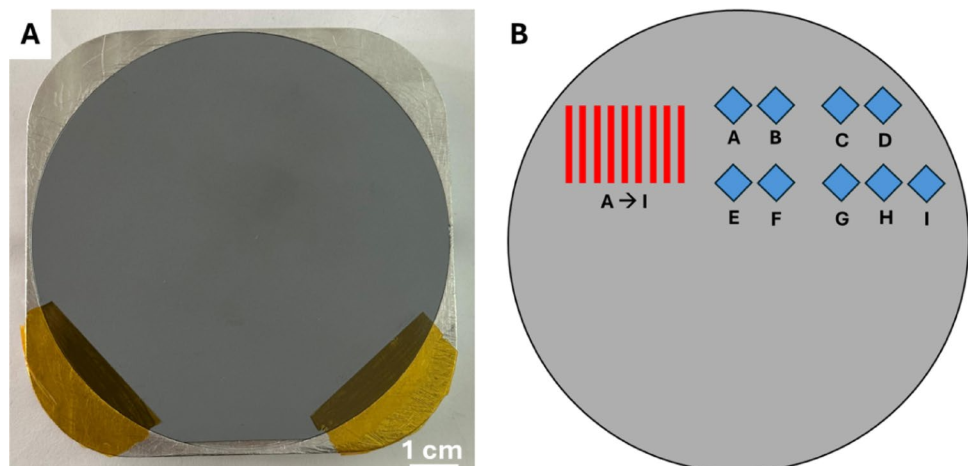

Fig. 2 Silicon substrate fixed on aluminium plate (**A**) and print layout of the PBF-LB/M jobs (**B**): linear track scans (red) and square samples (blue) on the silicon substrate (grey)

Table 1 Printing parameter combinations of the first (samples A – I) and second (samples J – R) PBF-LB/M jobs

VED (J/mm^3)		Hatch distance (mm)					
		0.09		0.11		0.13	
Point distance (mm)	0.06	A (failed)	114.1	B (failed)	93.3	C (failed)	79.0
		J	72.6	J	50.3	L	59.4
	0.08	D (failed)	85.6	E (failed)	70.0	F (failed)	59.2
		M	54.4	N	37.7	O	44.6
	0.1	G (failed)	68.4	H (failed)	56.0	I (failed)	47.4
		P	43.6	Q	30.2	R	35.6

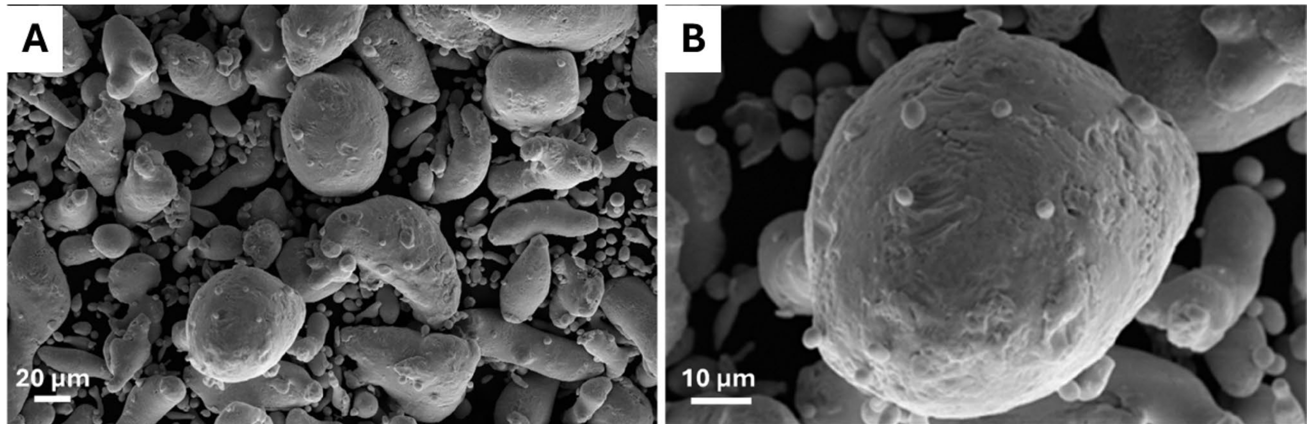

Fig. 3 FE-SEM images of the sieved (<80 μm) $SnAg_3$ powder feedstock

Microstructural analyses were carried out on the cross-sections of samples parallel to the building direction, employing Light Optical Microscope (LOM) and FE-SEM.

The thermal conductivity of the $SnAg_3$ alloy was determined using Laser Flash Analysis (LFA) and Transient Plane Source (TPS), following the ISO 22007-2:2008 standard. Two types of samples were analysed: square-based parallelepiped samples (6 × 6 × 4 mm) and cylindrical specimens (10 mm in diameter and 3 mm in height). All samples were fabricated using PBF-LB/M with the set of printing parameters referred to as “E” in Table 1. In particular, LFA technique was used to measure the thermal diffusivity (α), while TPS to evaluate the volumetric heat capacity (C). The through -plane thermal conductivity of the Sn alloy was calculated according to Eq. 2.

$$k = C * \alpha \tag{2}$$

3 Results and discussion

3.1 Analysis of powder particles

FE-SEM analyses were performed on the $SnAg_3$ feedstock powder to investigate its morphology. As shown in Fig. 3, the powder particles exhibit an elongated morphology with some particles characterized by a more spherical shape.

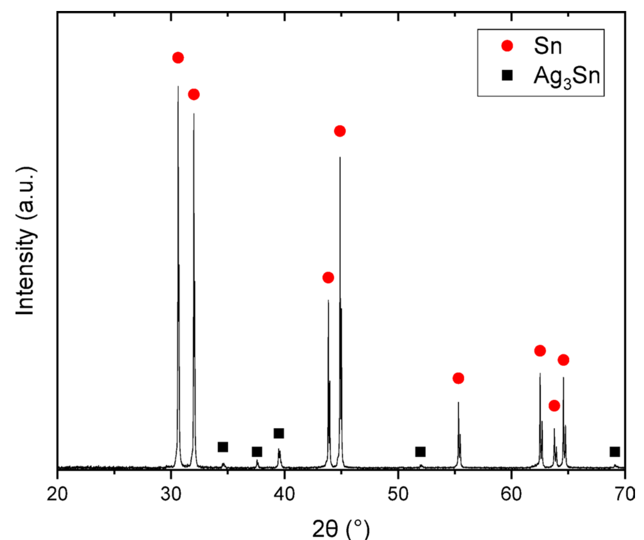

Fig. 4 XRD pattern of the $SnAg_3$ powder

The X-ray diffraction (XRD) analysis was conducted on $SnAg_3$ powder to identify its phase composition and crystal structure. The XRD pattern, reported in Fig. 4, reveals several prominent diffraction peaks that are mainly assigned to the crystalline Sn phase with tetragonal structure. The smaller peaks observed between 34° and 39°, at 52° and 69° match well with the characteristic reflections of the intermetallic compound Sn_3Ag.

3.2 Analysis of printed samples

Two printing jobs were conducted using different combinations of process parameters that are shown in Table 1. The VED was employed as a reference parameter to guide the selection of optimal printing conditions, aiming to avoid cracks in the Si substrate, to ensure complete material melting during fabrication, and to promote adhesion of the deposited material to the silicon substrate and minimal penetration of the melt pools.

The first job, performed with laser power of 110 W failed, with cracks propagating in the Si substrate. Reducing the laser power from 110 to 70 W—and consequently decreasing the energy density apported to the wafer—prevented substrate failure. A picture of the second print is shown in Fig. 5. At 110 W, the energy transferred from the laser to the material is significantly higher, resulting in rapid and intense localized heating. This leads to high thermal gradients between the molten zone and the substrate and to elevated thermal-induced stresses that exceed the strength of the wafer. By reducing the energy input, visible cracks were avoided, and the silicon wafer remained intact. Despite the failure of the first job, all samples were analysed. Table 2 reports cross-section LOM images of the linear track scans of the two PBF-LB/M jobs.

A comparison of the deposits indicated that those produced with a power of 70 W show higher contact angle with Si than those printed with a power of 110 W. Moreover, in first job samples it can be observed that, apart from sample F and I—i.e. the samples printed with lower VEDs—all deposits induced significant cracks below the tin-silicon interface, leading to abrupt failure of silicon wafer and, in

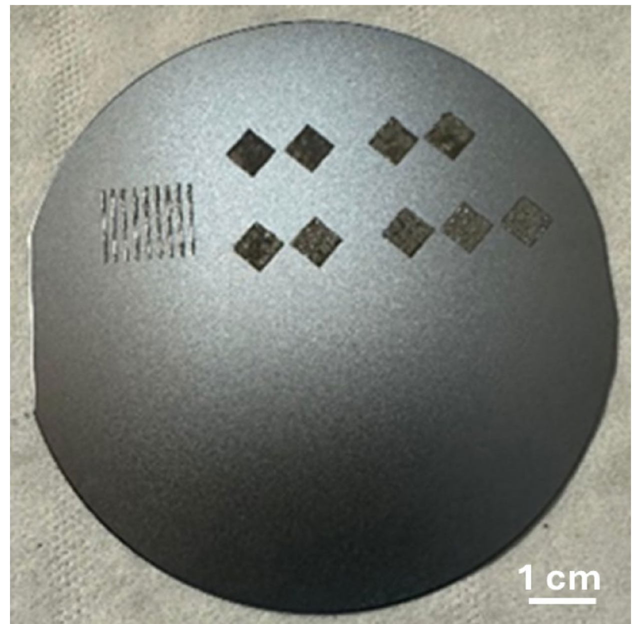

Fig. 5 Photograph of the $SnAg_3$ PBF-LB/M $SnAg_3$ deposits on silicon substrate printed with power of 70 W

Table 2 LOM images of first (samples A – I) and second job (samples J – R) cross-sectional areas of linear track scans

VED (J/mm3)		Hatch Distance (mm)					
		0,09		0,11		0,13	
Point Distance (mm)	0,06	A (110 W) VED = 114,07	J (70 W) VED = 72,59	B (110 W) VED = 93,33	K (70 W) VED = 59,39	C (110 W) VED = 78,97	L (70 W) VED = 50,26
	0,08	D (110 W) VED = 85,56	M (70 W) VED = 54,44	E (110 W) VED = 70,00	N (70 W) VED = 44,55	F (110 W) VED = 59,23	O (70 W) VED = 37,69
	0,1	G (110 W) VED = 68,44	P (70 W) VED = 43,56	H (110 W) VED = 56,00	Q (70 W) VED = 35,64	I (110 W) VED = 47,38	R (70 W) VED = 30,15

some cases, to the detachment of the metallic deposits from the substrate. This phenomenon, however, was not observed in samples printed with power of 70 W. In this case, the linear tracks adhered to the substrate, with no evident flaws. Thermal stresses are further increased at the interface by the different physical properties of the two materials. Indeed, Sn and Si have significantly different coefficients of thermal expansion (CTE), 22–23 ppm/K and 2.6-3 ppm/K respectively. By lowering the thermal gradient, the material contraction is reduced, thereby inducing less stress in the material and preventing Si brittle fracture. Moreover, despite the reduction in VED, all samples from the second job were found to be fully dense and free of any noticeable porosity.

Similar results were achieved with the square samples. In particular, no evident cracks were detected at Si-Sn interface, even though the interface area is larger compared to that of linear tracks. Representative images of samples A and P are reported in Fig. 6A, B.

Microstructural analysis was performed by FE-SEM at higher magnification on the cross-sections of the printed linear tracks and the squared deposits. It is observed that the microstructure changes along the height of the samples, as shown by representative micrographs in Fig. 7. Si inclusions, which are due to the partial melting of the substrate, are found in the $SnAg_3$ deposits. In the upper region of the cross-section, i.e., far from the Si substrate the density of Si inclusions is lower, and the typical solidification microstructure of the Sn-Ag alloy is well visible (Fig. 7C and D). In contrast, in the lower region, the Si structures are coarser and more frequent (Fig. 7B). The presence of Si dendrites suggests that Si is melted with Sn and it solidifies as primary phase. The microstructure is characterized by β-Sn solidification cells decorated at boundaries by Ag-Sn second phases. According to the XRD analysis results reported in Fig. 8, such particles are identified as Ag_3Sn precipitates. The formation of such phase is consistent with the equilibrium phase diagram of Ag-Sn system [28] and with literature results collected on similar solder alloys [29, 30]. These precipitates are formed at the end of the solidification in the inter-cellular regions [31]. Notably, Ag_3Sn is harder and more brittle than the β-Sn matrix and affects the mechanical properties of the solder, especially under thermal cycling conditions [32, 33]. The elemental distribution within the microstructure can be observed in the EDS maps that are reported in Fig. 7E-H.

The XRD diffractograms of the squared samples deposited with a power of 70 W show that all samples are constituted of the three main phases; namely, Sn, Si, and Ag_3Sn (as mentioned above). In samples J, K, and L, the Si peaks are more evident, while moving towards sample R the peaks of the Si phase become less intense. We assume that this observation is a result of different VEDs used to print the samples. Higher VEDs have resulted in melting of more wafer and mixing of Si with the Sn-based alloy due to the turbulence of the melt pool [34].

A quantitative evaluation of the damage caused by the laser beam to the silicon wafer was performed by measuring the maximum penetration depth of the melt pools into the substrate. By decreasing the VED, a shallower substrate penetration is achieved, down to 16 µm, as shown in Fig. 9A. This value is compatible with the typical thickness range of silicon chips commonly used in standard electronic applications, which generally varies from 50 to 500 µm depending on the device type and packaging requirements. For instance, ultra-thin dies used in advanced packaging or mobile applications may be thinned down to 50 µm or even less, while conventional dies for standard ICs often retain thicknesses in the range of 200–500 µm to ensure mechanical robustness and ease of handling during assembly [31, 35]. Therefore, the observed melt penetration remains well below the total die thickness in most practical cases, avoiding full-through melting and potential damage to functional regions of the silicon chip.

However, minimizing melt pool penetration also reduces the mechanical interlocking between the $SnAg_3$ deposit and the Si wafer, weakening the metallurgical anchorage at the interface and potentially compromising the mechanical robustness and long-term reliability of the thermal interface layer. As a result, a trade-off must be implemented between minimizing substrate damage and achieving a strong mechanical bonding at the interface.

As a consequence of the penetration of the melt pools in the substrate, a certain amount of Si is melted and mixed

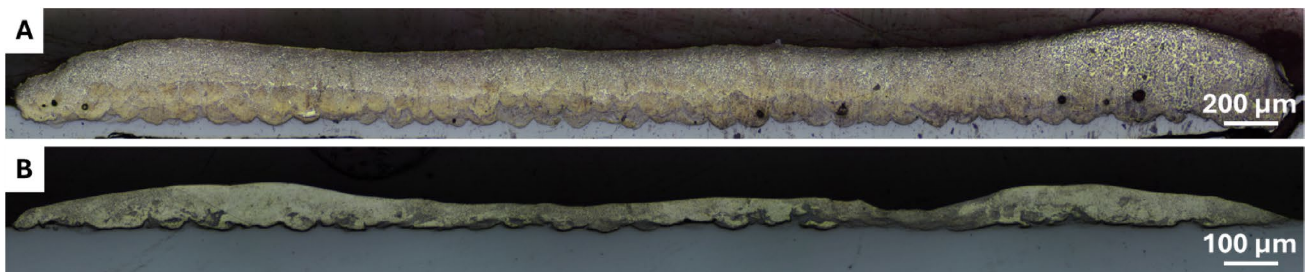

Fig. 6 LOM images of the cross-section of square sample A (**A**) and sample P (**B**)

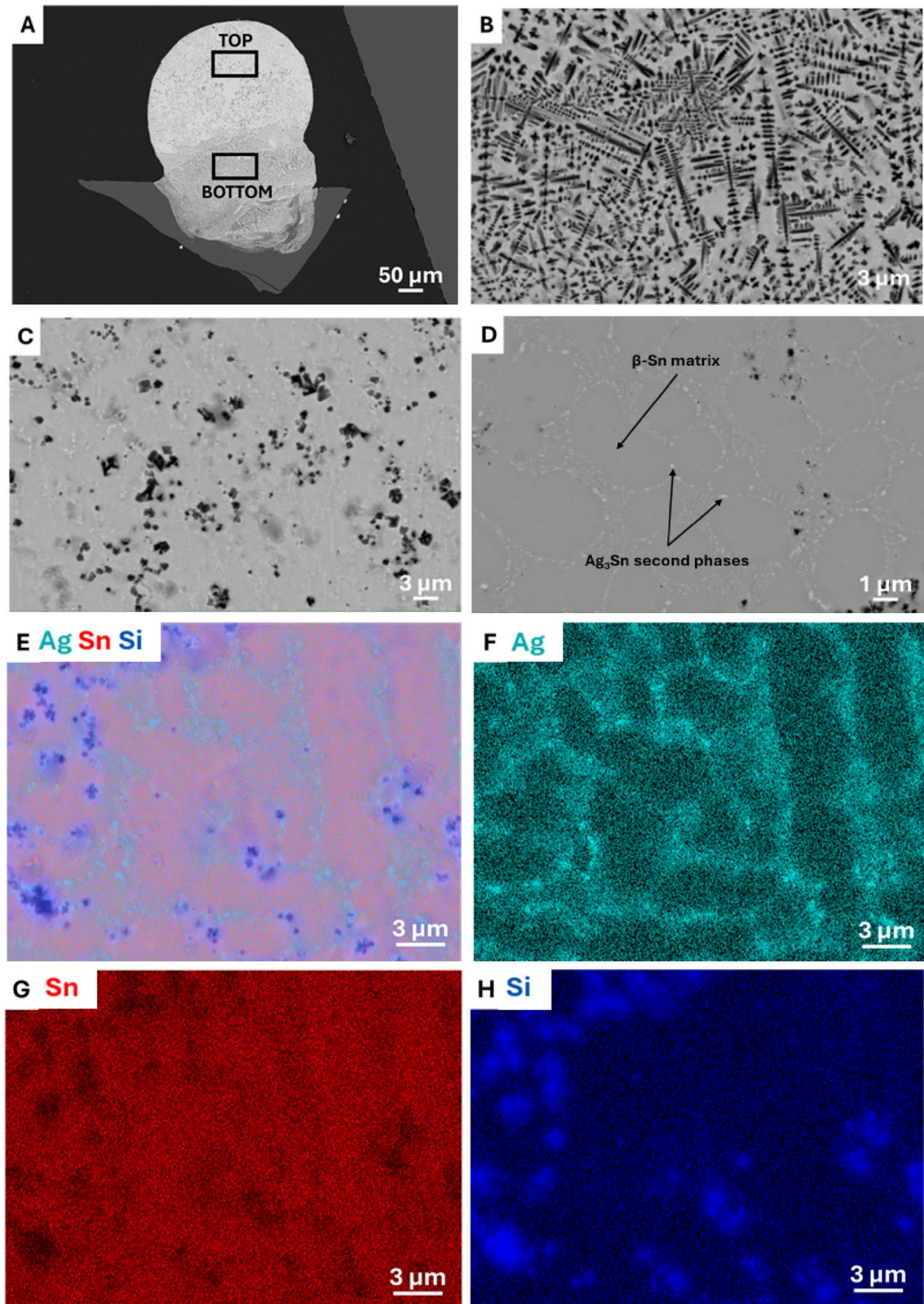

Fig. 7 FE-SEM representative image of the cross-sectional surface of sample A (**A**) and focus on the bottom (**B**) and top parts (**C**, **D**). EDS colour maps of the top part of the cross-sectional surface (**E**) and elemental distribution: Ag is predominantly present in Ag_3Sn intermetallics located at cell boundaries (**F**), β-Sn matrix (**G**) and Si particles randomly dispersed (**H**)

with Sn-Ag deposit. Si pick-up is measured by EDS in the top and bottom regions of the cross-sections of the square samples (Fig. 9B). As expected, the bottom region, which is closer to the substrate exhibited higher Si concentration compared to the top region. However, it was observed that the Si concentration is strongly influenced by the combinations of printing parameters. Specifically, a significant reduction in Si pick-up was observed with decreasing VED.

Figure 10 shows the EBSD images—i.e. phase maps and inverse pole figure (IPF) maps—of polished cross-section of samples K (Fig. 10A and B) and O (Fig. 10C and D). Figure 10E, instead, reports the Kernel average misorientation maps and scales of the two samples. As shown in Fig. 10A and C, relatively large and elongated Si structures protrude into the $SnAg_3$. These microstructural features have formed in both K and O samples by the relatively high VEDs—i.e. 59.39 and 37.69 J/mm^3, respectively, which have resulted in relatively large uptake of Si after melting and diffusing it into the Sn-based alloy.

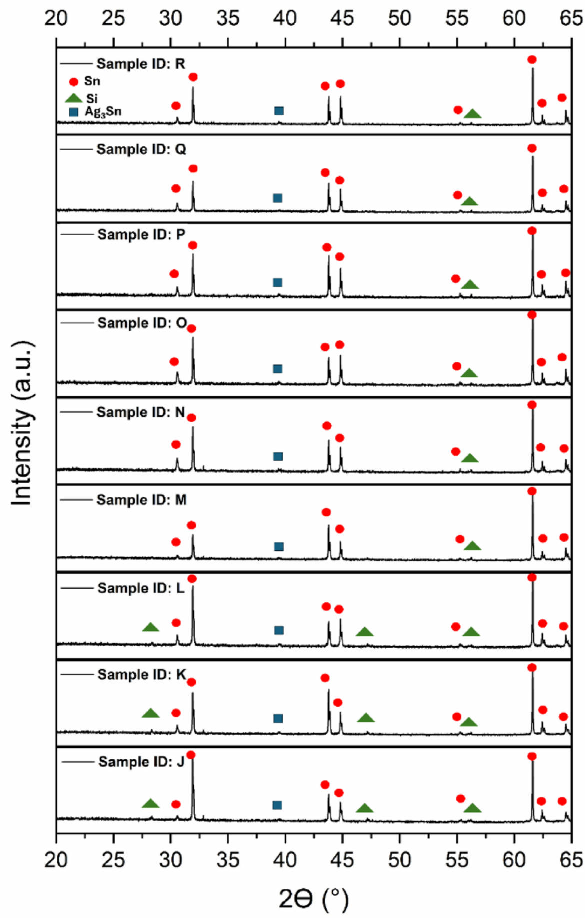

Fig. 8 XRD diffractogram of square samples printed with power of 70 W

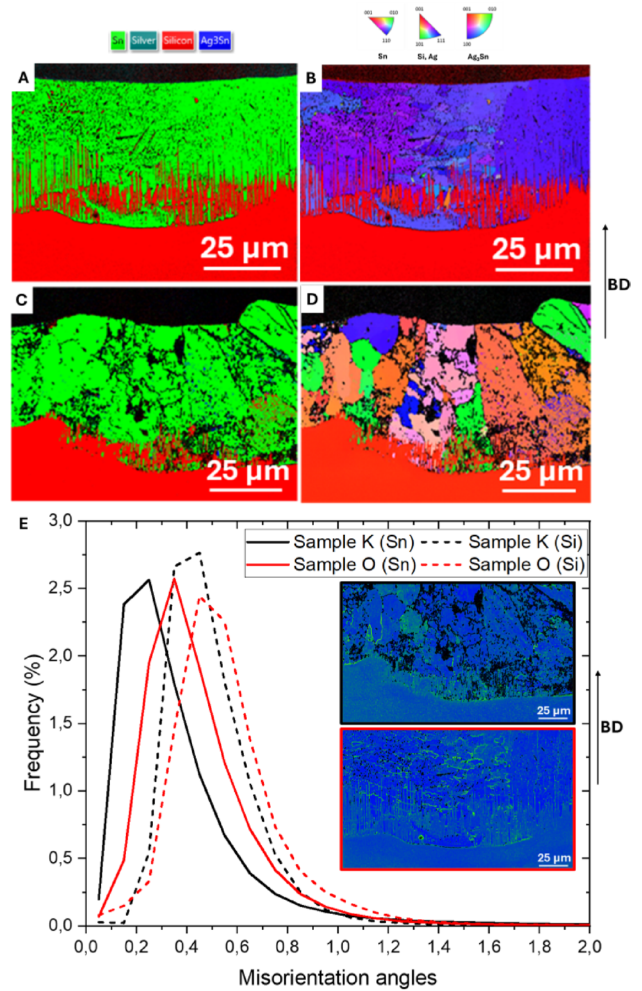

Fig. 10 EBSD images of the cross-section of sample K: phase map (**A**) and IPF – Building Direction map (**B**). EBSD images of the cross-section of sample O: phase map (**C**) and IPF – Building Direction map (**D**). Kernel average misorientation maps (**E**) of sample K (black) and sample O (red)

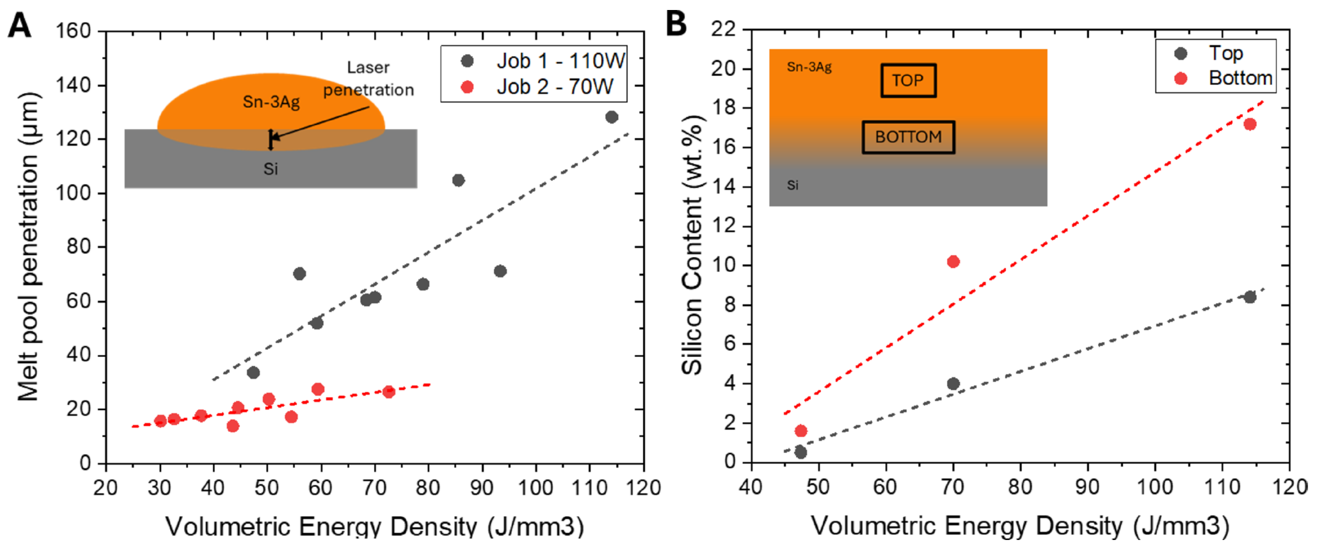

Fig. 9 Evaluation of the melt pool maximum penetration depth in silicon wafer (**A**) and silicon pick-up in $SnAg_3$ deposits (**B**) as a function of VED

In PBF-LB/M, the grain orientation and texture observed in the final microstructure are strongly influenced by the VED, which governs the thermal gradients and solidification conditions during printing. When a high VED is used, the material experiences larger and deeper melt pools, characterized by higher temperature and slower cooling rates, leading to the development of a more stable and directional thermal gradient. This promotes epitaxial grain growth along the build direction, typically aligned with the direction of maximum heat extraction. As a result, grains tend to grow in a preferentially oriented manner, leading to the strong texture along the 110 direction observed in the IPF map of sample K (Fig. 10B).

On the other hand, a low VED leads to smaller melt pools, involves lower temperatures and faster cooling rates, which cause more frequent nucleation events and weaker thermal gradients. This reduces the directional solidification driving force and promotes random grain orientations. Consequently, the microstructure of sample O appears with a random texture, as shown in IPF map in Fig. 10E.

Kernel Average Misorientation (KAM) maps shown in Fig. 10E provide localized information on the degree of misorientation. Higher KAM values indicate greater local misorientation, typically associated with residual deformation, crystallographic defects, or internal stresses [36]. Although the results obtained for samples K and O are very similar and comparable, some interesting differences can be observed. Looking at both Si and Sn misorientation peaks, the sample processed with lower VED (Sample O) is characterized by higher misorientation angles, while the high-VED sample (Sample K) shows a lower degree of local misorientation in both the deposited Sn alloy and the underlying Si substrate, respectively. This suggests that the low VED condition, although involving a smaller energy input and reduced melt pool size, leads to a more distorted microstructure, with greater accumulation of geometrically necessary dislocations. This can be explained by considering the lower temperatures associated with lower VED that are less efficient in relaxing residual stresses after solidification.

Moreover, the deposited Sn alloy exhibits higher misorientation angles than Si in both samples. This can be explained by the fact that Si has higher stiffness and strength than tin (E_{si}=130–185 vs. E_{Sn} = ~ 50 GPa; $\sigma_{f,\ Si}$ = 7 GPa vs. YS_{Si}=10–20 MPa [37–40]). Moreover, the predominant phase of a $SnAg_3$ alloy is β-Sn, which has a body-centred tetragonal (BCT) crystal structure [41]. This structure is known for its ductility, allowing the material to accommodate plastic deformation. In contrast, silicon possesses a diamond cubic crystal structure, characterized by strong covalent bonds. This structure renders silicon brittle at room temperature, limiting its ability to undergo plastic deformation.

The higher VED value exerted to sample K during its fabrication resulted in the formation of larger columnar Si-rich structures protruding into the Sn-based alloy. Han et al. has observed a similar trend in the Sn-Ag-Cu solder alloy system deposited on a Cu substrate [42]. Moreover, it has also been shown that the epitaxial growth of TIMs along the desired heat conduction direction can boost their heat conductivity performance [43, 44]. The microstructural texture of thermal interface materials have been shown to significantly affect their thermal conductivity [45]. Generally, the smaller the grain size and subsequently the larger the population of the grain boundaries, the higher the resistance for directional thermal conductivity. In our system, thermal conductivity is expected to be influenced by the grain structure along the build direction. Specifically, a lower density of grain boundaries is generally associated with improved heat transport properties. As shown in Figs. 10B, sample K exhibits fewer and larger grains, whereas sample O shows a finer and more randomly oriented grain structure. Although direct measurements of thermal conductivity of $SnAg_3$ on Si are not available at this stage, these microstructural differences suggest the potential for tuning thermal transport behaviour by tailoring the solidification structure through appropriate selection of process parameters. Moreover, the presence of silicon in the $SnAg_3$ interlayer can have a dual effect on thermal conductivity. On one hand, molten Si forms isolated inclusions or columnar structures rather than integrating into the metallic matrix, disrupting lattice continuity and increasing interface density. This enhances phonon and electron scattering, reducing the mean free path of conduction electrons and thus lowering thermal conductivity [46, 47]. On the other hand, crystalline Si has a much higher thermal conductivity than $SnAg_3$. When columnar Si structures remain connected to the underlying Si wafer, they act as thermal bridges, improving vertical heat transfer and potentially enhancing the overall thermal conductivity of the system [43].

The through-plane thermal conductivity of the $SnAg_3$ alloy was experimentally evaluated using TPS and LFA techniques. The results of these measurements are summarized in Table 3. The alloy exhibited an average thermal conductivity of 49.6 ± 0.9 W/m·K. The measured thermal conductivity of the $SnAg_3$ alloy was found to be lower than the values reported in the literature for similar compositions. For instance, Kehoe et al. [22] reported a thermal conductivity of approximately 74 W/m·K for a $SnAg_{3.5}$ alloy, while Eid et al. [48] measured a value of about 65 W/m·K for the SAC155 alloy (Sn – 1.5 wt% Ag – 0.5 wt% Cu). The lower conductivity observed in this study can be primarily attributed to differences in processing routes. In the present study, the samples were produced by PBF-LB/M, whereas the alloys reported in the cited works were realized

Table 3 Volumetric heat capacity, thermal diffusivity and thermal conductivity for the $SnAg_3$ alloy

Material	Volumetric heat capacity [MJ/m^3K] (measured via TPS)	Thermal diffusivity [mm^2/s] (measured via LFA)	Thermal conductivity [W/m·K] (calculated)
$SnAg_3$	1.397	36.2	50.6
		35.6	49.7
		36.3	50.7
		35.4	49.5
		34.7	48.5

by casting. During PBF-LB/M, the extremely high cooling rates promote the formation of a fine cellular microstructure with high grain boundary density [49], which enhance phonon scattering and thus reduce heat conduction efficiency [50]. Moreover, residual porosity act as additional thermal barriers, further decreasing the effective thermal conductivity. Conversely, cast alloys generally exhibit coarser grains, enabling more efficient phonon and electron transport. Therefore, the lower thermal conductivity measured in PBF-LB/M fabricated $SnAg_3$ samples is consistent with the expected microstructural and physical differences induced by the AM process.

4 Conclusions

This study demonstrated the successful fabrication of wafer-scale $SnAg_3$ TIM on silicon substrates using PBF-LB/M. By adjusting the VED, it was possible to control the laser-material interaction, influencing both the microstructure and the integrity of the silicon substrate. High VEDs promoted the formation of columnar Si-rich structures at the interface protruding into $SnAg_3$. However, high VED values also caused significant thermal stresses and cracking in the brittle silicon. In contrast, reducing the VED prevented substrate damage while still achieving full-density, well-bonded deposits, with melt pool penetration limited to 16 µm—compatible with standard silicon chip thicknesses. Microstructural and EBSD analyses revealed that higher VEDs resulted in more oriented grain structures with lower residual stress, while lower VEDs led to finer and more misoriented grains. The presence of Ag_3Sn intermetallics and varying silicon inclusion levels—both influenced by VED—highlight the importance of balancing thermal and mechanical performance. Overall, this work offers a new route for integrating high-performance TIMs directly onto wafers, with the potential to improve heat dissipation in advanced electronic devices.

Acknowledgements The authors would like to thank the European Space Agency (ESA) for supporting this research through the Open Space Innovation Platform (OSIP) programme. Special thanks are extended to all collaborators who contributed to the discussions and technical insights that helped shape this work.

Author contributions AM, AH wrote the draft, performed the experiments, prepared the figures, analysed the data. MM revised the draft, supervised the project. DJ, RC revised the draft, supervised the project, secured the fundings.

Funding Open access funding provided by Politecnico di Milano within the CRUI-CARE Agreement.

Data availability No datasets were generated or analysed during the current study.

Declarations

Competing interests The authors declare no competing interests.

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