Modular 76-channel instrument for Broadband Raman Spectroscopy

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***Abstract*—Raman microscopy is a label-free and non-invasive technique to reveal the chemical compounds of a sample. However, standard Raman microscopes acquire a single frequency at a time, preventing fast imaging as many biological applications require. Here, we present the preliminary development of a multichannel CMOS-based readout for the simultaneous acquisition of 76 frequencies of the Raman spectrum using the broadband stimulated Raman scattering technique. The acquisition system employs the lock-in technique and a custom multichannel CMOS chip to enable a low-noise operation and a parallel architecture for fast imaging. An FPGA-based DSP chain reduces the low-frequency noise by exploiting a 2-step frequency down-conversion technique. The hardware design of the system based on a motherboard and several module PCBs to realize a highly space-optimized architecture is also presented. Particular emphasis is placed on the experimental results obtained with the 2-step frequency down-conversion technique by means of bench tests.**

***Index Terms*—Broadband Raman Spectroscopy, multichannel, low noise, lock-in, FPGA, IC, 2-step demodulation, PCB, DSP.**

I. Introduction

Raman Spectroscopy is a non-invasive and non-destructive chemical analysis technique that provides detailed information about the molecular structures and interactions of a biological sample, since each molecule is characterized by a vibrational spectrum. Of particular interest is the cancer diagnosis [1], with the aim of replacing the traditional clinical practice (histological examination), which is slow and subjective, with a faster and more objective identification technique.

Standard Raman spectroscopy requires about 1 second to acquire a vibrational spectrum, resulting in an acquisition time of up to several hours for a high spatial resolution image [2]. Broadband Raman Spectroscopy has been proposed to measure all the relevant vibrational frequencies in parallel. In this case, the acquisition of the Raman spectrum requires a custom multichannel electronic system, exploiting a parallel acquisition in order to ensure fast imaging. Here the preliminary development of a 76-channel lock-in acquisition system for Broadband Raman Spectroscopy is presented.

This electronic system will be part of an innovative microscope for Raman spectroscopy extended to the fingerprint region [3]. This region, identified in the $600cm^{-1}-1800cm^{-1}$ range of wavenumbers, is the most informative for chemical identification as it contains multiple contributions from proteins and nucleic acids [4].

979-8-3503-0320-9/23/$31.00

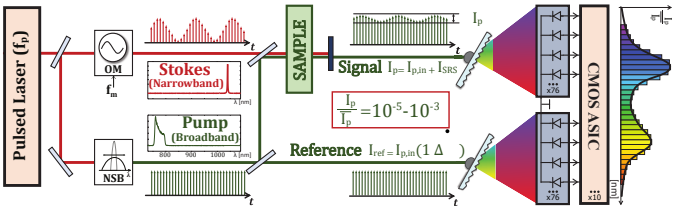

Fig. 1. Simplified optical SRS setup: an optical modulator (OM) produces a Stokes laser beam modulated at few MHz while a non-linear spectral broadening component (NSB) provides the Pump beam.

A. Broadband SRS

In Stimulated Raman Spectroscopy (SRS), two laser beams, at different frequencies ν_p and ν_s, also known as Pump and Stokes, are used to simultaneously excite a sample. For the Raman effect, there is a probability in the order of $10^{-3}-10^{-5}$, that some Pump photons will be scattered to the Stokes frequency, if the Raman shift $\Delta\nu = \nu_p - \nu_s$ matches a vibrational mode Ω of the molecules examined [2]. As a consequence, the optical power of the Pump is reduced by ΔP_p (Stimulated Raman Loss - SRL) and the optical power of the Stokes is increased by ΔP_s (Stimulated Raman Gain - SRG). The SRG and SRL spectra provide the vibrational fingerprint of the molecules and allow for their analysis and identification. The Raman spectrum can be acquired by scanning either the Pump or Stokes frequencies (single frequency SRS) or by employing a broadband laser beam, either Pump or Stokes (broadband SRS). The latter option enables faster imaging as the whole spectrum is acquired with a single measurement.

The optical setup required for Broadband SRS is schematically represented in Fig. 1. It consists of a single pulsed laser source used to generate two coherent laser beams, a broadband Pump and a narrow-band Stokes. The sample is placed in a microscope that allows for 2D scanning so that a Raman image can be acquired. A replica of the Pump beam is also provided, to be used as a reference signal for differential acquisition in order to compensate the laser intensity noise (the major noise contribution in SRS). While the Stokes is filtered out after the sample, the two Pump replicas (signal and reference) are spatially diffused over two pairs of Photodiode Arrays (PDAs), so that each element can acquire a specific wavelength of the Raman spectrum. A lock-in technique is implemented to detect the small signal generated by Raman scattering, removing the large average power of the laser. The lock-in frequency is

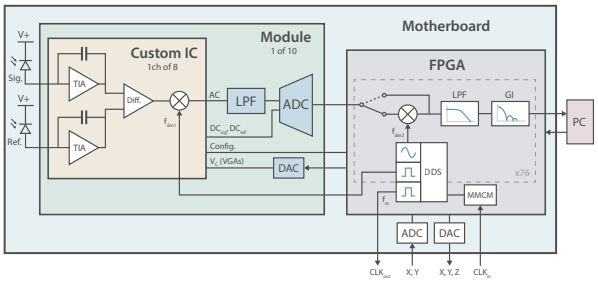

Fig. 2. Simplified diagram of the 76-ch platform, with the Custom IC (1 ch out of 8), the module (1 out of 10), the FPGA with the DSP chain (1 out of 76) and the motherboard highlighted.

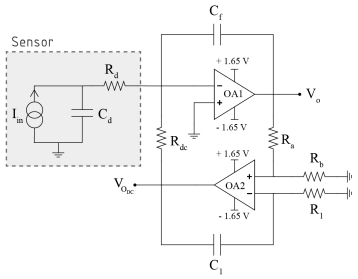

Fig. 3. Schematic of the first stage: Transimpedance Amplifier

selected in the 1-10MHz range, where a smaller laser intensity noise was observed.

II. 76-channel Crimson Platform

The 76-channel platform presented here has been designed as part of the CRIMSON European project with the following specifications: 1) 76 lock-in amplifiers operating in parallel; 2) differential readout for laser intensity noise compensation; 3) two operation modes (fast acquisition mode, with an acquisition time of a single spectrum smaller than $100\mu s$ and high resolution mode, with an acquisition time in the order of ms); 4) $10\mu W$ minimum optical power at each PD with an electronic noise lower than the intrinsic shot noise of the optical signal.

The system, schematically represented in Fig. 2, implements a modular architecture. It consists of ten 8-channel modules plugged into a motherboard. The optical signal is acquired by means of four 38-element PDAs (A5C-38) placed on the motherboard. Two PDAs for a total of 76 channels are used for the signal path, and the other two PDAs are devoted to the corresponding reference path. An Artix-7 FPGA provides all the control signals, implements a DSP chain for offset cancellation and adjustable lock-in bandwidth and manages the USB communication between the platform and the PC.

A. 8-channel CMOS front-end

Each module is based on an 8-channel custom Integrated Circuit, shown in Fig. 4 (on the right). The acquisition chain for each channel (able to acquire a single spectral line) is composed of two Transimpedance Amplifiers (TIA), one for the Reference and one for the Signal path, with two mean current management systems, a Variable Gain Amplifier stage (VGA), controlled by a network implementing an automatic balancing of the differential measurement, a cascade of two differential subtractor stages and a mixer that operates a Lock-In demodulation. This new IC proposes a solution for extending the optical power range of the measurements with respect to the old version [5][6]. In particular, it reduces by a factor 10 the minimum operative power down to $10\mu W$, maintaining an electronic noise below the intrinsic shot noise of the optical signal and fast acquisition of the Raman spectrum. The IC provides separate outputs for DC and AC signals to perform Raman normalization. A further analog acquisition chain is implemented off-chip with discrete components. Then, the acquired signals are digitized by a 16-channel 16-bit ADC and sent to the FPGA through the SPI interface.

A more detailed description of some IC-block is provided below:

1) Transimpedance Amplifier: The first stage uses a sophisticated low-noise transimpedance amplifier (TIA) with capacitive feedback and an additional feedback network to control the DC current coming from the photodiode. Fig. 3 shows the schematic of the preamplifier. The TIA topology with capacitive feedback is the most suitable choice because, unlike the one with a resistive feedback network, it does not suffer the trade-off between noise and gain. However there is a drawback: the stage tends to saturate pulse after pulse because of the mean current integrated into the feedback capacitance C_f . For this reason, a mean current discharging network is implemented. This circuit continuously reads the output mean voltage of the stage, proportional to the input DC current, and appropriately adjusts the voltage $V_{out,DC}$ to have the zero mean current in the feedback capacitance. Therefore the first stage is an improved version of the standard charge preamplifier and it is used to separate the DC current from the AC contribution to avoid saturation [7].

2) AGC network: This circuital block is dedicated to the equalization of Signal and Reference amplitudes to restore the symmetry required by the balanced SRS technique. For the network to successfully compensate the laser intensity noise, the two branches amplitudes have to be automatically equalized. This is obtained by adding two VGAs. The VGA_{sig} on the Signal path is characterized by a fixed gain, while the gain of VGA_{ref} on the Reference path can be tuned thanks to the variable tail current, that depends on a control voltage V_c. Two Peak Stretchers measure the pulse amplitude at the output of the VGAs. Then, an integrator compares the two amplitudes and modifies the control voltage Vc, and as a consequence the tail current of the Reference path, so to obtain the equalization of the signals at the output of the VGAs.

3) Mixer: At the end, the SRS signal is demodulated using a passive double-balanced mixer based on four transmission gate switches. The switching network is controlled by four digital clocks that are generated on-chip using the input

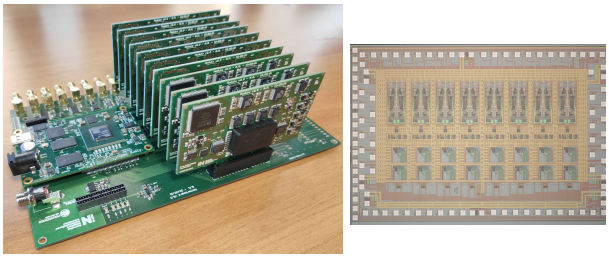

Fig. 4. Complete platform: 10 modules are mounted. The first visible module mounts a 3D-printed case to protect the custom IC (on the left). CRIMSON ASIC micrograph $4321\mu mx2854\mu m$ (on the right).

external clock provided by the laser. The clocks are non-overlapped to prevent that all four switches are closed at the same time.

The ASIC, shown in Fig. 4 (on the right), has been implemented in AMS $0.35\mu m$ CMOS technology. The IC die is composed of 8 independent differential channels and a shift register for every channel. In total, 82 PADs distributed along the chip's perimeter are required. It occupies an area of $12mm^2$ and has a nominal power consumption of $\approx 504mW$ with a power supply of 3.3V. The ASIC characterization is now underway.

B. Motherboard

The motherboard supports and interconnects the modules with the FPGA in a space-optimized fashion. Additional circuitry is present to acquire the external clock synchronized with the laser pulse and to generate the modulation clock for the Optical Modulator. A DAC and an ADC are employed to control and acquire the X, Y and Z coordinates of the microscope for imaging. The USB 3.0 interface featured by the XEM7310 is used for fast communication with a PC.

III. Two-step frequency down-conversion

The slow fluctuations of the output offset causing the resolution limit with low-bandwidth measurements observed in the 32-ch platform [8] is mainly due to the custom IC. They typically reach up to a few millivolts of amplitude in a time window of 10 minutes (see an example in Fig. 5),

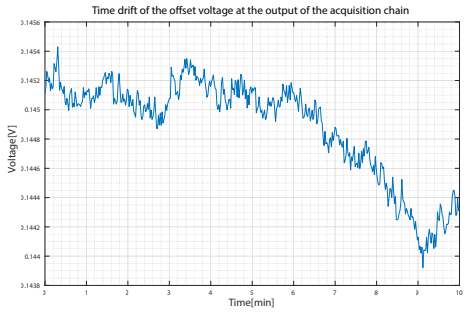

Fig. 5. Offset drift and low frequency noise acquired with a low-bandwidth measurement in a time window of 10 minutes: $\overline{V_{OS}} = 144.8mV$, $\sigma = 343\mu V$.

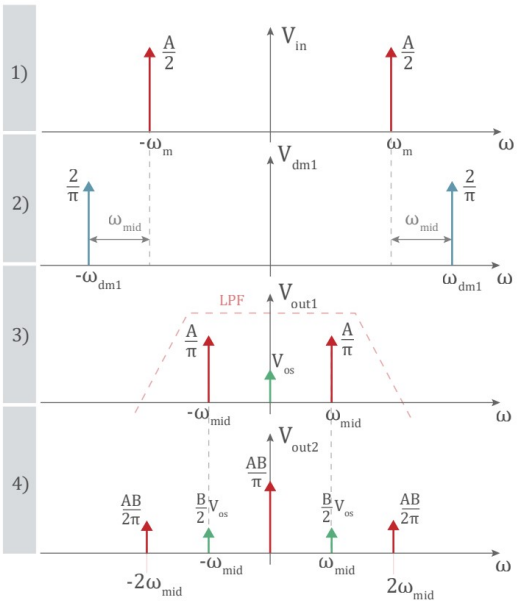

Fig. 6. 2-step frequency down-conversion: 1) Raman signal 2) 1^{st} demodulating signal. 3) Output of the 1^{st} analog demodulation and offset. 4) 2^{nd} digital demodulation result

limiting the possibility of detecting Raman signals of a few ppm in a long high resolution image. This low-frequency noise gets mixed with the Raman signal after the on-chip lock-in demodulation when the modulated signal is brought back to the base-band. In order to prevent this phenomenon, a 2-step frequency down-conversion approach, shown in Fig. 6, was used. The on-chip demodulation is performed in the analog domain and the second one in the digital domain, where no offset contribution is added. The on-chip demodulation is performed at $f_{mid} = f_{dm1} - f_m$ (f_{dm1}: first demodulation frequency, f_m: modulation frequency) so that the modulated Raman signal is not brought back to DC in the analog domain but to an intermediate modulation frequency f_{mid}. After being digitized by the ADC, a second sinusoidal demodulation is performed in the digital domain using a Direct Digital Synthesizer (DDS) such that $f_{dm2} = f_{mid}$ (f_{dm2}: second demodulation frequency) to bring the Raman signal back to the base-band and modulate the offset at f_{mid}. A 1^{st}-order digital low-pass filter sets the adjustable lock-in bandwidth, followed by a discrete time integrator implementing periodic notches at $k \cdot f_{mid}$ to filter out the spurious harmonics at f_{mid} and $2 \cdot f_{mid}$ generated by the second demodulation. Note that implementing a single demodulation in the digital domain would solve the problem of the low-frequency fluctuations of the analog mixer. However, it would require a fast ADC for each channel and a digital processor able to implement 76 lock-in amplifiers operating up to $10MHz$, dramatically increasing the complexity of the system. The additional demodulation step causes a SNR reduction by a factor $\sqrt{2}$, hence this technique should be enabled only for low-bandwidth measurements, where the resolution limit is

given by the observed offset drift and the 2-step frequency down-conversion ensuring a better SNR with respect to the direct demodulation, despite the aforementioned reduction. This technique also allows to use an intermediate frequency f_{mid} of a few kHz, hence relaxing the required ADC sampling frequency.

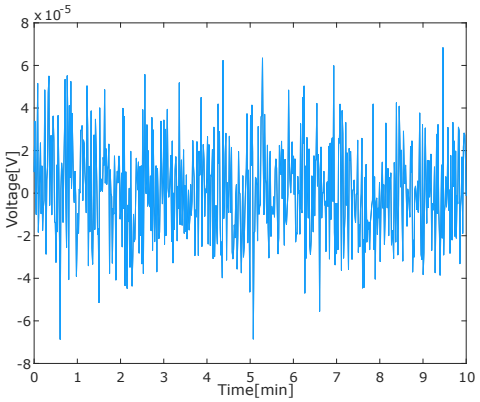

Fig. 7. DSP output after 2-step frequency down-conversion. Low-bandwidth measurement in a time window of 10 minutes: $\overline{V_{OS}} = 0.5\mu V$, $\sigma = 22.5\mu V$.

A. Experimental results

The 2-step frequency down-conversion has been tested on the bench to verify the correct operation. The plot in Fig. 7 shows the offset cancellation obtained with respect to Fig. 5. A comparison between the output results (when the input signal is a sinusoid with an amplitude of 25mV) in the case of direct and 2-step demodulation is reported in Table I. Moreover, the short and long measurement cases are distinguished to highlight the role of the offset drift in the measurement: in the first case the SNR reduction factor is confirmed, while in the second case the 2-step demodulation provides a better SNR by a factor 7.

TABLE I
SHORT (1 S) AND LONG ACQUISITION (10 MIN) TIME MEASUREMENTS.

		Direct Demod	**2-step frequency down-conv.**
short meas.	**SNR**	1285	903
long meas.	**SNR**	8270	57829

IV. FPGA FIRMWARE DESIGN

The DSP chain is mainly composed of a digital multiplier for the demodulation and an Infinite-Impulse-Response (IIR) low-pass filter implemented using a single multiplier and a discrete time integrator. Since the data stream acquired by the ADC is clocked at 40MHz, i.e. the clock signal used for SPI communication, while the DSP chain and the DDS operate synchronously to a 64MHz clock, a Clock Domain Crossing (CDC) must be performed to ensure the correct functionality of the design. The CDC is implemented by a Two-Clock FIFO synchronizer, that supports different write clock (40MHz) and read clock (64MHz) and performs the synchronization across clock domains internally [9].

V. CONCLUSION

With respect to the old system, the CRIMSON platform allows for a better acquisition of the fingerprint region of the Raman spectrum thanks to an higher number of channels. At the same time, it determines several design challenges due to the high number of resources required to implement 76 completely parallel acquisition chains and entailed different system-level optimizations. The detection of the optical signal is based on the lock-in technique. The front-end electronics is embedded in a $0.35\mu m$ CMOS custom IC. It integrates 8 channels and performs the low-noise amplification of the photogenerated current in a shot-noise limited operation for an average optical input power of down to $10\mu W$ per each photodiode. Based on this chip, a modular system has been developed consisting of a motherboard that supports and interconnects up to ten 8-channel modules. Particular efforts have been put into the implementation of a two-step frequency down-conversion, with the aim to compensate for the offset fluctuations of the acquisition chain experimentally observed in the 32-channel platform. For this purpose, a DSP chain has been implemented with the FPGA to operate the second demodulation step in the digital domain, allowing the compensation of the offset fluctuations. This technique has been fully tested and it shows an improved SNR for slow acquisitions (in the minutes range).

ACKNOWLEDGMENT

This project has received funding from the EU's Horizon 2020 research and innovation program under grant agreement No. 101016923. This work was partially performed at PoliFab, the micro-and-nanofabrication facility of Politecnico di Milano.

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