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Time-Multiplexed Control of Programmable Silicon Photonic Circuits Enabled by Monolithic CMOS Electronics

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Programmable photonic circuits require an electronic control layer to configure and stabilize the optical functionality at run-time. Such control action is normally implemented by supervising the status of the circuit with integrated light monitors and by providing feedback signals to integrated actuators. This paper demonstrates that the control action can be effectively performed with electrical signals that are time-multiplexed directly on the photonic chip. To this aim, the necessary electronic functionalities are monolithically integrated in a conventional 220 nm silicon photonics platform with no changes to the standard fabrication process. By exploiting a non-conventional structure to implement metal-oxide–semiconductor field-effect transistors, an electronic controller is co-designed into a programmable photonic circuit to enable a time-multiplexed readout of integrated photodetectors and sequential activation of thermal phase shifters with on-chip electronic memory. The accuracy of the time-multiplexed control, achieved on a time scale of less than 10 ms, is demonstrated by penalty-free routing of 10 Gbit s^{-1} modulated signals. This approach can be straightforwardly applied to large-scale photonic chips to reduce the number of required electrical input/output connections.

1. Introduction

Large-scale programmable photonic circuits consist of integrated networks of elementary optical elements[1] whose working point needs to be calibrated, stabilized and adaptively reconfigured to program the overall photonic functionality. A real-time active control layer, currently implemented by electronic feedback loops through external circuitry connected to on-chip light sensors and actuators, is thus needed to ensure reliable optical operations.[2–10] Although effective, the scaling of this approach is limited by the number of required electrical input/output (I/O) connections,[11,12] that approaches a prohibitive level in large-scale architectures. Flip-chip electronic-photonic interconnection via copper-pillar technology[13] enables larger I/O port counts with respect to wire bonding, yet implying extra assembly and packaging costs.

Monolithic integration of electronics and photonics on the same technological platform is envisioned as a way not only to overcome the electrical I/Os bottleneck but also to equip photonic chips with new enabling functionalities.[14–16] Building photonic circuits on consolidated microelectronic process stacks[17,18] has proven successful especially for the realization of high-speed optoelectronic systems, like transceivers operated at tens of GHz,[19,20] where the integration of front-end and driver circuits close to photonic modulators enables a strong reduction of parasitic effects. To this end, custom monolithic platforms have been developed, where the integration process of photonics and electronics has been reconsidered and optimized to maximize energy and speed performance.[21]

When the goal is instead real-time control of programmable optical systems, high-speed electronics is not necessary since the reconfiguration process and the compensation of functional drifts are usually performed with a μs to ms timescale. In these cases, the integration of electronic circuits, operating at few MHz, on a conventional photonic platform is a viable option to overcome the I/O bottleneck while keeping the cost low. This approach has been explored with the realization of junction field effect and bipolar transistors,[22,23] but their performance was not sufficient to integrate them into an operative photonic chip. Instead, CMOS devices and circuits have not been demonstrated so far because the process flow employed in silicon photonics technologies (with 220 or 300 nm silicon thickness) precludes the realization of vertical MOS transistors with good channel

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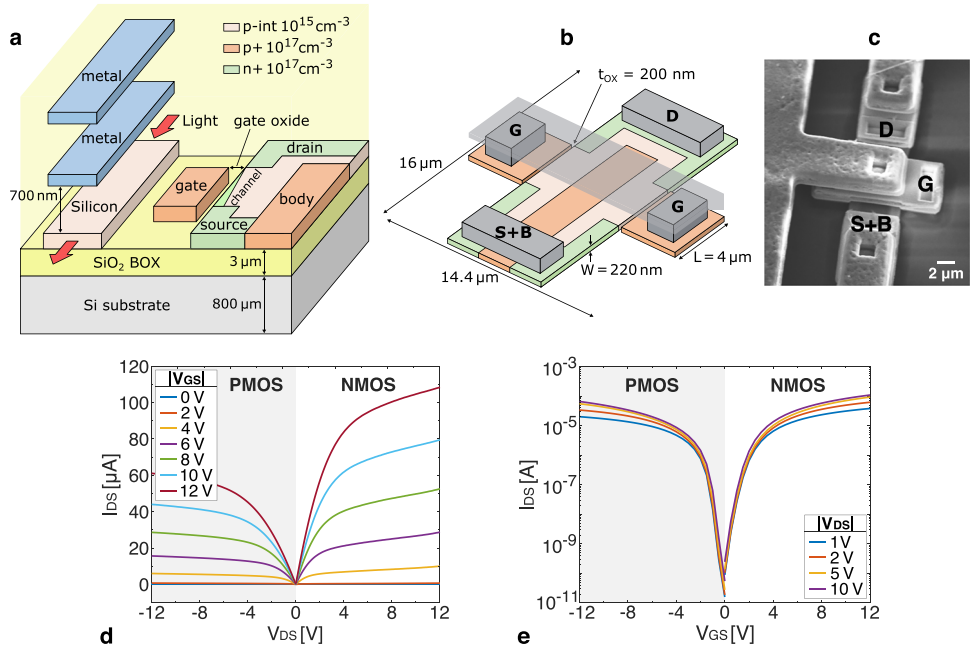

Figure 1. a) Overview of the typical technological stack of a silicon photonics chip, showing a section of the proposed side-wall MOSFET architecture. b) 3D quoted view and c) SEM image of the nMOS transistor cell. d) Experimental characteristic curves of the nMOS and pMOS transistors, measured at different gate–source voltages. e) Experimental trans-characteristic curves of the two devices, showing a high on/off ratio and a low leakage current regardless of the applied drain–source voltage.

modulation and sufficiently low threshold voltage. Indeed, silicon photonics lacks vertical control of diffusions and self-aligning gate process, it typically provides only a few doping concentrations (in the order of 10^{17} and 10^{20} cm^{-3}, both p- and n-type), and the metal layers employed for electrical routing are usually separated from the silicon of the waveguide (WG) core by at least 700 nm of oxide to minimize the propagation losses. Therefore, the optoelectronic devices implemented in this technology, like photodetectors, variable optical attenuators and modulators,[24–29] are usually resistors or lateral pn junctions, obtained by locally doping the same 220 nm-thick silicon layer that is used for the waveguides.

Here, a non-conventional strategy is proposed to design fully functional MOS field-effect transistors (MOSFETs) on a commercial 220 nm silicon-on-insulator (SOI) platform with no modifications to the standard fabrication processes, thus realizing a truly zero-change and technology-transparent integration. Starting from the elementary transistor, the implementation of several electronic building blocks with increasing complexity is described, up to the integration of electronic multiplexers enabling sequential monitoring, configuration and control of programmable photonic architectures, with the future perspective of complete autonomy of the chip from external electronics as the result of a full electronic–photonic co-design.

2. CMOS Side-Gate Transistors Design and Integration

Figure 1a shows the proposed MOSFET structure in the typical SOI stack employed in integrated photonic technologies (Advanced Micro Foundry, Singapore[30]). The 220 nm-thick silicon layer normally used for the WG core, lightly p-doped (nominally 10^{15} cm^{-3}), is here used as the substrate of transistors. A silicon gate is patterned next to the substrate, at the minimum distance allowed by the technology, and doped (10^{17} cm^{-3}, p-type) to ensure good conductivity. The gate oxide t_{ox} is 200 nm-thick in this technology, while the channel width W is set to 220 nm by the thickness of the silicon layer. The combination of low substrate doping and close proximity of the lateral gate ensures a threshold voltage between 1.5 and 2.5 V. The drain (D) and source (S) contacts of n-type MOSFETs are finally created by locally n-doping (10^{17} cm^{-3}) the silicon layer, while a p-type diffusion (10^{17} cm^{-3}) provides the body (B) contact of the transistor. The channel length L of 4 μm has been optimized with numerical simulations (Section S1, Supporting Information), to obtain high resistance and low leakage current in the off condition. The final MOSFET device is a symmetric elementary cell obtained by mirroring the single structure along the D–S axis, to exploit the silicon area efficiently (Figure 1b). The light doping level of the SOI layer, together with the charge trap effects happening at the Si/SiO_2 interface, make the native silicon behave almost as an intrinsic semiconductor with very low conductivity,[31] well suited to implement the substrate of both n- and p-type MOSFETs. The pMOSFET has thus been realized with the same geometry of the nMOSFET, simply by inverting the doping species that implement the transistor diffusion regions. If necessary, the conductivity of the native silicon can be further tuned by applying a proper voltage V_{sub} to the chip substrate, that acts as a common back-gate.

The fabricated transistors, shown in Figure 1c, have been systematically characterized. A $V_{sub} = -10$ V has been chosen to ensure good performance and low leakage currents to both

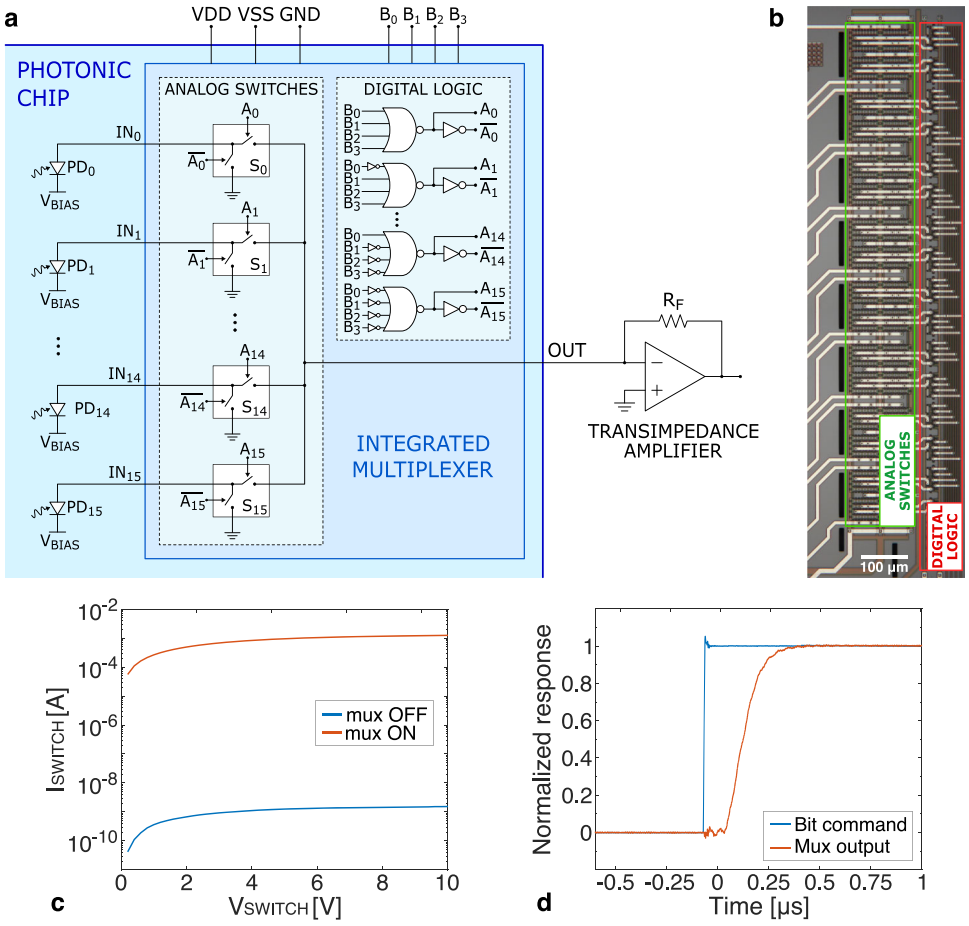

Figure 2. a) Schematic view of the on-chip integrated multiplexer and b) its microscope photograph. The circuit has a footprint of 250μm × 1200μm. c) Measured on/off response of the multiplexer, confirming the high on/off current ratio. d) Response time of the multiplexer when changing the configuration bits, from which a maximum switching frequency of ≈2 MHz is derived.

n- and p-type MOSFETs. Figures 1d and 1e report the measured characteristic and trans-characteristic curves of the two devices, respectively. The nMOS (pMOS) shows a threshold voltage of 2.45 V (1.8 V), a gain factor $\mu C_{ox} W/L$ of 4μA V^{-2} (2μA V^{-2}), an Early voltage of 35 V (55 V) and an inverse subthreshold slope of 350 mV dec^{-1} (250 mV dec^{-1}). These values are well suited for the realization of fully-functional electronic circuits with the desired performance, as it will be shown in the following sections.

3. Monolithic Electronic Multiplexer in a Silicon Photonic Chip

By using the MOSFETs structures described in Section 2, a 16-to-1 analog multiplexer (MUX) made of 596 nMOSFETs and 84 pMOSFETs has been monolithically integrated on the photonic chip, without impairing the fabrication of photonic devices. The electronic circuit includes 16 analog switches and the digital logic to properly drive them. The circuit has been designed to sequentially interrogate 16 monitor photodetectors (PDs),[32] which are connected to a single external transimpedance amplifier (TIA), or to drive 16 actuators (thermal tuners, see Section 4) integrated on the same chip to manage a programmable photonic circuit.

The schematic of the designed multiplexer connected to 16 PDs is shown in **Figure 2**a. Single-pole double-throw (SPDT) analog switches are used to connect one photodiode to the external amplifier and the others to ground, keeping them biased always at the same operating voltage to reduce the switching time of the circuit. A CMOS digital logic drives the correct switches according to the input address bits. The overall footprint of the multiplexer is 250μm × 1200μm (Figure 2b). The measured on and off currents of each channel, shown in Figure 2c, confirm that the circuit properly connects and disconnects the photodiodes according to the digital command. The value of the on resistance (R_{ON} = 1.8 kΩ) ensures that the bias voltage of the PDs is not significantly modified when currents up to few hundreds of μA flow through the MUX. In addition, being R_{ON} well below the equivalent resistance of the photodiodes, the noise contribution of each switch is negligible with respect to the series noise of the following TIA, thus not affecting the sensitivity of the readout.

The transfer function of each switch has a measured bandwidth of about 100 MHz, allowing to route signals up to this frequency on all the channels. Figure 2d reports the transient that occurs when changing the configuration of the digital bits. A settling time ≈500 ns is observed, corresponding to a maximum switching frequency of 2 MHz. This allows to perform

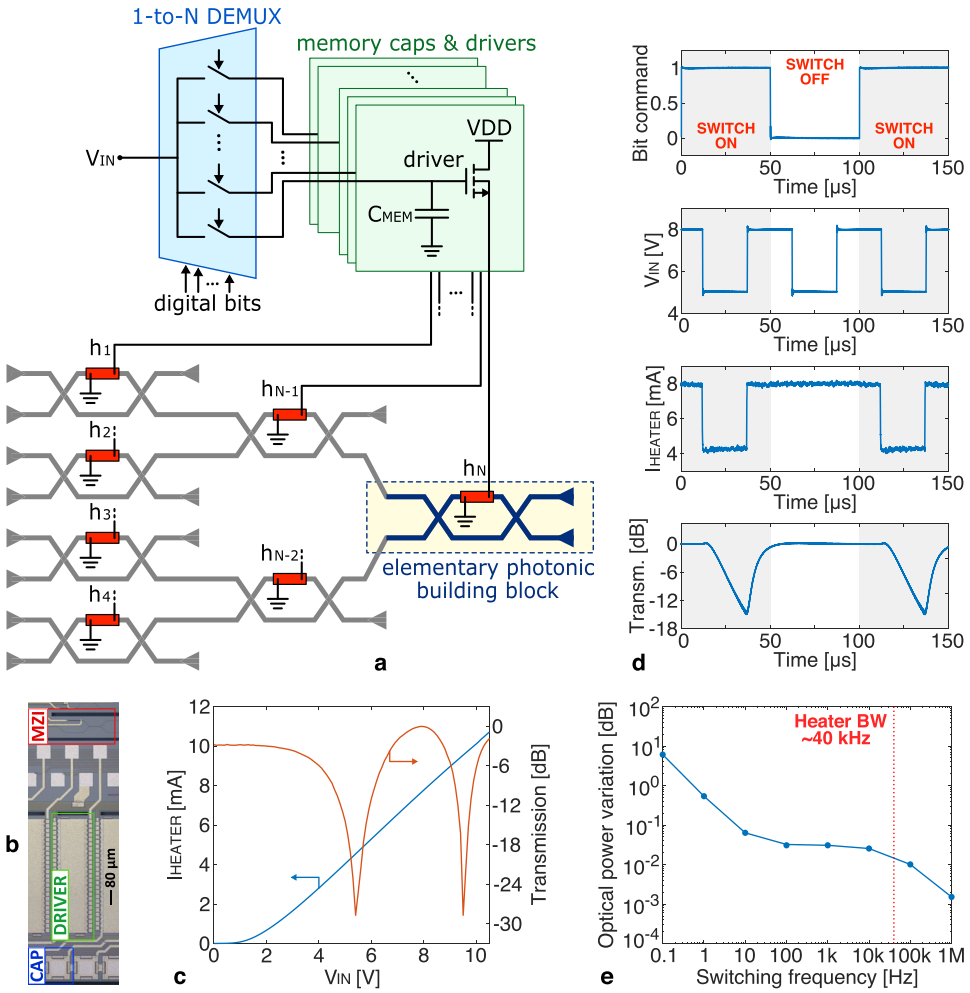

Figure 3. a) Schematic view of the connections necessary to sequentially drive volatile actuators in a binary-tree mesh of MZIs and b) microscope photograph of an integrated heater driver incorporating the memory capacitor. c) Measured current in the actuator as a function of the gate voltage and corresponding response of a MZI. d) Measured heater current and MZI transmission as a function of the driver gate voltage and bit command. As expected, when the switch is turned off, the heater current is held constant and the MZI transmission does not change. e) Variation of optical power at the output of a MZI operated in cross condition, as a function of the S&H refresh frequency. Above 10 Hz, the MZI working point does not change.

time-multiplexing of 16 PDs at a readout rate of about 100 kHz, linearly scaling up to 160 PDs interrogated at about 10 kHz. The minimum refresh rate required by a particular application is indeed what limits the maximum number of channels of the device. The detailed measurement setup is described in Section S2, Supporting Information.

The number of electrical connections required to operate an N-to-1 multiplexer connected to N devices is

$$N_{\text{CONN, MUX}} = \log_2(N) + 4 \quad (1)$$

since, in addition to the bits providing the digital address, one output port, two power supplies (V_{DD}, V_{SS}) and one reference voltage (GND) are needed. Since N connections are instead required to address each device in the conventional way, the use of the multiplexer is convenient for $N \geq 8$, the advantage becoming more evident as the number of devices increases (doubling the MUX channels requires only adding one digital address bit). The device is thus pivotal in enabling the functional scaling of complex photonic architectures, where a large number of sensors and actuators need to be addressed.

4. Sequential Control of Volatile Actuators with an On-Chip Electronic Memory

The time-multiplexed approach can be effectively exploited also to sequentially control integrated actuators, even when they are volatile, that is, they require a continuous bias for their operation, as in the case of thermal tuners. To this end, an on-chip memory device needs to be integrated on the photonic chip together with the actuator driver, in the configuration shown in **Figure 3**a. The power transistor, made of 700 nMOSFETs in parallel, is connected in source follower configuration to supply the heater, with a linear relation between gate voltage and current. The memory functionality is instead provided by a sample & hold (S&H) architecture connected to the driver gate. The S&H can be made by exploiting the switches of a DEMUX, with the same structure shown in Section 3, and a bank of memory capacitors (C_{MEM}) of

about 10 pF each, obtained by interleaving the metal layers available in the technology. When a switch is closed, the input charges the corresponding memory capacitor and defines the heater current. When the switch is opened, the memory capacitor keeps the gate voltage constant, maintaining the working conditions of the photonic device stable. The maximum hold time, related to the leakage current of the switches and to the memory capacitance, is ≈1 s in our prototype.

A top-view photograph of a power MOSFET and a single S&H channel is shown in Figure 3b. To test its functionality, the integrated driver has been connected to a thermal phase shifter in one arm of a balanced Mach–Zehnder interferometer (MZI) (Figure 3a). Figure 3c shows that a current of up to 11 mA (blue curve) can be delivered by the driver when a supply of 12 V is used. This translates into a phase shift of around 3π in the thermally tuned waveguide, as confirmed by the voltage-dependent transmission of the MZI (red curve). Figure 3d shows the operation of the S&H circuit. The DEMUX bit command and the input voltage V_{IN} are controlled with two square waves at 10 and 20 kHz, respectively. The measurement shows that, as expected, the input voltage causes variations of the heater current only when the S&H switch is closed (switch ON). Instead, when the switch is OFF, the current is kept constant by the memory capacitor and it is not affected by the input. The response time of the driver (≈300 ns) is much faster than the actuator thermal time constant (≈10μs), confirming that the electronic circuit does not limit the functionality of the MZI.

The discharge time of the S&H has been investigated to verify the possibility of implementing an on-chip electronic memory for volatile thermal actuators. To this end, the driver voltage has been set to 5.5 V to bias the MZI at the minimum transmission point (−26 dB, Figure 3c) and the S&H bit command has been driven with a square wave of variable frequency. The change of optical power at the MZI output due to the S&H discharge is shown in Figure 3e. When the S&H is operated with a switching frequency above 100 Hz a negligible degradation of 0.03 dB is measured, demonstrating that the driver can maintain the heater current constant. The residual error is due to charge injection effects, that modify the stored voltage when the switch is opened. Since the S&H is made with a DEMUX having the same structure and performance of the MUX discussed in Section 3, with 500 ns addressing time, it is possible to estimate that up to 20 000 actuators can be time-multiplexed without penalties in the optical performance.

The impact of the discharge of the S&H driver on the quality of optical signals transmitted through MZI switches has also been investigated. To this aim, the portion of the photonic circuit shown in the inset of **Figure 4**a has been considered, where two optical signals modulated at 10 Gbit s^{-1} on-off keying (OOK) are injected at two input ports. The reference and the interference signals share the same wavelength of 1550 nm and have a power of −4 and −8 dBm respectively. The impact of the interference signal is critically dependent on the working point of the first MZI, which is set and maintained by the S&H driver. Figure 4a shows the bit-error-rate (BER) measured at the reference signal output, for different values of the S&H switching frequency. The working point of the MZI is kept stable for refresh frequencies above few Hz, resulting in a BER that approaches the value of 10^{-11}, measured when the interference is switched off. A degradation of the BER instead occurs at low frequency because the S&H discharge induces a drift of the MZI bias point and a consequent lower suppression of the interference signal. Figure 4b shows the eye diagrams that are observed when the suppression of interference signal is minimum (max interference) and when the S&H switching frequency is set to 0.1 and 10 Hz respectively, the latter providing a suppression of more than 20 dB (see Figure 3c).

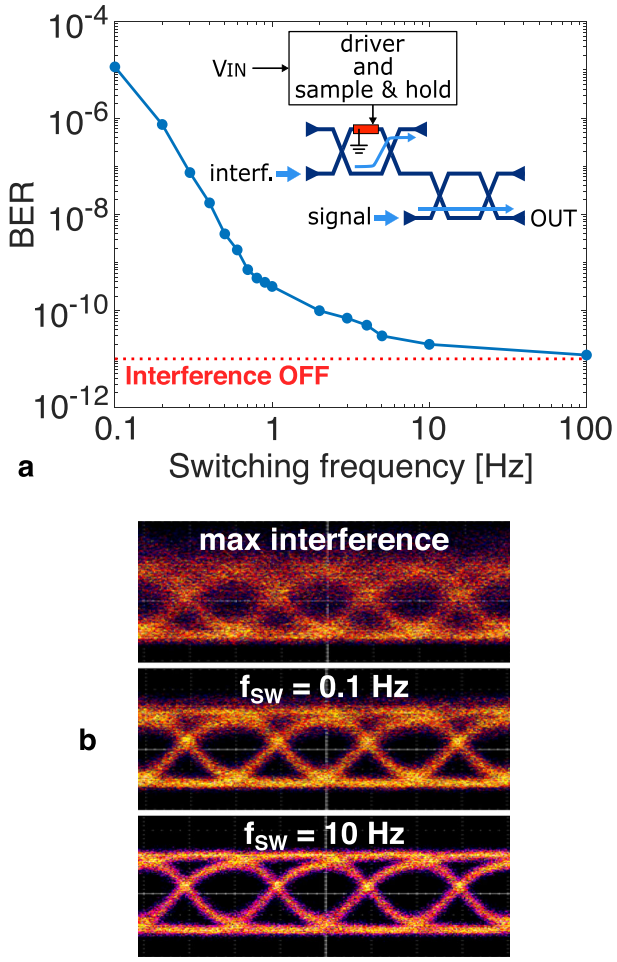

Figure 4. a) BER measurement at 10 Gbit s^{-1}, acquired at the output of the optical structure shown in the inset of the figure, when controlling the heater driver to minimize the interference, as a function of the switching frequency. b) Corresponding eye diagrams at the output. The two measurements confirm that the S&H allows to time-multiplex the actuators with a refresh rate down to 10 Hz without penalties.

5. Time-Multiplexed Control of a Photonic Router

The time-multiplexed control strategy enabled by the integrated electronic circuits has been applied to configure a programmable optical architecture and automatically route optical signals. The optical router is made with a four-layer binary tree of MZIs (**Figure 5**a), comprising 110 photonic building blocks, that steer the light from one of the 16 inputs to a single optical output. A top-view picture of the photonic chip integrating the optical router and the integrated MUX for sensor readout is shown in

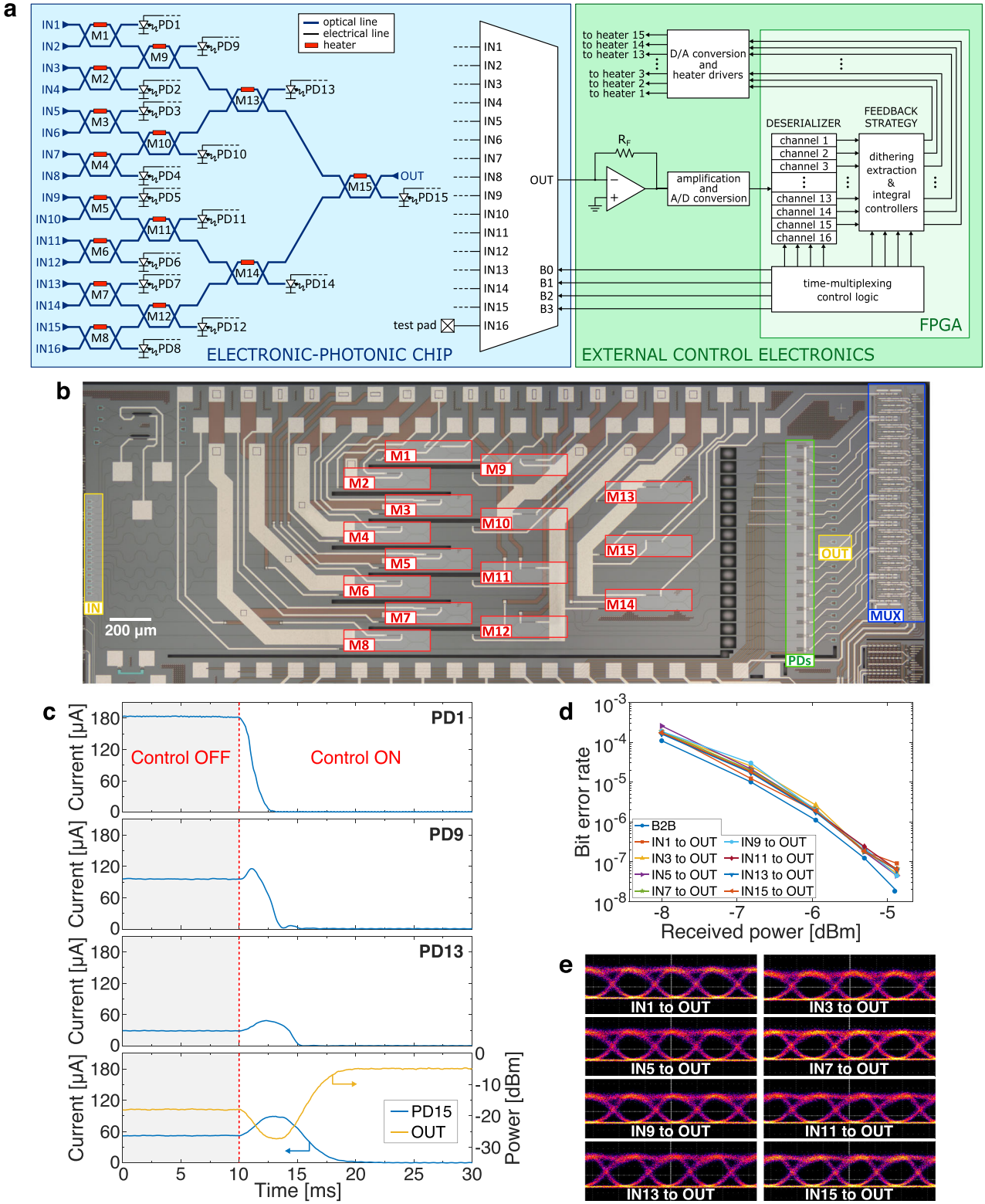

Figure 5. a) Schematic view of the complete electro-optical system, including the photonic chip with the integrated multiplexer and the control electronics. b) Microscope photograph of the electronic–photonic chip. c) PD currents during the configuration transient of the mesh for the IN1-to-OUT path, happening in less than 10 ms. d) BER measurement and e) eye diagrams for 8 different I/O configurations, obtained when routing a 10 Gbit s^{-1} modulated signal through the controlled photonic chip. Each point of the BER curves has been acquired on a time window of 4 min, for an overall experiment duration of about 3 h.

Figure 5b. The state of each MZI is observed with 15 monitor PDs. Their photocurrent is routed by the MUX to the readout TIA and then used to tune the working point of each MZI switch. The MUX reduces the number of electrical I/Os with respect to the case of parallel detection,[11,33,34] as given by Equation (1), and it simplifies the readout scheme, since only one TIA is needed to monitor the state of the entire photonic system. A time-multiplexed logic has been implemented to control the router functionality in real-time, by exploiting the dithering technique in combination with integral controllers.[35] The dithering frequency has been set to 2 kHz and the MUX switching to 80 kHz, allowing to read the four sensors along each path at 20 kHz, which is enough to avoid aliasing phenomena. Deserialization of the readout is needed to extract the four data sequences from a single analog-to-digital converter (ADC) bit stream and to generate the control voltages to be applied to the correct heaters, depending on the selected light path. The deserializer, dithering extraction block, integral controllers and system management logic have been implemented with an FPGA housed on the external control electronic board (see Section S3, Supporting Information).[36]

Figure 5c shows the configuration transients of the photonic router when the control system is active, obtained by monitoring the power on the 4 PDs along the selected path and the output signal. The laser has been injected at input port IN1 and after 10 ms the configuration procedure has been activated. The heater voltages, starting from random initial conditions, are updated by the feedback loop in order to minimize the photocurrents of PD1, PD9, PD13, PD15, so that all the light is routed to the output port OUT. The configuration of each MZI is performed in few ms and the full path is established in less than 10 ms. The time-multiplexed logic has been tested for all the other input–output configurations, demonstrating that it does not affect the readout of the PDs nor produce electrical crosstalk among them.

Transmission measurements have been performed to quantify the degradation of optical signals when the time-multiplexed control strategy is applied to the entire router architecture (see Section S4, Supporting Information for the detailed optical setup). A 10 Gbit s^{-1} OOK is injected in the photonic circuit and observed at the output of the chip. Figure 5d shows the BER measurements acquired for eight different input-output configurations, where each data point is obtained on a time window of about 4 min. The results show an average power penalty of only 0.3 dB with respect to the back-to-back case (B2B) (propagation through a straight waveguide integrated in the same chip) and a penalty variation of ≈0.2 dB among the different configurations. The curves confirm the correct operation of the MUX and of the time-multiplexed control strategy, which does not limit the optical performance. Effective mitigation of thermal fluctuations of the photonic chip is also demonstrated, since the measurements are carried out on an overall time window of about 3 h. Figure 5e shows the eye diagrams for the same input–output configurations, that remain clearly open in all the conditions with an average extinction ratio of 9 dB and a variation of 0.1 dB among the selected light paths.

6. Conclusions

This work demonstrated the possibility of controlling silicon photonic circuits by time-multiplexing the required electrical signals directly on the photonic chip, thanks to the integration of monolithic CMOS transistors. This approach has been exploited to sequentially interrogate photodetectors integrated into an MZI mesh, with a millisecond timescale. Similarly, time-multiplexing of electrical control signals has been used to set the working point of thermal actuators and hold it through the implementation of analog electrical memories, with no penalty with respect to a traditional external driving circuit. This latter functionality can be straightforwardly applied to provide electronic memory to generic volatile actuators, including electro-optic, ferroelectric, piezoelectric or liquid crystal phase shifters.

The advantages of on-chip multiplexing become more and more pronounced when the complexity of optical architectures increases, thanks to a significant reduction in the number of input/output electrical connections from the photonic circuit to the external control electronics. This approach can thus be a key enabler for further functional scale-up of integrated optical systems, especially when both MUX and DEMUX circuits are incorporated and operated on the same chip. In addition, since the proposed monolithic CMOS devices can be integrated into standard active silicon photonics platforms, a vast class of optical chips is expected to include on-board electronic functionalities in the future, providing an effective control layer at zero cost and without penalties in the photonic performance.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

CMOS electronics, monolithic integration, silicon photonics, time-multiplexed control

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